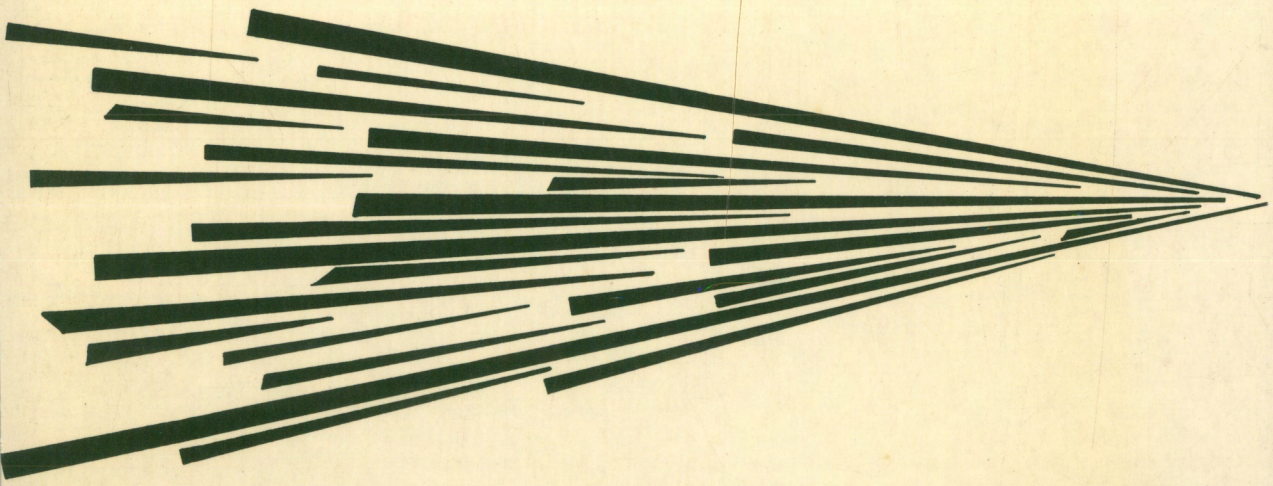
mecl high-speed integrated circuits



MOTOROLA Semiconductors

MOTOROLA

MECL INTEGRATED CIRCUITS

Prepared by
Technical Information Center

This book presents technical data for a broad line of MECL integrated circuits. Complete specifications for the individual circuits are provided in the form of data sheets. In addition, selector guides are included to simplify the task of choosing the best combination of circuits for optimum system architecture.

The information in this book has been carefully checked and is believed to be reliable; however, no responsibility is assumed for inaccuracies. Furthermore, this information does not convey to the purchaser of microelectronic devices any license under the patent right of any manufacturer.

Printed in Switzerland
293/J78/10.0

Series B

CONTENTS

DEVICE INDEX

DEVICE INDEX (continued)

GENERAL INFORMATION

GENERAL INFORMATION
SECTION I — HIGH-SPEED LOGICS

High speed logic is used whenever improved system performance would increase a product's market value. For a given system design, high-speed logic is the most direct way to improve system performance and emitter-coupled logic (ECL) is today's fastest form of digital logic. Emitter-coupled logic offers both the logic speed and logic features to meet the market demands for higher performance systems.

MECL PRODUCTS

Motorola introduced the original monolithic emitter-coupled logic family with MECL I (1962) and followed this with MECL II (1966). These two families are now obsolete and have given way to the MECL III (MC1600 series), MECL 10,000, MECL 10800, and PLL (MC12000 series) families.

Chronologically the third family introduced, MECL III (1968) is a higher power, higher speed logic. Typical 1 ns edge speeds and propagation delays along with greater than 500 MHz flip-flop toggle rates, make MECL III useful for high-speed test and communications equipment. Also, this family is used in the high-speed sections and critical timing delays of larger systems. For more general purpose applications, however, trends in large high-speed systems showed the need for an easy-to-use logic family with propagation delays on the order of 2 ns. To match this requirement, the MECL 10,000 Series was introduced in 1971.

An important feature of MECL 10,000 is its compatibility with MECL III to facilitate using both families in the same system. A second important feature is its significant power economy — MECL 10,000 gates use less than one-half the power of MECL III. Finally, low gate power and advanced circuit design techniques have permitted a new level of complexity for MECL 10,000 circuits. For example, the complexity of the MC10803 Memory Interface Function compares favorably to that of any bipolar integrated circuit on the market.

The basic MECL 10,000 Series has been expanded by a subset of devices with even greater speed. This additional series provides a selection of MECL 10,000 logic functions with flip-flop repetition rates up to 200 MHz min. The MECL 10,200 Series is meant for use in critical timing chains, and for clock distribution circuits. MECL 10,200 parts are otherwise identical to their 10,000 Series counterparts (subtract 100 from the MECL 10,200 part number to obtain the equivalent standard MECL 10,000 part number).

Continuing technical advances led more recently to the development of the M10800 LSI processor family. The M10800 family combines the performance of ECL with the system advantages of LSI density. Architectural features of the M10800 family significantly reduce the component count of a high-performance processor system. The M10800 LSI family is fully compatible with the MECL 10,000 and MECL III logic families for a complete selection of system design components.

MECL FAMILY COMPARISONS

Feature	MECL 10,000			MECL III
	10,100 Series 10,500 Series	10,200 Series 10,600 Series	10,800 LSI*	
1. Gate Propagation Delay	2 ns	1.5 ns	1 - 2.5 ns	1 ns
2. Output Edge Speed	3.5 ns	2.5 ns	3.5 ns	1 ns
3. Flip-Flop Toggle Speed	160 MHz	250 MHz	N.A.	300 - 500 MHz
4. Gate Power	25 mW	25 mW	2.3 mW	60 mW
5. Speed Power Product	50 pJ	37 pJ	4.6 pJ	60 pJ

*Average for Equivalent LSI Gate.

FIGURE 1a — GENERAL CHARACTERISTICS

Ambient Temperature Range	MECL 10,000	M10800	MECL III	PLL
0° to 75°C	MCM10100 Series	–	MC1697P	MC12000 Series
-30°C to +85°C	MC10100 Series MC10200 Series	MC10800 Series	MC1600 Series	MC12000 Series
-55°C to 125°C	MC10500 Series MC10600 Series MCM10500 Series	–	MC1648M	MC12500 Series

FIGURE 1b – OPERATING TEMPERATURE RANGE

Package Style	MECL 10,000	M10800	MECL III	PLL
16-Pin Plastic DIP	MC10100P Series MC10200P Series	–	MC1658P	MC12000P Series
16-Pin Ceramic DIP	MC10100L Series MC10200L Series MC10500L Series MC10600L Series MCM10100L Series MCM10500L Series	MC10804L MC10807L	MC1600L Series	MC12000L Series MC12500L Series
16-Pin Flat Package	MC10500F Series MC10600F Series MCM10500F Series	–	MC1600F Series	MC12513F
20-Pin Ceramic DIP	–	MC10805L	–	–
24-Pin Plastic Package	MC10181P	–	–	–
24-Pin Ceramic DIP	MC10181L, MC10581L	MC10802L	–	–
24-Pin Flat Package	MC10581F	–	–	–
48-Pin Ceramic Quil	–	MC10800L Series	–	–
14-Pin Plastic DIP	–	–	MC1648P	MC12000P MC12002P MC12020P MC12040P
14-Pin Ceramic DIP	–	–	MC1648L	MC12000L MC12002L MC12020L MC12040L
14-Pin Flat Package	–	–	MC1648F	MC12540F
8-Pin Plastic DIP	–	–	MC1697P	–

For package information see page 1-28.

FIGURE 1c – PACKAGE STYLES

MECL IN PERSPECTIVE

In evaluating any logic line, speed and power requirements are the obvious primary considerations. Figure 1 provides the basic parameters of the MECL 10,000, M10800, and MECL III families. But these provide only the start of any comparative analysis, as there are a number of other important features that make MECL highly desirable for system implementation. Among these:

Complementary Outputs cause a function and its complement to appear simultaneously at the device outputs, without the use of external inverters. It reduces package count by eliminating the need for associated invert functions and, at the same time, cuts system power requirements and reduces timing differential problems arising from the time delays introduced by inverters.

High Input Impedance and Low Output Impedance permit large fan out and versatile drive characteristics.

Insignificant Power Supply Noise Generation, due to differential amplifier design which eliminates current spikes even during signal transition period.

Nearly Constant Power Supply Current Drain simplifies power-supply design and reduces costs.

Low Cross-Talk due to low-current switching in signal path and small (typically 850 mV) voltage swing, and to relatively long rise and fall times.

Wide Variety of Functions, including complex functions facilitated by low power dissipation (particularly in MECL 10,000 series). A basic MECL 10,000 gate consumes less than 8 mW in on-chip power in some complex functions.

Wide Performance Flexibility due to differential amplifier design which permits MECL circuits to be used as linear as well as digital circuits.

Transmission Line Drive Capability is afforded by the open emitter outputs of MECL devices. No "Line Drivers" are listed in MECL families, because *every* device is a line driver.

Wire-ORing reduces the number of logic devices required in a design by producing additional OR gate functions with only an interconnection.

Twisted Pair Drive Capability permits MECL circuits to drive twisted-pair transmission lines as long as 1000 feet.

Wire-Wrap Capability is possible with MECL 10,000 and the M10800 LSI family because of the slow rise and fall time characteristic of the circuits.

Open Emitter-Follower Outputs are used for MECL outputs to simplify signal line drive. The outputs match any line impedance and the absence of internal pulldown resistors saves power.

Input Pulldown Resistors of approximately 50 kΩ permit unused inputs to remain unconnected for easier circuit board layout.

MECL APPLICATIONS

Motorola's MECL product lines are designed for a wide range of systems needs. Within the computer market, MECL 10,000 is used in systems ranging from special purpose peripheral controllers to large mainframe computers. Big growth areas in this market include disk and communication channel controllers for larger systems and high performance minicomputers.

The industrial market primarily uses MECL for high performance test systems such as IC or PC board testers. However, the high bandwidths of MECL 10,000, MECL III, and MC12,000 are required for many frequency synthesizer systems using high speed phase lock loop networks. MECL will continue to grow in the industrial market through complex medical electronic products and high performance process control systems.

MECL 10,000 and MECL III have been accepted within the Federal market for numerous signal processors and navigation systems. Full military temperature range MECL 10,000 is offered in the MC10500 and MC10600 Series, and in the PLL family as the MC12500 Series.

BASIC CONSIDERATIONS FOR HIGH-SPEED LOGIC DESIGN

High-speed operation involves only four considerations that differ significantly from operation at low and medium speeds:

1. Time delays through interconnect wiring, which may have been ignored in medium-speed systems, become highly important at state-of-the-art speeds.

2. The possibility of distorted waveforms due to reflections on signal lines increases with edge speed.

3. The possibility of "crosstalk" between adjacent signal leads is proportionately increased in high-speed systems.

4. Electrical noise generation and pick-up are more detrimental at higher speeds.

In general, these four characteristics are speed- and frequency-dependent, and are virtually independent of the type of logic employed. The merit of a particular logic family is measured by how well it compensates for these deleterious effects in system applications.

The interconnect-wiring time delays can be reduced only by reducing the length of the interconnecting lines. At logic speeds of two nanoseconds, an equivalent "gate delay" is introduced by every foot of interconnecting wiring. Obviously, for functions interconnected within a single monolithic chip, the time delays of signals travelling from one function to another are insignificant. But for a great many externally interconnected parts, this can soon add up to an appreciable delay time. Hence, the greater the number of functions per chip, the higher the system speed. *MECL circuits, particularly those of the MECL 10,000 Series are designed with a propensity toward complex functions to enhance overall system speed.*

Waveform distortion due to line reflections also becomes troublesome principally at state-of-the-art speeds. At slow and medium speeds, reflections on interconnecting lines are not usually a serious problem. At higher speeds, however, line lengths can approach the wavelength of the signal and improperly terminated lines can result in reflections that will cause false triggering (see Figure 2). The solution, as in RF technology, is to employ "transmission-line" practices and properly terminate each signal line with its characteristic impedance at the end of its run. *The low-impedance, emitter-follower outputs of MECL circuits facilitate transmission-line practices without upsetting the voltage levels of the system.*

The increased affinity for crosstalk in high-speed circuits is the result of very steep leading and trailing edges (fast rise and fall times) of the high-speed signal. These steep wavefronts are rich in harmonics that couple readily to adjacent circuits. *In the design of MECL 10,000, the rise and fall times have been deliberately slowed. This reduces the affinity for crosstalk without compromising other important performance parameters.*

From the above, it is evident that the MECL logic line is not simply capable of operating at high speed, but has been specifically designed to reduce the problems that are normally associated with high-speed operation.

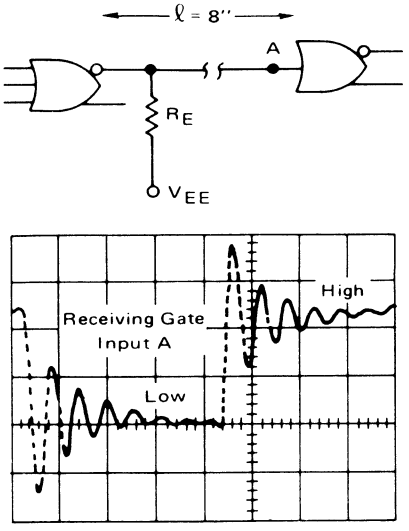


FIGURE 2a – UNTERMINATED TRANSMISSION LINE (No Ground Plane Used)

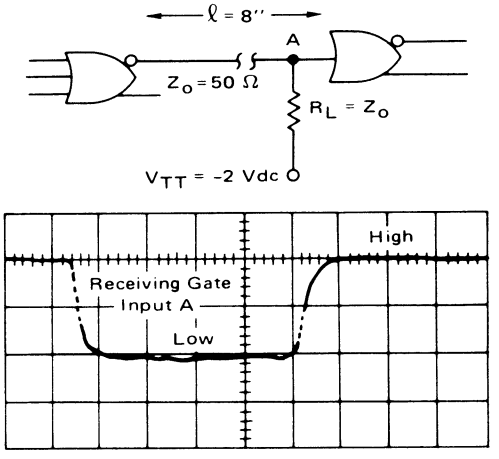


FIGURE 2b – PROPERLY TERMINATED TRANSMISSION LINE (Ground Plane Added)

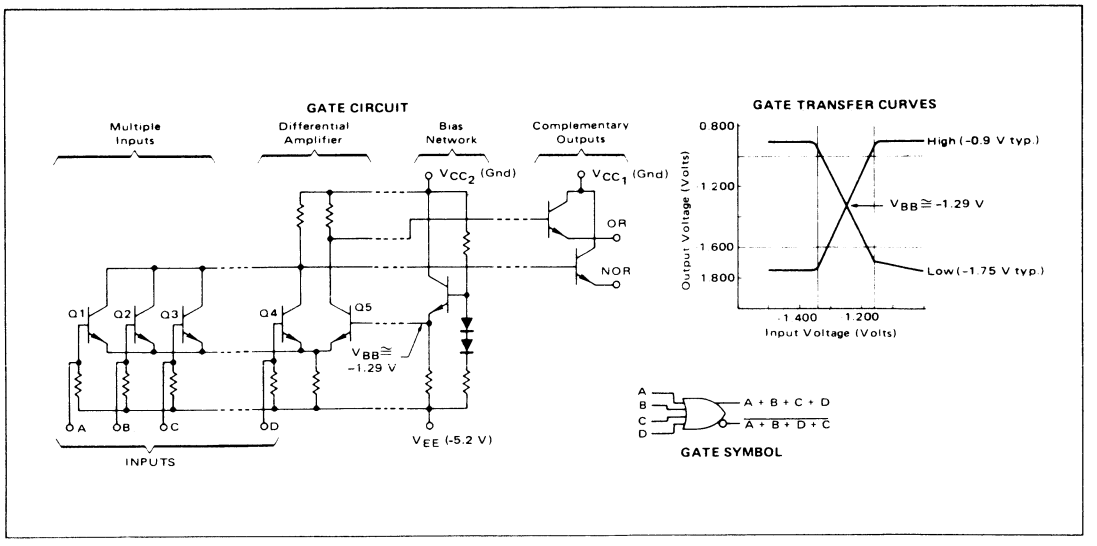


FIGURE 3 – MECL GATE STRUCTURE AND SWITCHING BEHAVIOR

CIRCUIT DESCRIPTION

The typical MECL circuit, Figure 3, consists of a differential-amplifier input circuit, a temperature and voltage compensated bias network, and emitter-follower outputs to restore dc levels and provide buffering for transmission line driving. High fan-out operation is possible because of the high input impedance of the differential amplifier input and the low output impedance of the emitter follower outputs. Power-supply noise is virtually eliminated by the nearly constant current drain of the differential amplifier, even during the transition period. Basic gate design provides for simultaneous output of both the OR function and its complement, the NOR function.

Power-Supply Connections Any of the power supply levels, V_{TT}, V_{CC}, or V_{EE} may be used as ground; however, the use of the V_{CC} node as ground results in best noise immunity. In such a case: V_{CC} = 0, V_{TT} = -2.0 V, V_{EE} = -5.2 V.

System Logic Specifications — The output logic swing of 0.85 V, as shown by the typical transfer characteristics curve, varies from a LOW state of V_{OL} = -1.75 V to a HIGH state of V_{OH} = -0.9 V with respect to ground.

Positive logic is used when reference is made to logical "0's" or "1's." Then

"0" = -1.75 V = LOW
typical
"1" = -0.9 V = HIGH

Circuit Operation -- Beginning with all logic inputs LOW (nominal -1.75 V), assume that Q1 through Q4 are cut off because their P-N base-emitter junctions are not conducting, and the forward-biased Q5 is conducting. Under these conditions, with the base of Q5 held at -1.29 V by the V_{BB} network, its emitter will be one diode drop (0.8 V) more negative than its base, or -2.09 V. (The 0.8 V differential is a characteristic of this P-N junction.) The base-to-emitter differential across Q1 – Q4 is then the difference between the common emitter voltage (-2.09 V) and the LOW logic level (-1.75 V) or 0.34 V. This is less than the threshold voltage of Q1 through Q4 so that these transistors will remain cut off.

When any one (or all) of the logic inputs are shifted upward from the -1.75 V LOW state to the -0.9 V HIGH state, the base voltage of that transistor increases beyond the threshold point and the transistor turns on. When this happens, the voltage at the common-emitter point rises from -2.09 V to -1.7 (one diode drop below the -0.9 V base voltage of the input transistor), and since the base voltage of the fixed-bias transistor (Q5) is held at -1.29 V, the base-emitter voltage Q5 cannot sustain conduction. Hence, this transistor is cut off.

This action is reversible, so that when the input signal(s) return to the LOW state, Q1 – Q4 are again turned off and Q5 again becomes forward biased. The collector voltages resulting from the switching action of Q1 – Q4 and Q5 are transferred through the output emitter-follower to the output terminal. Note that the differential action of the switching transistors (one section being off when the other is on) furnishes simultaneous complementary signals at the output. This action also maintains constant power supply current drain.

DEFINITIONS OF LETTER SYMBOLS AND ABBREVIATIONS

Current:

I_{CC}	Total power supply current drawn from the positive supply by a MECL unit under test.
I_{CBO}	Leakage current from input transistor on MECL devices without pulldown resistors when test voltage is applied.
I_{CCH}	Current drain from V_{CC} power supply with all inputs at logic HIGH level.
I_{CCL}	Current drain from V_{CC} power supply with all inputs at logic LOW level.
I_E	Total power supply current drawn from a MECL test unit by the negative power supply.
I_F	Forward diode current drawn from an input of a saturated logic-to-MECL translator when that input is at ground potential.
I_{in}	Current into the input of the test unit when a maximum logic HIGH ($V_{IH\ max}$) is applied at that input.
$*I_{INH}$	HIGH level input current into a node with a specified HIGH level ($V_{IH\ max}$) logic voltage applied to that node. (Same as I_{in} for positive logic.)
$*I_{INL}$	LOW level input current, into a node with a specified LOW level ($V_{IL\ min}$) logic voltage applied to that node.
I_L	Load current that is drawn from a MECL circuit output when measuring the output HIGH level voltage.
$*I_{OH}$	HIGH level output current: the current flowing into the output, at a specified HIGH level output voltage.
$*I_{OL}$	LOW level output current: the current flowing into the output, at a specified LOW level output voltage.
I_{OS}	Output short circuit current.
I_{out}	Output current (from a device or circuit, under such conditions mentioned in context).

Current (cont.) :

I_R Reverse current drawn from a transistor input of a test unit when V_{EE} is applied at that input.

I_{SC} Short-circuit current drawn from a translator saturating output when that output is at ground potential.

Voltage:

V_{BB} Reference bias supply voltage.

V_{BE} Base-to-emitter voltage drop of a transistor at specified collector and base currents.

V_{CB} Collector-to-base voltage drop of a transistor at specified collector and base currents.

V_{CC} General term for the most positive power supply voltage to a MECL device (usually ground, except for translator and interface circuits).

V_{CC1} Most positive power supply voltage (output devices). (Usually ground for MECL devices.)

V_{CC2} Most positive power supply voltage (current switches and bias driver). (Usually ground for MECL devices.)

V_{EE} Most negative power supply voltage for a circuit (usually -5.2 V for MECL devices).

V_F Input voltage for measuring I_F on TTL interface circuits.

V_{IH} Input logic HIGH voltage level (nominal value).

*$V_{IH\ max}$ Maximum HIGH level input voltage: The most positive (least negative) value of high-level input voltage, for which operation of the logic element within specification limits is guaranteed.

V_{IHA} Input logic HIGH threshold voltage level.

$V_{IHA\ min}$ Minimum input logic HIGH level (threshold) voltage for which performance is specified.

*$V_{IH\ min}$ Minimum HIGH level input voltage: The least positive (most negative) value of HIGH level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{IL} Input logic LOW voltage level (nominal value).

*$V_{IL\ max}$ Maximum LOW level input voltage: The most positive (least negative) value of LOW level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{ILA} Input logic LOW threshold voltage level.

$V_{ILA\ max}$ Maximum input logic LOW level (threshold) voltage for which performance is specified.

*$V_{IL\ min}$ Minimum LOW level input voltage: The least positive (most negative) value of LOW level input voltage for which operation of the logic element within specification limits is guaranteed.

V_{in} Input voltage (to a circuit or device).

V_{max} Maximum (most positive) supply voltage, permitted under a specified set of conditions.

*V_{OH} Output logic HIGH voltage level: The voltage level at an output terminal for a specified output current, with the specified conditions applied to establish a HIGH level at the output.

V_{OHA} Output logic HIGH threshold voltage level.

$V_{OHA\ min}$ Minimum output HIGH threshold voltage level for which performance is specified.

$V_{OH\ max}$ Maximum output HIGH or high-level voltage for given inputs.

$V_{OH\ min}$ Minimum output HIGH or high-level voltage for given inputs.

*V_{OL} Output logic LOW voltage level: The voltage level at the output terminal for a specified output current, with the specified conditions applied to establish a LOW level at the output.

V_{OLA} Output logic LOW threshold voltage level.

$V_{OLA\ max}$ Maximum output LOW threshold voltage level for which performance is specified.

$V_{OL\ max}$ Maximum output LOW level voltage for given inputs.

$V_{OL\ min}$ Minimum output LOW level voltage for given inputs.

V_{TT} Line load-resistor terminating voltage for outputs from a MECL device.

V_{OLS1} Output logic LOW level on MECL 10,000 line receiver devices with all inputs at V_{EE} voltage level.

V_{OLS2} Output logic LOW level on MECL 10,000 line receiver devices with all inputs open.

*JEDEC, EIA, NEMA standard definition

Time Parameters:

$t+$	Waveform rise time (LOW to HIGH), 10% to 90%, or 20% to 80%, as specified.
$t-$	Waveform fall time (HIGH to LOW), 90% to 10%, or 80% to 20%, as specified.
t_r	Same as t+
t_f	Same as t-
$t+-$	Propagation Delay, see Figure 9.
$t-+$	Propagation Delay, see Figure 9.
t_{pd}	Propagation delay, input to output from the 50% point of the input waveform at pin x (falling edge noted by – or rising edge noted by +) to the 50% point of the output waveform at pin y (falling edge noted by – or rising edge noted by +). (Cf Figure 9.)
$t_{x\pm y\pm}$	
t_{x+}	Output waveform rise time as measured from 10% to 90% or 20% to 80% points on waveform (whichever is specified) at pin x with input conditions as specified.
t_{x-}	Output waveform fall time as measured from 90% to 10% or 80% to 20% points on waveform (whichever is specified) at pin x, with input conditions as specified.
f_{Tog}	Toggle frequency of a flip-flop or counter device.
f_{shift}	Shift rate for a shift register.

Read Mode (Memories)

t_{ACS}	Chip Select Access Time
t_{RCS}	Chip Select Recovery Time
t_{AA}	Address Access Time

Write Mode (Memories)

t_W	Write Pulse Width
t_{WSD}	Data Setup Time Prior to Write
t_{WHD}	Data Hold Time After Write
t_{WSA}	Address setup time prior to write
t_{WHA}	Address hold time after write
t_{WSCS}	Chip select setup time prior to write
t_{WHCS}	Chip select hold time after write
t_{WS}	Write disable time
t_{WR}	Write recovery time

Temperature:

T_{stg}	Maximum temperature at which device may be stored without damage or performance degradation.
T_J	Junction (or die) temperature of an integrated circuit device.
T_A	Ambient (environment) temperature existing in the immediate vicinity of an integrated circuit device package.
θ_{JA}	Thermal resistance of an IC package, junction to ambient.
θ_{JC}	Thermal resistance of an IC package, junction to case.
lfpm	Linear feet per minute.
θ_{CA}	Thermal resistance of an IC package, case to ambient.

Miscellaneous:

e_g	Signal generator inputs to a test circuit.
TP_{in}	Test point at input of unit under test.
TP_{out}	Test point at output of unit under test.
D.U.T.	Device under test.
C_{in}	Input capacitance.
C_{out}	Output capacitance.
Z_{out}	Output impedance.
$^*P_D$	The total dc power applied to a device, not including any power delivered from the device to a load.
R_L	Load Resistance.
R_T	Terminating (load) resistor.
R_p	An input pull-down resistor (i.e., connected to the most negative voltage).
P.U.T.	Pin under test.

*JEDEC, EIA, NEMA standard definition

SECTION II — TECHNICAL DATA

GENERAL CHARACTERISTICS and SPECIFICATIONS

(See pages 1-6 through 1-8 for definitions of symbols and abbreviations.)

In subsequent sections of this Data Book, the important MECL parameters are identified and characterized, and complete data provided for each of the functions. To make this data as useful as possible, and to avoid a great deal of repetition, the data that is common to all functional blocks in a line is not repeated on each individual sheet. Rather, these common characteristics, as well as the application information that applies to each family, are discussed in this section.

In general, the common characteristics of major importance are:

Maximum Ratings, including both dc and ac characteristics and temperature limits;

Transfer Characteristics, which define logic levels and switching thresholds;

DC Parameters, such as output levels, threshold levels, and forcing functions.

AC Parameters, such as propagation delays, rise and fall times and other time dependent characteristics.

In addition, this section will discuss general layout and design guides that will help the designer in building and testing systems with MECL circuits.

LETTER SYMBOLS AND ABBREVIATIONS

Throughout this section, and in the subsequent data sheets, letter symbols and abbreviations will be used in discussing electrical characteristics and specifications. The symbols used in this book, and their definitions, are listed on the preceding pages.

MAXIMUM RATINGS

The limit parameters beyond which the life of the devices may be impaired are given in Figure 4a. In addition, Table 4b provides certain limits which, if exceeded, will not damage the devices, but could degrade the performance below that of the guaranteed specifications.

MECL TRANSFER CURVES

For MECL logic gates, the dual (complementary) outputs must be represented by two transfer curves: one to describe the OR switching action and one to describe the NOR switching action. A typical transfer curve and associated data for all MECL families is shown in Figure 5.

It is not necessary to measure transfer curves at all points of the curves. To guarantee correct operation it is sufficient merely to measure two sets of min/max logic level parameters.

FIGURE 4a — LIMITS BEYOND WHICH DEVICE LIFE MAY BE IMPAIRED

Characteristic	Symbol	Unit	MECL 10,000	M10800 LSI	MECL III
Characteristic	V_{EE}	Vdc	-8.0 to 0	-8.0 to 0	-8.0 to 0
Supply Voltage (V_{CC} = 0)	V_{TT}	Vdc	–	-4.0 to 0	–
Input Voltage (V_{CC} = 0)	V_{in}	Vdc	0 to V_{EE}	0 to V_{EE}	0 to V_{EE}
Input Voltage Bus (V_{CC} = 0)	V_{in}	Vdc	–	0 to -2.0①	–
Output Source Current Continuous	I_{out}	mAdc	50	50	40
Output Source Current Surge	I_{out}	mAdc	100	100	–
Storage Temperature	T_{stg}	°C	-55 to +150	-55 to +150	-55 to +150
Junction Temperature Ceramic Package②	T_J	°C	165	165	165③
Junction Temperature Plastic Package	T_J	°C	150	–	150

NOTES: ① Input voltage limit is V_{CC} to -2 volts when bus is used as an input and the output drivers are disabled.

② Maximum T_J may be exceeded ($\leq 250^{\circ}C$) for short periods of time ($\leq$ 240 hours) without significant reduction in device life.

③ Except MC1666 – MC1670 which have maximum junction temperatures = 145°C.

FIGURE 4b – LIMITS BEYOND WHICH PERFORMANCE MAY BE DEGRADED

Characteristics	Symbol	Unit	MECL 10,000	M10800 LSI	MECL III
Operating Temperature Range Commercial ①	T_A	°C	MC: −30 to +85 MCM: 0 to 75	−30 to +85	−30 to +85
Operating Temperature Range MIL ①	T_A	°C	−55 to +125	—	−55 to +125 (MC1648M)
Supply Voltage (V_{CC} = 0)②	V_{EE}	Vdc	MC: −4.68 to −5.72 MCM: −4.94 to −5.46	−4.68 to −5.72	−4.68 to −5.72
Supply Voltage (V_{CC} = 0)	V_{TT}	Vdc	—	−1.9 to −2.2	—
Output Drive Commercial	—	Ω	50 Ω to −2.0 Vdc	50 Ω to −2.0 Vdc	50 Ω to −2.0 Vdc④
Output Drive MIL	—	Ω	100 Ω to −2.0 Vdc	100 Ω to −2.0 Vdc	—
Maximum Clock Input Rise and Fall Time (20% to 80%)	t_r, t_f	ns	—	10	③

NOTES: ①With airflow ≥ 500 lfpm.

②Functionality only. Data sheet limits are specified for −5.2 V ± 0.010 V.

③10 ns maximum limit for MC1690, MC1697, and MC1699.

④ Except MC1648 which has an internal output pulldown resistor.

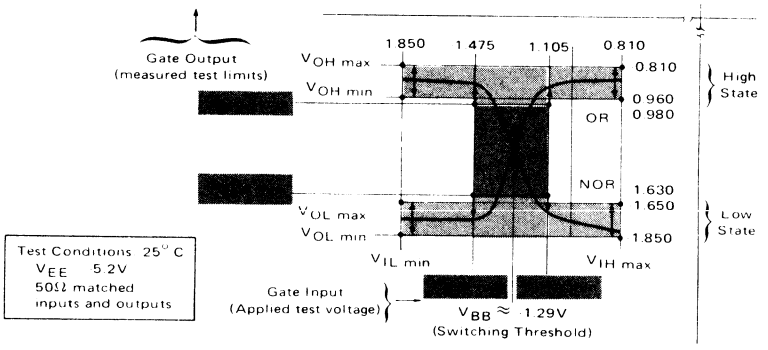


FIGURE 5 – MECL TRANSFER CURVES (MECL 10,000 EXAMPLE) and SPECIFICATION TEST POINTS

The first set is obtained by applying test voltages, V_{IL} min and V_{IH} max (sequentially) to the gate inputs, and measuring the OR and NOR output levels to make sure they are between V_{OL} max and V_{OL} min, and V_{OH}max and V_{OH}min specifications.

The second set of logic level parameters relates to the switching thresholds. This set of data is distinguished by an "A" in symbol subscripts. A test voltage, V_{ILA} max, is applied to the gate and the NOR and OR outputs are measured to see that they are above the V_{OHA} min and below the V_{OLA} max levels, respectively. Similar checks are made using the test input voltage V_{IHA} min.

The result of these specifications insures that:

a) The switching threshold (≈ V_{BB}) falls within the darkest rectangle; i.e. switching does not begin outside this rectangle;

b) Quiescent logic levels fall in the lightest shaded ranges;

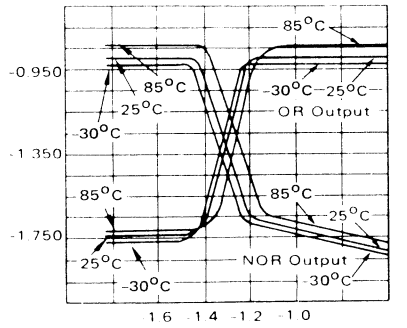
c) Guaranteed noise immunity is met.

Figure 6 shows the guaranteed MECL 10,000 and MECL III logic levels and switching thresholds over specified temperature ranges. As shown in the Figure 6a Typical Transfer Curves, MECL outputs rise with increasing ambient temperature. All circuits in each family have the same worst-case output level specifications regardless of power dissipation or junction temperature differences to reduce loss of noise margin due to thermal differences.

All of these specifications assume −5.2 V power supply operation. Operation at other power-supply voltages is possible, but will result in further transfer curve changes. Transfer characteristic data obtained for a variety of supply voltages are shown in Figure 7. The table accompanying these graphs indicates the change rates of output voltages as a function of power supply voltages.

TRANSFER DATA FOR TEMPERATURE VARIATIONS

FIGURE 6a – TYPICAL TRANSFER CHARACTERISTICS AS A FUNCTION OF TEMPERATURE
(See tables below for data)



Forcing Function	Parameter	−55°C①	−30°C②	0°C③	25°C②	25°C①	75°C③	85°C②	125°C①
		MC10500 MC10600 MCM10500	MC10100 MC10200 MC10800	MCM10100	MC10100 MC10200 MC10800	MC10500 MC10600 MCM10500	MCM10100	MC10100 MC10200 MC10800	MC10500 MC10600 MCM10500
V_{IHmax} =	V_{OHmax}	−0.880	−0.890	−0.840	−0.810	−0.780	−0.720	−0.700	−0.630
	V_{OHmin}	−1.080	−1.060	−1.000	−0.960	−0.930	−0.900	−0.890	−0.825
	V_{OHAmin}	−1.100	−1.080	−1.020	−0.980	−0.950	−0.920	−0.910	−0.845
V_{IHAmin}		−1.255	−1.205	−1.145	−1.105	−1.105	−1.045	−1.035	−1.000
V_{ILAmax}		−1.510	−1.500	−1.490	−1.475	−1.475	−1.450	−1.440	−1.400
	V_{OLAmax}	−1.635	−1.655	−1.645	−1.630	−1.600	−1.605	−1.595	−1.525
	V_{OLmax}	−1.655	−1.675	−1.665	−1.650	−1.620	−1.625	−1.615	−1.545
V_{ILmin} =	V_{OLmin}④	−1.920	−1.890	−1.870	−1.850	−1.850	−1.830	−1.825	−1.820
V_{ILmin}	I_{INLmin}	0.5	0.5	0.5	0.5	0.5	0.3	0.3	0.3

NOTES: ① MC10500, MC10600, and MCM10500 series specified driving 100 Ω to −2.0 V.
② MC10100, MC10200, and MC10800 series specified driving 50 Ω to −2.0 V.
③ Memories (MCM10100) specified 0–75°C for commercial temperature range, 50 Ω to −2.0 V. Military temperature range memories (MCM10500) specified per Note 1.
④ Special circuits such as MC10123, MC10118, MC10119, and MC10800 family bus outputs have lower than normal V_{OLmin}. See individual data sheets for specific values.

Each MECL 10,000 series device has been designed to meet the dc specifications shown in the test table, after thermal equilibirum has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 linear fpm is maintained. V_{EE} = −5.2 V ± 0.010 V.

FIGURE 6b – MECL 10,000 DC TEST PARAMETERS

Forcing Function	Parameter	−30°C	25°C	85°C
V_{IHmax} =	V_{OHmax}	−0.875	−0.810	−0.700
	V_{OHmin}	−1.045	−0.960	−0.890
	V_{OHAmin}	−1.065	−0.980	−0.910
V_{IHAmin}		−1.180	−1.095	−1.025
V_{ILAmax}		−1.515	−1.485	−1.440
	V_{OLAmax}	−1.630	−1.600	−1.555
	V_{OLmax}	−1.650	−1.620	−1.575
V_{ILmin} =	V_{OLmin}	−1.890	−1.850	−1.830
V_{ILmin}	I_{INLmin}	0.5	0.5	0.3

NOTE: All outputs loaded 50 Ω to −2.0 Vdc except MC1648 which has an internal output pulldown resistor.

ELECTRICAL CHARACTERISTICS
Each MECL III series device has been designed to meet the dc specifi cation shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 linear fpm is maintained. V_{EE} = −5.2 V ± 0.10 V.

FIGURE 6c – MECL III DC TEST PARAMETERS

TRANSFER DATA FOR POWER SUPPLY VARIATIONS

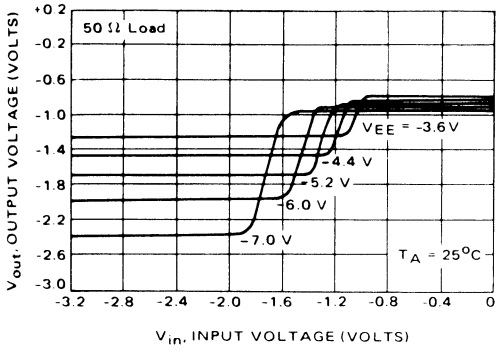


FIGURE 7a – MECL III/10,000 "OR"

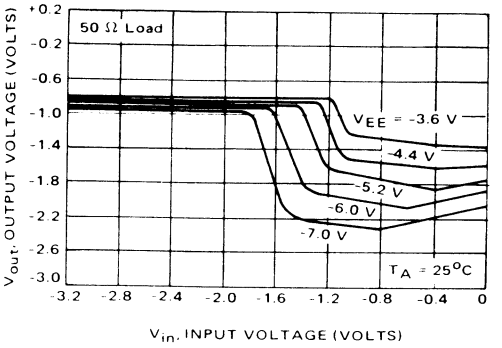
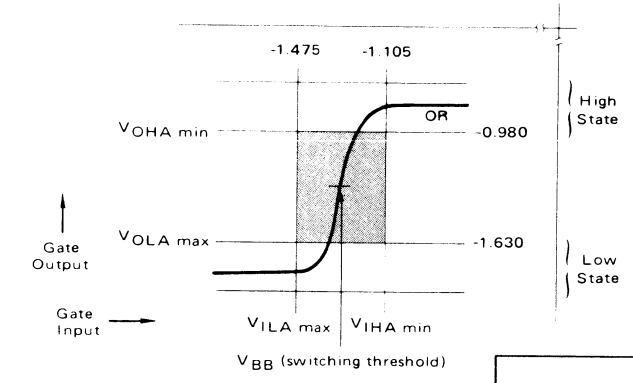


FIGURE 7b – MECL III/10,000 "NOR"

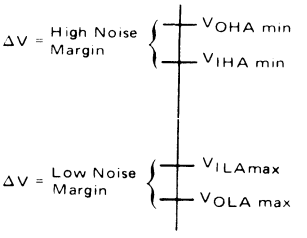
Voltage	MECL 10,000*	MECL III	M10800 LSI
$\Delta V_{OH}/\Delta V_{EE}$	0.016	0.033	0.016
$\Delta V_{OL}/\Delta V_{EE}$	0.250	0.270	0.030
$\Delta V_{BB}/\Delta V_{EE}$	0.148	0.140	0.015

*and subsets: 10,200; 10,500; 10,600.

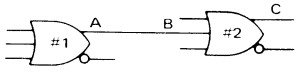
FIGURE 7C – TYPICAL LEVEL CHANGE RATES



Specification Points for Determining Noise Margin



Noise Margin Computations



Family	Guaranteed Worst-Case dc Noise Margin	Typical dc Noise Margin
All MECL 10,000	0.125	0.210
MECL III	0.115	0.200

FIGURE 8 – MECL Noise Margin Data

NOISE MARGIN

"Noise margin" is a measure of a logic circuit's resistance to undesired switching. MECL noise margin is defined in terms of the specification points surrounding the switching threshold. The critical parameters of interest here are those designated with the "A" subscript ($V_{OHA\ min}$, $V_{OLA\ max}$, $V_{IHA\ min}$, $V_{ILA\ max}$) in the transfer characteristic curves.

Guaranteed noise margin (NM) is defined as follows:

$$NM_{HIGH\ LEVEL} = V_{OHA\ min} - V_{IHA\ min}$$

$$NM_{LOW\ LEVEL} = V_{ILA\ max} - V_{OLA\ max}$$

To see how noise margin is computed, assume a MECL gate drives a similar MECL gate, Figure 8.

At a gate input (point B) equal to $V_{ILA\ max}$, MECL gate #2 can begin to enter the shaded transition region.

This is a "worst case" condition, since the $V_{OLA\ max}$ specification point guarantees that no device can enter the transition region before an input equal to $V_{ILA\ max}$ is reached. Clearly then, $V_{ILA\ max}$ is one critical point for noise margin computation, since it is the edge of the transition region.

To find the other critical voltage, consider the output from MECL gate #1 (point A). What is the most positive value possible for this voltage (considering worst case specifications)? From Figure 8 it can be observed that the $V_{OLA\ max}$ specification insures that the LOW state OR output from gate #1 can be no greater than $V_{OLA\ max}$.

Note that $V_{OLA\ max}$ is more negative than $V_{ILA\ max}$. Thus, with $V_{OLA\ max}$ at the input to gate #2, the transition region is not yet reached. (The input voltage to gate #2 is still to the left of $V_{ILA\ max}$ on the transfer curve.)

In order to ever run the chance of switching gate #2, we would need an additional voltage, to move the input from $V_{OLA\ max}$ to $V_{ILA\ max}$. This constitutes the "safety factor" known as noise margin. It can be calculated as the magnitude of the difference between the two specification voltages, or for the MECL 10,000 levels shown:

$$NM_{LOW} = V_{ILA\ max} - V_{OLA\ max}$$
$$= -1.475\ V - (-1.630\ V)$$
$$= 155\ mV.$$

Similarly, for the HIGH state:

$$NM_{HIGH} = V_{OHA\ min} - V_{IHA\ min}$$
$$= -0.980\ V - (-1.105\ V)$$
$$= 125\ mV$$

Analogous results are obtained when considering the "NOR" transfer data.

Note that these noise margins are absolute worst case conditions. The lesser of the two noise margins is that for the HIGH state, 125 mV. This then, constitutes the guaranteed margin against signal undershoot, and power or thermal disturbances.

As shown in the table, typical noise margins are usually better than guaranteed – by about 75 mV.

Noise margin is a dc specification that can be calculated, since it is defined by specification points tabulated on MECL data sheets. However, by itself, this specification does not give a complete picture regarding the noise immunity of a system built with a particular set of circuits. Overall system noise immunity involves not only noise-margin specifications, but also other circuit-related factors that determine how difficult it is to apply a noise signal of sufficient magnitude and duration to cause the circuit to propagate a false logic state. In general, then, noise immunity involves line impedances, circuit output impedances, and propagation delay in addition to noise-margin specifications. This subject is discussed in greater detail in Application Note AN-592.

AC OR SWITCHING PARAMETERS

Time-dependent specifications are those that define the effects of the circuit on a specified input signal, as it travels through the circuit. They include the time delay involved in changing the output level from one logic state to another. In addition, they include the time required for the output of a circuit to respond to the input signal, designated as propagation delay, or access time, in the case of memories. Since this terminology has varied over the years, and because the "conditions" associated with a particular parameter may differ among logic families, the common MECL waveform and propagation delay terminologies are depicted in Figure 9. Specific rise, fall, and propagation delay times are given on the data sheet for each specific functional block, but like the transfer characteristics, ac parameters are temperature and voltage dependent. Typical variations for MECL 10,000 are given in the curves of Figure 10.

SETUP AND HOLD TIMES

Setup and hold times are two ac parameters which can easily be confused unless clearly defined. For MECL logic devices, t_{setup} is the minimum time (50% – 50%) before the positive transition of the clock pulse (C) that information must be pres-

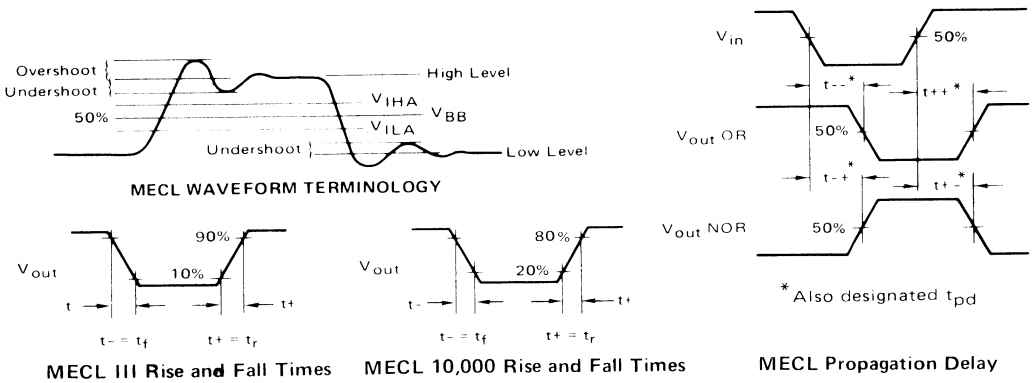


FIGURE 9a – TYPICAL LOGIC WAVEFORMS

FIGURE 9b – MEMORY CHIP SELECT ACCESS TIME WAVEFORM

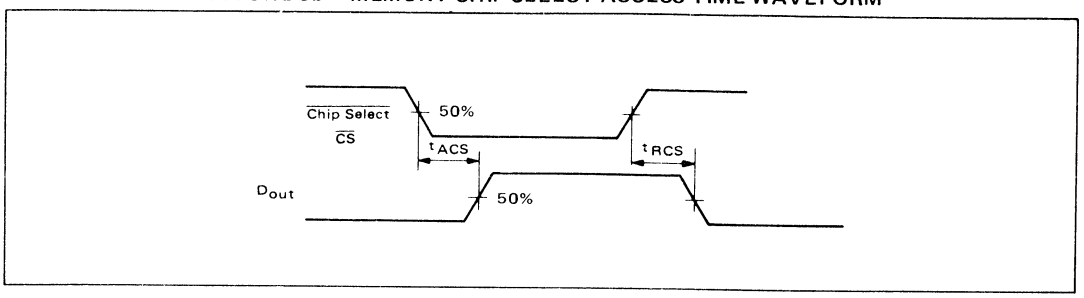
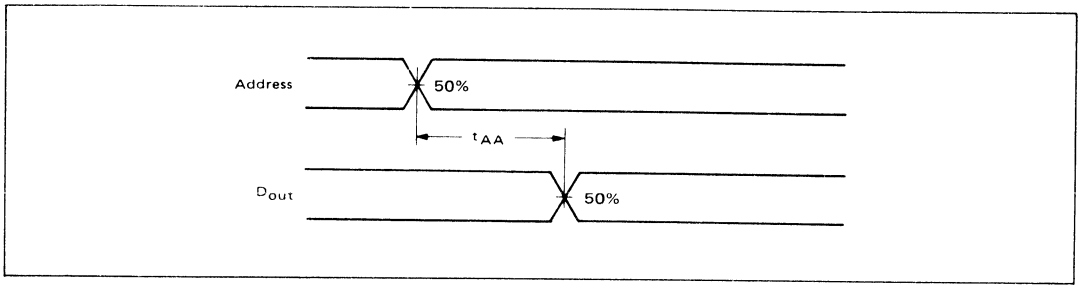


FIGURE 9c – MEMORY ADDRESS ACCESS TIME WAVEFORM



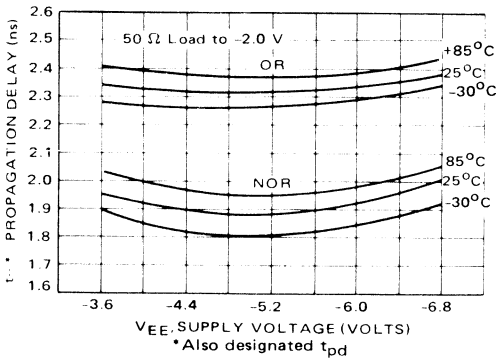


FIGURE 10a – TYPICAL PROPAGATION DELAY t-- versus V_{EE} AND TEMPERATURE (MECL 10,000)

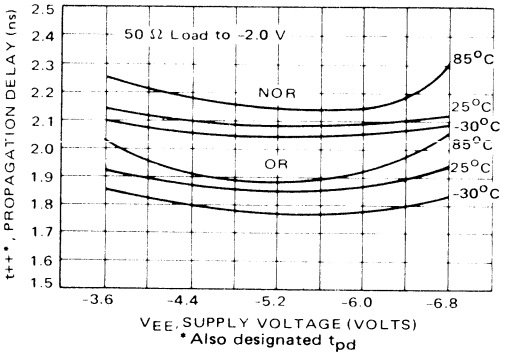


FIGURE 10b – TYPICAL PROPAGATION DELAY t++ versus V_{EE} AND TEMPERATURE (MECL 10,000)

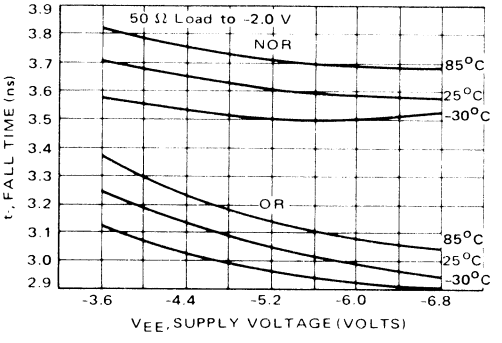


FIGURE 10c – TYPICAL FALL TIME (90% to 10%) versus TEMPERATURE AND SUPPLY VOLTAGE (MECL 10,100)

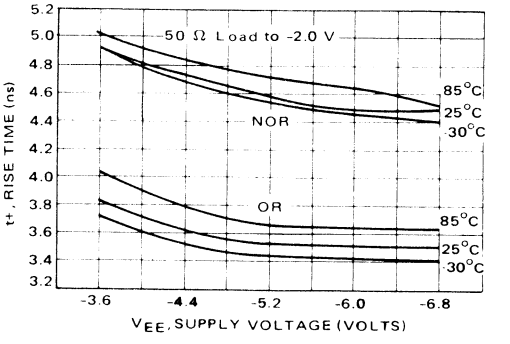


FIGURE 10d – TYPICAL RISE TIME (10% to 90%) versus TEMPERATURE AND SUPPLY VOLTAGE (MECL 10,100)

sent at the Data input (D) to insure proper operation of the device. The t_{hold} is defined similarly as the minimum time after the positive transition of the clock pulse (C) that the information must remain unchanged at the Data input (D) to insure proper operation. Setup and hold waveforms for logic devices are shown in Figure 11a.

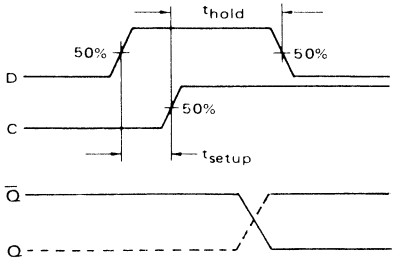


FIGURE 11a – SETUP AND HOLD WAVEFORMS FOR MECL LOGIC DEVICES

For MECL memory devices, t_{setup} is the minimum time before the negative transition of the write enable pulse ($\overline{WE}$) that information must be present at the chip select ($\overline{CS}$), Data (D), and address (A) inputs for proper writing of the selected cell. Similarly t_{hold} is the minimum time after the positive transition of the write enable pulse ($\overline{WE}$) that the information must remain unchanged at the inputs to insure proper writing. Memory setup and hold waveforms are shown in Figure 11b.

In specifying devices, Motorola establishes and guarantees values (shown as minimums on the data sheets) for t_{setup} and t_{hold}. For most MECL circuits, proper device operation typically occurs with the inputs present for somewhat less time than that specified for t_{setup} and t_{hold}.

TESTING MECL 10,000 and MECL III

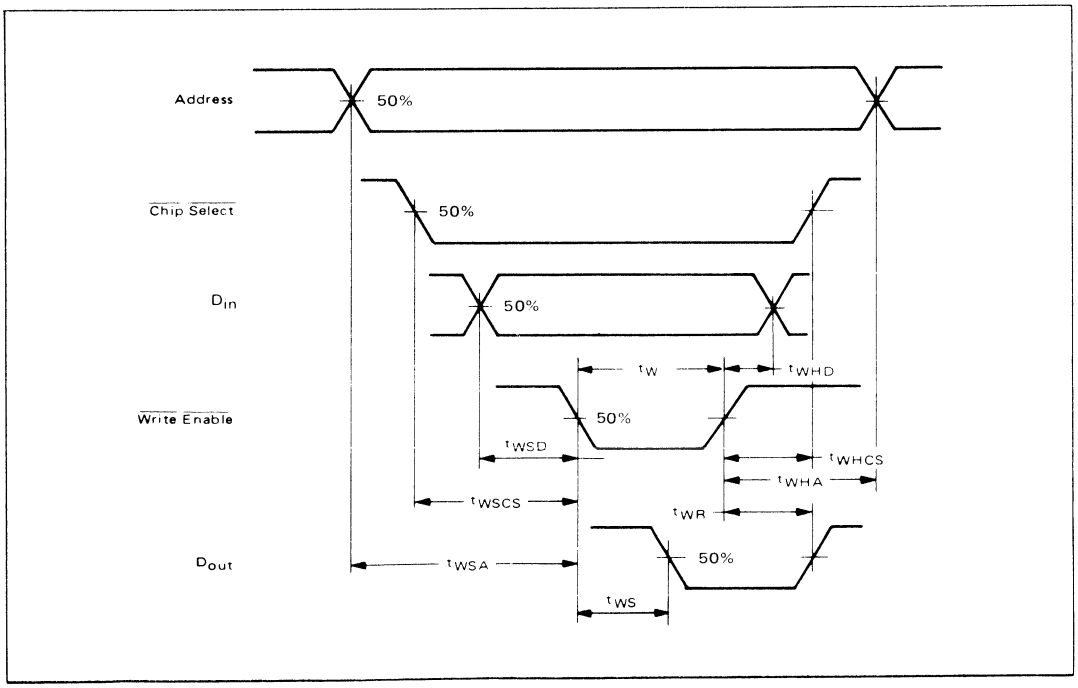
To obtain results correlating with Motorola circuit specifications certain test techniques must be used. A schematic of a typical gate test circuit is shown in Figure 12a, and a typical memory test circuit in Figure 12b.

A solid ground plane is used in the test setup, and capacitors bypass V_{CC1}, V_{CC2}, and V_{EE} pins to ground. All power leads and signal leads are kept as short as possible.

The sampling scope interface runs directly to the 50-ohm inputs of Channel A and B via 50-ohm coaxial cable. Equal-length coaxial cables must be used between the test set and the A and B scope inputs. A 50-ohm coax cable such as RG58/U or RG188A/U, is recommended.

Interconnect fittings should be 50 ohm GR, BNC, Sealectro Conhex, or equivalent. Wire length should be $< \frac{1}{4}$ inch from TP_{in} to input pin and TP_{out} to output pin.

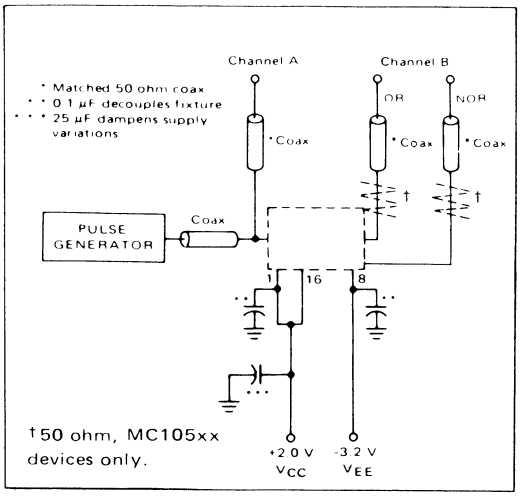
FIGURE 11b – SETUP AND HOLD WAVEFORMS FOR MECL MEMORIES (WRITE MODE)



The pulse generator must be capable of 2.0 ns rise and fall times for MECL 10,000 and 1.5 ns for MECL III. In addition, the generator voltage must have an offset to give MECL signal swings of ≈ ±400 mV about a threshold of ≈+0.7 V when V_{CC} = +2.0 V and V_{EE} = −3.2 V for ac testing of logic devices.

The power supplies are shifted +2.0 V, so that the device under test has only one resistor value to load into – the precision 50-ohm input impedance of the sampling oscilloscope. Use of this technique yields a close correlation between Motorola and customer testing. Unused outputs are loaded with a 50-ohm resistor (100-ohm for MIL temp devices) to ground. The positive supply (V_{CC}) should be decoupled from the test board by RF type 25 μF capacitors to ground. The V_{CC} pins are bypassed to ground with 0.1 μF, as is the V_{EE} pin.

Additional information on testing MECL 10,000 and understanding data sheets is found in Application Notes AN-579 and AN-701.



NOTE: All power supply levels are shown shifted 2 volts positive.

FIGURE 12a – MECL LOGIC SWITCHING TIME TEST SETUP

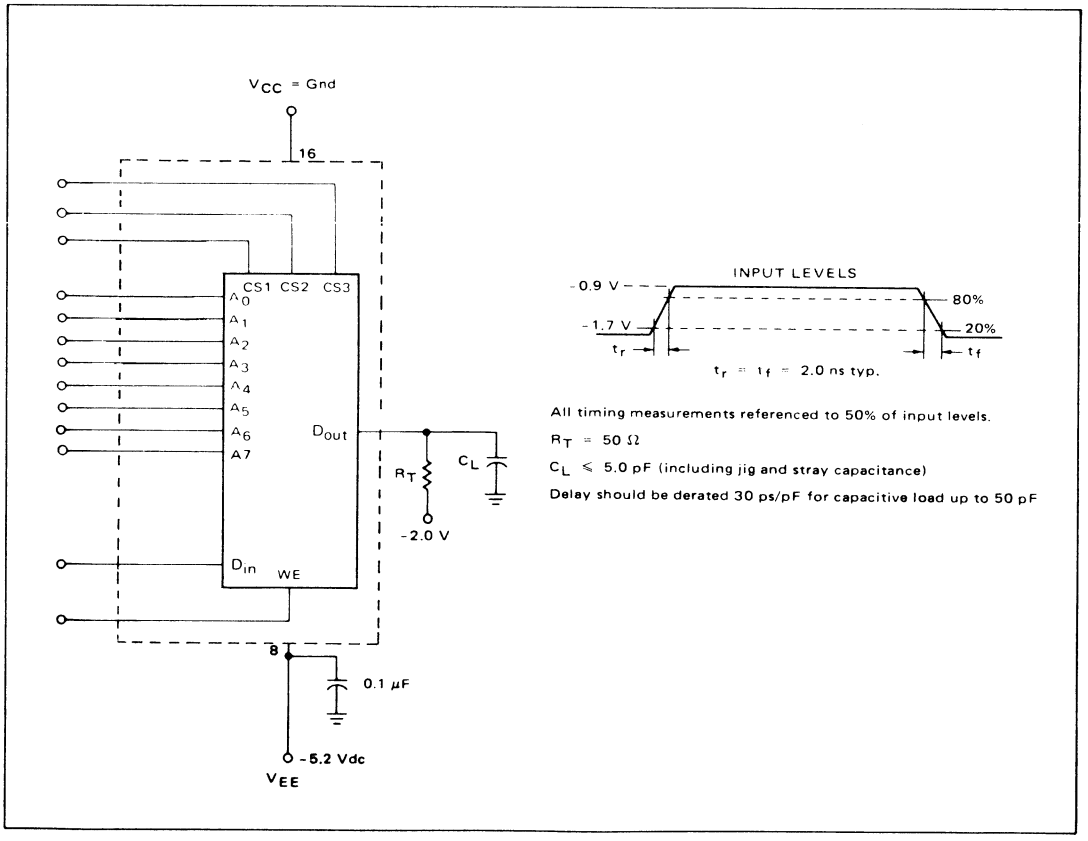


FIGURE 12b – MECL MEMORY SWITCHING TIME TEST CIRCUIT

POWER SUPPLY CONSIDERATIONS

MECL circuits are characterized with the V_{CC} point at ground potential and the V_{EE} point at −5.2 V. While this MECL convention is not necessarily mandatory, it does result in maximum noise immunity. This is so because any noise induced on the V_{EE} line is applied to the circuit as a common-mode signal which is rejected by the differential action of the MECL input circuit. Noise induced into the V_{CC} line is not cancelled out in this fashion. Hence, a good system ground at the V_{CC} bus is required for best noise immunity.

Power supply regulation which will achieve 10% regulation or better at the device level is recommended. The −5.2 V power supply potential will result in best circuit speed. Other values for V_{EE} may be used. A more negative voltage will increase noise margins at a cost of increased power dissipation. A less negative voltage will have just the opposite effect.

On logic cards, a ground plane or ground bus system should be used. A bus system should be wide enough to prevent significant voltage drops between supply and device and to produce a low source inductance.

Although little power supply noise is generated by MECL logic, power supply bypass capacitors are recommended to handle switching currents caused by stray capacitance and asymmetric circuit loading. A parallel combination of a 1.0 μF and a 100 pF capacitor at the power entrance to the board, and a 0.01 μF low-inductance capacitor between ground and the −5.2 V line every four to six packages, are recommended.

Most MECL 10,000 and MECL III circuits have two V_{CC} leads. V_{CC1} supplies current to the output transistors and V_{CC2} is connected to the circuit logic transistors. The separate V_{CC} pins reduce cross-coupling between individual circuits within a package when the outputs are driving heavy loads. Circuits with large drive capability, similar to the MC10110, have two V_{CC1} pins. All V_{CC} pins should be connected to the ground plane or ground bus as close to the package as possible.

For further discussion of MECL power supply considerations to be made in system designing, see MECL System Design Handbook.

POWER DISSIPATION

The power dissipation of MECL functional blocks is specified on their respective data sheets. This specification does not include power dissipated in the output devices due to output termination. The omission of internal output pull-down resistors permits the use of external terminations designed to yield best system performance. To obtain total operating power dissipation of a particular functional block in a system, the dissipation of the output transistor, under load, must be added to the circuit power dissipation.

The table in Figure 13 lists the power dissipation in the output transistors plus that in the external terminating resistors, for the more commonly used termination values and circuit configurations. To obtain true package power dissipation, one output-transistor power-dissipation value must be added to the specified package power dissipation for each external termination resistor used in conjunction with that package. To obtain system power dissipation, the stated dissipation in the external terminating resistors must be added as well. Unused outputs draw no power and may be ignored.

Terminating Resistor Value	Output Transistor Power Dissipation (mW)	Terminating Resistor Power Dissipation (mW)
150 ohms to -2.0 Vdc	5.0	4.3
100 ohms to -2.0 Vdc	7.5	6.5
75 ohms to -2.0 Vdc	10	8.7
50 ohms to -2.0 Vdc	15	13
2.0 k ohms to V_{EE}	2.5	7.7
1.0 k ohm to V_{EE}	4.9	15.4
680 ohms to V_{EE}	7.2	22.6
510 ohms to V_{EE}	9.7	30.2
270 ohms to V_{EE}	18.3	57.2
82 ohms to V_{CC} and 130 ohms to V_{EE}	15	140

FIGURE 13 – AVERAGE POWER DISSIPATION IN OUTPUT CIRCUIT WITH EXTERNAL TERMINATING RESISTORS

The power dissipation of MECL functional blocks varies with both temperature and V_{EE}. Typical variations are shown in Figure 14. The graph is normalized so that it applies to all MECL lines. The reference temperature is 25°C and the reference power is obtained by multiplying the typical I_E value (total power supply drain current specified on the data sheet) by V_{EE} (5.2 V). For those devices where only the maximum value of I_E is specified on the data sheet, typical power dissipation is approximately 80% of that calculated with the $I_{E\ (max)}$ specification.

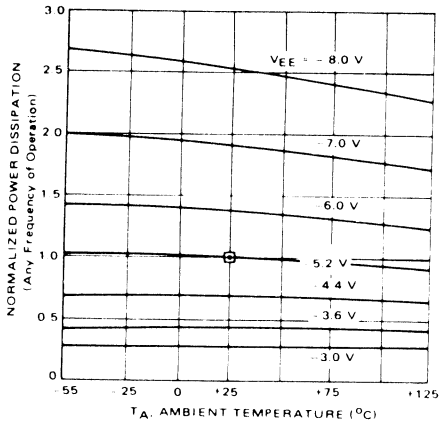


FIGURE 14 – NORMALIZED POWER DISSIPATION versus TEMPERATURE AND SUPPLY VOLTAGE

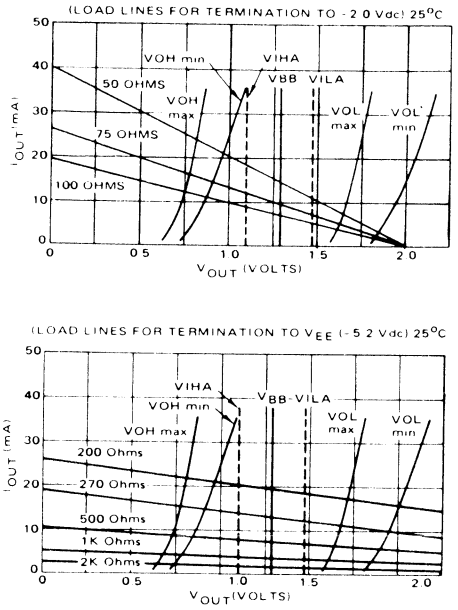


FIGURE 15 – OUTPUT VOLTAGE LEVELS versus DC LOADING

LOADING CHARACTERISTICS

The differential input to MECL circuits offers several advantages. Its common-mode-rejection feature offers immunity against power-supply noise injection, and its relatively high input impedance makes it possible for any circuit to drive a relatively large number of inputs without deterioration of the guaranteed noise margin. Hence, dc fanout with MECL circuits does not normally present a design problem.

Graphs showing typical output voltage levels as a function of load current for MECL III and 10,000 are shown in Figure 15. These graphs can be used to determine the actual output voltages for loads exceeding normal operation.

While dc loading causes a change in output voltage levels, thereby tending to affect noise margins, ac loading increases the capacitances associated with the circuit and, therefore, affects circuit speed, primarily rise and fall times.

MECL 10,000 and MECL III circuits typically have a 7 ohm output impedance and are relatively unaffected by capacitive loading on a positive-going output signal. However, the negative-going edge is dependent on the output pulldown or termination resistor. Loading close to a MECL output pin will cause an additional propagation delay of 0.1 ns per fanout load with a 50 ohm resistor to −2.0 Vdc or 270 ohms to −5.2 Vdc. A 100 ohm resistor to −2.0 Vdc or 510 ohms to −5.2 Vdc results in an additional 0.2 ns propagation delay per fanout load.

Terminated transmission line signal interconnections are used for best MECL 10,000 or MECL III system performance. The propagation delay and rise time of a driving gate are affected very little by capacitance loading along a matched parallel-terminated transmission line. However, the delay and characteristic impedance of the transmission line itself are affected by the distributed capacitance. Signal propagation down the line will be increased by a factor, $\sqrt{1+C_d/C_o}$. Here C_o is the normal intrinsic line capacitance, and C_d is the distributed capacitance due to loading and stubs off the line.

Maximum allowable stub lengths for loading off of a MECL 10,000 transmission line vary with the line impedance. For example, with Z_o = 50 ohms, maximum stub length would be 4.5 inches (1.8 in. for MECL III). But when Z_o = 100 ohms, the maximum allowable stub length is decreased to 2.8 inches (1.0 in. for MECL III).

The input loading capacitance of a MECL 10,000 gate is about 2.9 pF and 3.3 pF for MECL III. To allow for the IC connector or solder connection and a short stub length, 5 to 7 pF is commonly used in loading calculations.

UNUSED MECL INPUTS

The input impedance of a differential amplifier, as used in the typical MECL input circuit, is very high when the applied signal level is low. Under low-signal conditions, therefore, any leakage to the input capacitance of the gate could cause a gradual buildup of voltage on the input lead, thereby adversely affecting the switching characteristics at low repetition rates.

All single-ended input MECL logic circuits contain input pulldown resistors between the input transistor bases and V_{EE}. As a result, unused inputs may be left unconnected (the resistor provides a sink for I_{CBO} leakage currents, and inputs are held sufficiently negative that circuits will not trigger due to noise coupled into such inputs). Input pulldown resistor values are typically 50 kΩ and are not to be used as pulldown resistors for preceding open-emitter outputs.

Several MECL devices do not have input pulldowns. Examples are the differential line receivers. If a single differential receiver within a package is unused, one input of that receiver must be tied to the V_{BB} pin provided, and the other input goes to V_{EE}. Also, several MECL memories do not have input pulldowns on all inputs.

Several MECL circuits do not operate properly when inputs are connected to V_{CC} for a HIGH logic level. Proper design practice is to set a HIGH level as about −0.9 volts below V_{CC} with a resistor divider, a diode drop, or an unused gate output.

SECTION IV — SYSTEM DESIGN CONSIDERATIONS

THERMAL MANAGEMENT

Circuit performance and long-term circuit reliability are affected by die temperature. Normally, both are improved by keeping the IC junction temperatures low.

Electrical power dissipated in any integrated circuit is a source of heat. This heat source increases the temperature of the die relative to some reference point, normally the ambient temperature of 25°C in still air. The temperature increase, then, depends on the amount of power dissipated in the circuit and on the net thermal resistance between the heat source and the reference point.

The temperature at the junction is a function of the packaging and mounting system's ability to remove heat generated in the circuit—from the junction region to the ambient environment. The basic formula (a) for converting power dissipation to estimated junction temperature is:

$$T_J = T_A + P_D(\overline{\theta}_{JC} + \overline{\theta}_{CA}) \quad (1)$$

or

$$T_J = T_A + P_D(\overline{\theta}_{JA}) \quad (2)$$

where

T_J = maximum junction temperature
T_A = maximum ambient temperature
P_D = calculated maximum power dissipation including effects of external loads (see Power Dissipation in section III).
$\overline{\theta}_{JC}$ = average thermal resistance, junction to case
$\overline{\theta}_{CA}$ = average thermal resistance, case to ambient
$\overline{\theta}_{JA}$ = average thermal resistance, junction to ambient

This Motorola recommended formula has been approved by RADC and DESC for calculating a "practical" maximum operating junction temperature for MIL-M-38510 (JAN) MECL 10,000 devices.

Only two terms on the right side of equation (1) can be varied by the user—the ambient temperature, and the device case-to-ambient thermal resistance, $\overline{\theta}_{CA}$. (To some extent the device power dissipation can be also controlled, but under recommended use the V_{EE} supply and loading dictate a fixed power dissipation.) Both system air flow and the package mounting technique affect the $\overline{\theta}_{CA}$ thermal resistance term. $\overline{\theta}_{JC}$ is essentially independent of air flow and external mounting method, but is sensitive to package material, die bonding method, and die area.

For applications where the case is held at essentially a fixed temperature by mounting on a large or temperature-controlled heat sink, the estimated junction temperature is calculated by:

$$T_J = T_C + P_D(\overline{\theta}_{JC}) \quad (3)$$

FIGURE 16 — THERMAL RESISTANCE VALUES FOR STANDARD MECL IC CERAMIC PACKAGES

Package Type (All Using Standard* Mounting) (All Gold Eutectic Die Bond)	THERMAL RESISTANCE IN STILL AIR			
	θ_{JA} (°C/Watt)		θ_{JC} (°C/Watt)	
	Average	Maximum	Average	Maximum
14 Lead Dual-In-Line 1/4" X 3/4" Alumina Die Area = 4096 Sq. Mils	100	130	25	40
14 Lead Flat Pack 1/4" X 1/4" Alumina Die Area: 4096 Sq. Mils	165	205	40	60
16 Lead Dual-In-Line 1/4" X 3/4" Alumina Die Area: 4096 Sq. Mils	100	130	25	40
16 Lead Flat Pack 1/4" X 3/8" Beryllia Die Area = 4096 Sq. Mils	88	115	13	20
20 Lead Dual-In-Line 1/4" X 1" Alumina Die Area = 11,349 Sq. Mils	73	95	16	25
24 Lead Dual-In-Line 1/2" X 1 1/4" Alumina Die Area = 8192 Sq. Mils	45	55	10	15
24 Lead Flat Pack 3/8" X 5/8" Beryllia Die Area = 8192 Sq. Mils	40	52	6	10
48 Lead Quad-In-Line (QUIL) 1/2" X 1 1/4" Alumina Die Area = 16,384 Sq. Mils	40	52	8	12

*Standard Mounting Methods:
Dual In-Line: In socket or on PC Board with no contact between bottom of package and socket or PC Board.
Flat Pack: Bottom of Package in direct contact with non-metallized area of PC Board.

where T_C = maximum case temperature and the other parameters are as previously defined.

The maximum and average thermal resistance values for standard MECL IC packages are given in Figure 16. In Figure 17, this basic data is converted into graphs showing the maximum power dissipation allowable at various ambient temperatures (still air) for circuits mounted in the different packages, taking into account the maximum permissible operating junction temperature for long term life (≥ 100,000 hours).

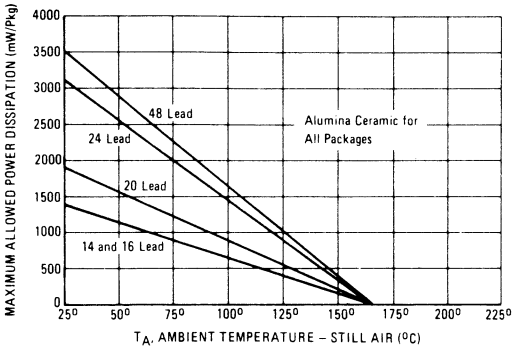


FIGURE 17a – AMBIENT TEMPERATURE DERATING CURVES (CERAMIC DUAL-IN-LINE PKG)

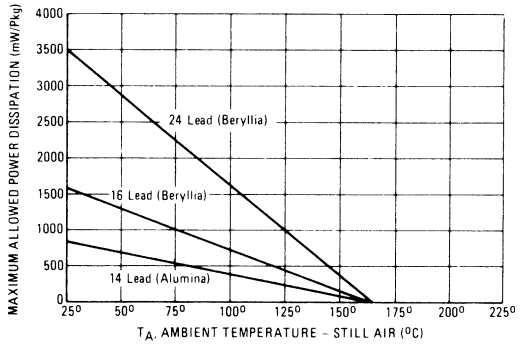


FIGURE 17b – AMBIENT TEMPERATURE DERATING CURVES (CERAMIC FLAT PKG)

per minute. From Figure 18, $\overline{\theta}_{JA}$ is 50°C/W. With T_A (air flow temperature at the device) equal to 25°C, the following maximum junction temperature results:

$$T_J = P_D(\overline{\theta}_{JA}) + T_A$$

$$T_J = (0.195\ W)\ (50°C/W + 25°C = 34.8°C$$

Under the above operating conditions, the MECL 10,000 quad gate has its junction elevated above ambient temperature by only 9.8°C.

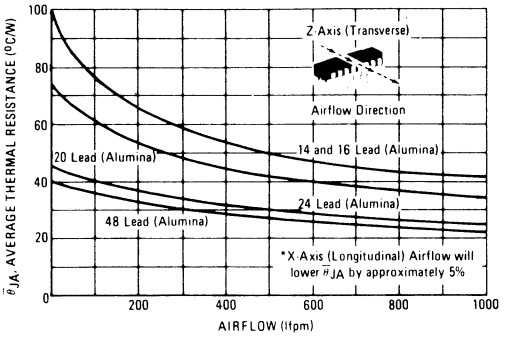


FIGURE 18a – AIRFLOW versus THERMAL RESISTANCE (CERAMIC DUAL-IN-LINE PKG)

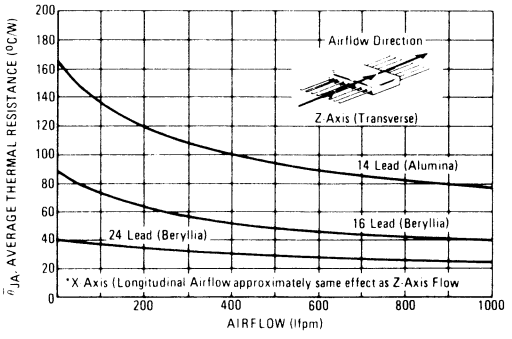


FIGURE 18b – AIRFLOW versus THERMAL RESISTANCE (CERAMIC FLAT PKG)

AIR FLOW

The effect of air flow over the packages on $\overline{\theta}_{JA}$ (due to a decrease in $\overline{\theta}_{CA}$) is illustrated in the graphs of Figure 18. This air flow reduces the thermal resistance of the package, therefore permitting a corresponding increase in power dissipation without exceeding the maximum permissible operating junction temperature.

As an example of the use of the information above, the maximum junction temperature for a 16 lead ceramic dual-in-line packaged MECL 10,000 quad OR/NOR gate (MC10101L) loaded with four 50 ohm loads can be calculated. Maximum total power dissipation (including 4 output loads) for this quad gate is 195 mW. Assume for this thermal study that air flow is 500 linear feet

Even though different device types mounted on a printed circuit board may each have different power dissipations, all will have the same input and output levels provided that each is subject to identical air flow and the same ambient air temperature. This eases design, since the only change in levels between devices is due to the increase in ambient temperatures as the air passes over the devices, or differences in ambient temperature between two devices.

The majority of MECL 10,000, 10800, and MECL III users employ some form of air-flow cooling. As air passes over each device on a printed circuit board, it absorbs heat from each package. This heat gradient from the first package to the last

package is a function of the air flow rate and individual package dissipations. Figure 19 provides gradient data at power levels of 200 mW. 250 mW, 300 mW, and 400 mW with an air flow rate of 500 lfpm. These figures show the proportionate increase in the junction temperature of each dual in-line package as the air passes over each device. For higher rates of air flow the change in junction temperature from package to package down the airstream will be lower due to greater cooling.

Power Dissipation (mW)	Junction Temperature Gradient (°C/Package)
200	0.4
250	0.5
300	0.63
400	0.88

Devices mounted on 0.062" PC board with Z axis spacing of 0.5". Air flow is 500 lfpm along the Z axis.

FIGURE 19 – THERMAL GRADIENT OF JUNCTION TEMPERATURE
(16-Pin MECL Dual In Line Package)

THERMAL EFFECTS ON NOISE MARGIN

The data sheet dc specifications for standard MECL 10,000, 10800, and MECL III devices are given for an operating temperature range from $-30^{\circ}C$ to $+85^{\circ}C$ (0° to $+75^{\circ}C$ for memories) in Figure 6b and 6c of Section II, TECHNICAL DATA. These values are based on having an airflow of 500 lfpm over socket or P/C board mounted packages with no special heat sinking (i.e., dual-in-line package mounted on lead seating plane with no contact between bottom of package and socket or P/C board and flat package mounted with bottom in direct contact with non-metallized area of P/C board). Under these conditions, adequate cooling is provided to keep the maximum operating junction temperatures below $145^{\circ}C$ for MECL III device types 1666-1670 and below $165^{\circ}C$ for all other MECL device types.

The designer may want to use MECL devices under conditions other than those given above. The majority of the low-power device types may be used without air and with higher θ_{JA}. However, the designer must bear in mind that junction temperatures will be higher for higher θ_{JA}, even though the ambient temperature is the same. Higher junction temperatures will cause logic levels to shift.

As an example, a 300 mW 16 lead dual-in-line ceramic device operated at $\theta_{JA} = 100^{\circ}C/W$ (in still air) shows a HIGH logic level shift of about 21 mV above the HIGH logic level when operated with 500 lfpm air flow and a $\theta_{JA} = 50^{\circ}C/W$. (Level shift = $\Delta T_J \times 1.4$ mV/°C).

If logic levels of individual devices shift by different amounts (depending on P_D and θ_{JA}), noise margins are somewhat reduced. Therefore, the system designer must lay out his system bearing in mind that the mounting procedures to be used should minimize thermal effects on noise margin.

The following sections on package mounting and heat sinking are intended to provide the designer with sufficent information to insure good noise margins and high reliability in MECL system use.

MOUNTING AND HEAT SINK SUGGESTIONS

With large high-speed logic systems, the use of multilayer printed circuit boards is recommended to provide both a better ground plane and a good thermal path for heat dissipation. Also, a multilayer board allows the use of microstrip line techniques to provide transmission line interconnections.

Two-sided printed circuit boards may be used where board dimensions and package count are small. If possible, the V_{CC} ground plane should face the bottom of the package to form the thermal conduction plane. If signal lines must be placed on both sides of the board, the V_{EE} plane may be used as the thermal plane, and at the same time may be used as a pseudo ground plane. The pseudo ground plane becomes the ac ground reference under the signal lines placed on the same side as the V_{CC} ground plane (now on the opposite side of the board from the packages), thus maintaining a microstrip signal line environment.

Two-ounce copper P/C board is recommended for thermal conduction and mechanical strength. Also, mounting holes for low power devices may be countersunk to allow the package bottom to contact the heat plane. This technique used along with thermal paste will provide good thermal conduction.

Printed channeling is a useful technique for conduction of heat away from the packages when the devices are soldered into a printed circuit board. As illustrated in Figure 20, this heat dissipation method could also serve as V_{EE} voltage distribution or as a ground bus. The channels should terminate into channel strips at each side or the rear of a plug-in type printed circuit board. The heat can then be removed from the circuit board, or board slide rack, by means of wipers that come into thermal contact with the edge channels.

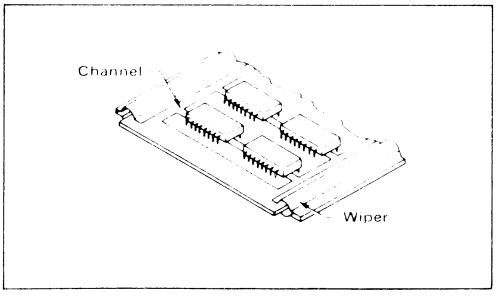


FIGURE 20 – CHANNEL/WIPER HEAT SINKING ON DOUBLE LAYER BOARD

For operating some of the higher power device types* in 16 lead dual-in-line packages in still air, requiring $\overline{\theta}_{JA} < 100^{o}C/W$, a suitable heat sink is the IERC LIC-214A2WCB shown in Figure 21. This sink reduces the still air $\overline{\theta}_{JA}$ to around 55°C/W. By mounting this heat sink directly on a copper ground plane (using silicone paste) and passing 500 lfpm air over the packages, $\overline{\theta}_{JA}$ is reduced to approximately 35°C/W, permitting use at higher ambient temperatures than +85°C (+75°C for memories) or in lowering TJ for improved reliability.

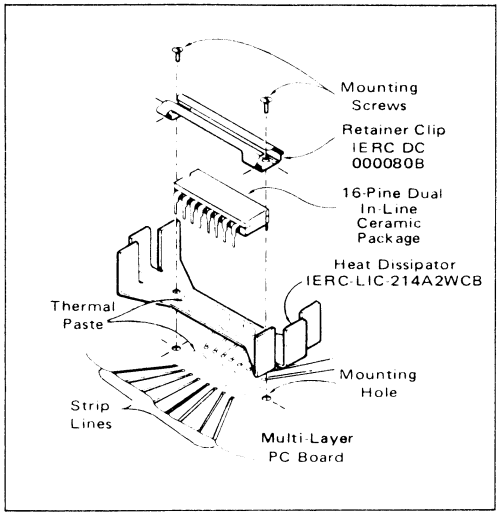


FIGURE 21 – MECL HIGH-POWER DUAL-IN-LINE PACKAGE MOUNTING METHOD

It should be noted that the use of a heat sink on the top surface of the dual-in-line package is not very effective in lowering the $\overline{\theta}_{JA}$. This is due to the location of the die near the bottom surface of the package.

Also, very little (< 10%) of the internal heat is withdrawn through the package leads due to the isolation from the ceramic by the solder glass seals and the limited heat conduction from the die through 1.0 to 1.5 mil aluminum bonding wires.

INTERFACING MECL TO SLOWER LOGIC TYPES

MECL circuits are interfaceable with most other logic forms. For MECL/TTL/DTL interfaces, when MECL is operated at the recommended −5.2 volts and TTL/DTL at +5 V supply, currently available translator circuits, such as the MC10124 and MC10125, may be used.

For systems where a dual supply (−5.2 V and +5 V) is not practical, the MC12000 includes a single supply MECL to TTL and TTL to MECL translator, or a discrete component translator can be designed. For details, see MECL System Design Handbook. Such circuits can easily be made fast enough for any available TTL.

MECL also interfaces readily with MOS. With CMOS operating at +5 V, any of the MECL to TTL translators works very well. On the other hand, CMOS will drive MECL directly when using a common −5.2 V supply.

Specific circuitry for use in interfacing MECL families to other logic types is given in detail in the MECL System Design Handbook.

Complex MECL 10,000 functions are presently available to interface MECL 10,000 with MOS logic, MOS memories, TTL three-state circuits, and IBM bus logic levels. See Application Note AN-720 for additional interfacing information.

CIRCUIT INTERCONNECTIONS

Though not necessarily essential, the use of multilayer printed circuit boards offers a number of advantages in the development of high-speed logic cards. Not only do multilayer boards achieve a much higher package density, interconnecting leads are kept shorter, thus minimizing propagation delay between packages. This is particularly beneficial with MECL III which has relatively fast (1 ns) rise and fall times. Moreover, the unbroken ground planes made possible with multilayer boards permit much more precise control of transmission line impedances when these are used for interconnecting purposes. Thus multilayer boards are recommended for MECL III layouts and are justified when operating MECL 10,000 at top circuit speed, when high-density packaging is a requirement, or when transmision line interconnects are used.

Point-to-point back-plane wiring without matched line terminations may be employed for MECL interconnections if line runs are kept short. At MECL 10,000 speeds, this applies to line runs up to 6 inches, and for MECL III up to 1 inch (maximum open wire lengths for less than 100 mV undershoot). But, because of the open-emitter outputs of MECL 10,000 and MECL III circuits, pull-down resistors are always required. Several ways of connecting such pull-down resistors are shown in Figure 22.

Resistor values for the connection in Figure 22a may range from 270 ohms to 2 kΩ depending on power and load requirements. (See MECL System Design Handbook.) Power may be saved by connecting pull-down resistors in the range of 50 ohms (100 ohm minimum for MC10,500 and MC10,600 Series parts) to 150 ohms, to −2.0 Vdc, as shown in Figure 22b. Use of a series damping resistor, Figure 22c, will extend permissible lengths of unmatched-impedance interconnections, with some loss of edge speed.

With proper choice of the series damping resistor, line lengths can be extended to any length,** while limiting overshoot and undershoot to a predetermined amount. Damping resistors usually range in value from 10 ohms to 100 ohms, depending on the line length, fanout, and line impedance. The open emitter-follower outputs of MECL III and MECL 10,000 give the system designer all possible line driving options.

* MC1654, 1678, 1694, 10128, 10129, 10136, 10137, 10177, 10182, and 10804. Max $P_D > 800$ mW.

** Limited only by line attenuation and bandwidth characteristics.

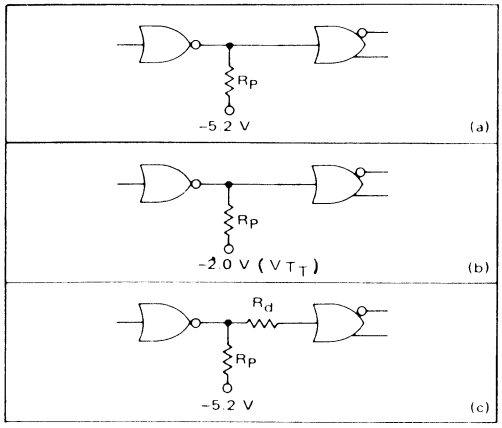


FIGURE 22 – PULL-DOWN RESISTOR TECHNIQUES

One major advantage of MECL over saturated logic is its capability for driving matched-impedance transmission lines. Use of transmission lines retains signal integrity over long distances. The MECL III and MECL 10,000 emitter-follower output transistors will drive a 50-ohm transmission line (100 ohms or greater for MECL 10,500 and MC10,600 Series) terminated to -2.0 Vdc. This is the equivalent current load of 22 mA in the HIGH logic state and 6 mA in the LOW state.

Parallel termination of transmission lines can be done in two ways. One, as shown in Figure 23a, uses a single resistor whose value is equal to the impedance (Z_0) of the line. A terminating voltage (V_{TT}) of -2.0 Vdc must be supplied to the terminating resistor.

Another method of parallel termination uses a pair of resistors, R1 and R2. Figure 23b illustrates this method. The following two equations are used to calculate the values of R1 and R2:

$$R1 = 1.6\ Z_0$$

$$R2 = 2.6\ Z_0$$

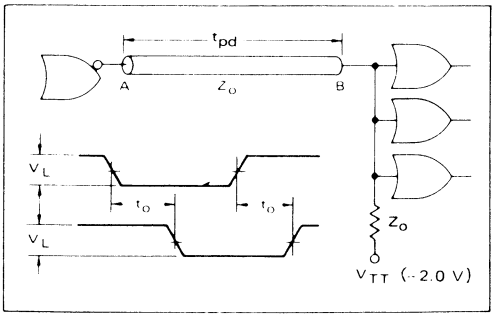


FIGURE 23a – PARALLEL TERMINATED LINE

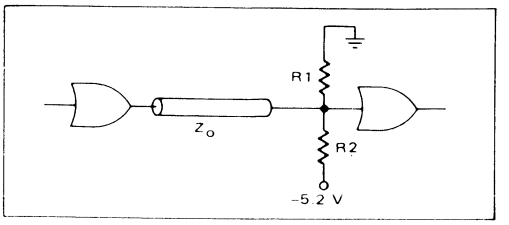


FIGURE 23b – PARALLEL TERMINATION – THEVENIN EQUIVALENT

Another popular approach is the series-terminated transmission line (see Figure 24). This differs from parallel termination in that only one-half the logic swing is propagated through the lines. The logic swing doubles at the end of the transmission line due to reflection on an open line, again establishing a full logic swing.

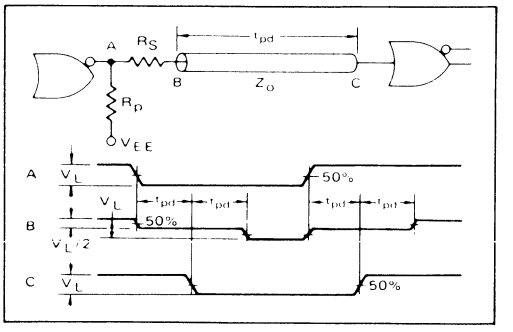


FIGURE 24 – SERIES TERMINATED LINE

To maintain clean wave fronts, the input impedance of the driven gate must be much greater than the characteristic impedance of the transmission line. This condition is satisfied by MECL circuits which have high impedance inputs. Using the appropriate terminating resistor (R_S) at point A (Figure 24), the reflections in the transmission line will be terminated.

The advantages of series termination include ease of driving multiple series-terminated lines, low power consumption, and low cross talk between adjacent lines. The disadvantage of this system is that loads may not be distributed along the transmission line due to the one-half logic swing present at intermediate points.

For board-to-board interconnections, coaxial cable may be used for signal conductors. The termination techniques just discussed also apply when using coax. Coaxial cable has the advantages of good noise immunity and low attenuation at high frequencies. No significant performance degradation occurs for lengths up to 20 feet for MECL III, and up to 50 feet for MECL 10,000.

Twisted pair lines are one of the most popular methods of interconnecting cards or panels. The complementary outputs of any MECL III or MECL 10,000 function are connected to one end of the twisted pair line, and any MECL differential line receiver to the other as shown in the example, Figure 25. R_T is used to terminate the twisted pair line. The 1 to 1.5 V common-mode noise rejection of the line receiver ignores common-mode cross talk, permitting multiple twisted pair lines to be tied into cables. MECL signals may be sent very long distances (> 1000 feet) on twisted pair, although line attenuation will limit bandwidth, degrading edge speeds when long line runs are made.

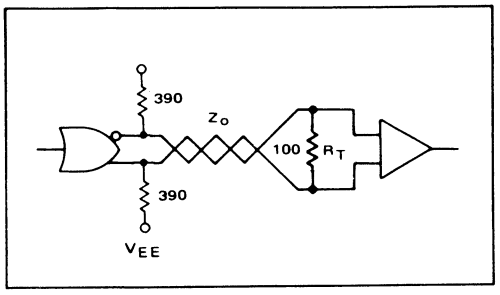


FIGURE 25 – TWISTED PAIR LINE DRIVER/RECEIVER

If timing is critical, parallel signal paths (shown in Figure 26) should be used when fanout to several cards is required. This will eliminate distortion caused by long stub lengths off a signal path.

Wire-wrapped connections can be used with MECL 10,000. For MECL III, the fast edge speeds (1 ns) create a mismatch at the wire-wrap connections which can cause reflections, thus reducing noise immunity. The mismatch occurs also with MECL 10,000, but the distance between the wire-wrap connection and the end of the line is generally short enough so the reflections cause no problem.

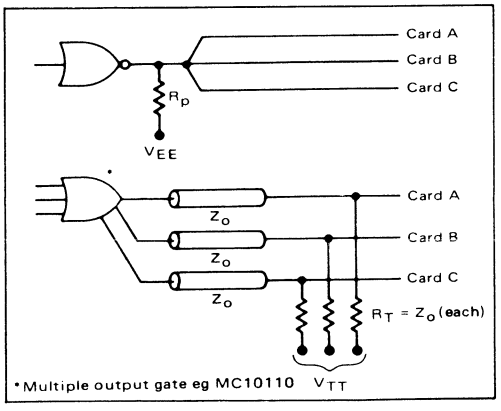


FIGURE 26 – PARALLEL FANOUT TECHNIQUES

Series damping resistors may be used with wire-wrapped lines to extend permissible backplane wiring lengths. Twisted pair lines may be used for even longer distances across large wire-wrapped cards. The twisted pair gives a more defined characteristic impedance (than a single wire), and can be connected either single-ended, or differentially using a line receiver.

The recommended wire-wrapped circuit cards have a ground plane on one side and a voltage plane on the other, to insure a good ground and a stable voltage source for the circuits. In addition, the ground plane near the wire-wrapped lines lowers the impedance of those lines and facilitates terminating the line. Finally, the ground plane serves to minimize cross talk between parallel paths in the signal lines. Point-to-point wire routing is recommended because cross talk will be minimized and line lengths will be shortest. Commercial wire-wrap boards designed for MECL 10,000 are available from several vendors.

Microstrip and Stripline

Microstrip and stripline techniques are used with printed circuit boards to form transmission lines. Microstrip consists of a constant-width conductor on one side of a circuit board, with a ground plane on the other side (shown in Figure 27). The characteristic impedance is determined by the width and thickness of the conductor, the thickness of the circuit board, and the dielectric constant of the circuit board material.

Stripline is used with multilayer circuit boards as shown in Figure 27. Stripline consists of a constant-width conductor between two ground planes.

Refer to MECL System Design Handbook for a full discussion of the properties and use of these lines.

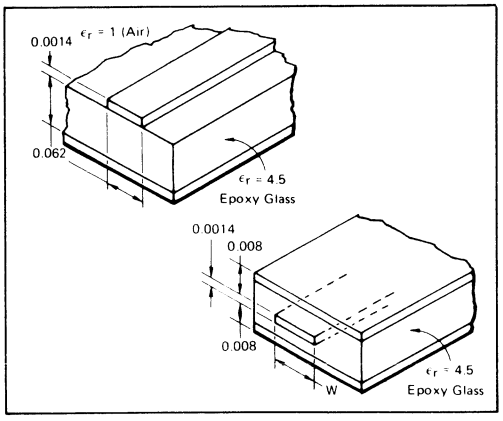


FIGURE 27 – PC INTERCONNECTION LINES FOR USE WITH MECL

CLOCK DISTRIBUTION

Clock distribution can be a system problem. At MECL 10,000 speeds, either coaxial cable or twisted pair line (using the MC10101 and MC10115) can be used to distribute clock signals throughout a system. Clock line lengths should be controlled and matched when timing could be critical. Once the clocking signals arrive on card, a tree distribution should be used for large-fanouts at high frequency. An example of the application of this technique is shown in Figure 28.

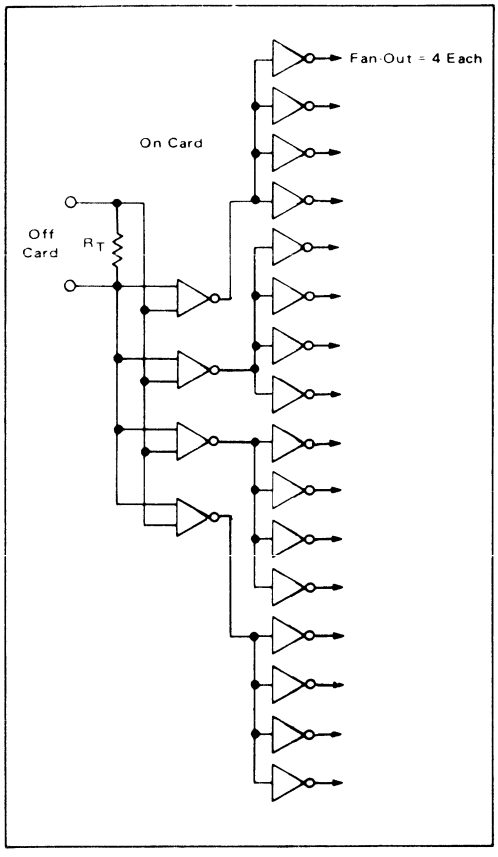


FIGURE 28 – 64 FANOUT CLOCK DISTRIBUTION

Because of the very high clock rates encountered in MECL III systems, rules for clocking are more rigorous than in slower systems.

The following guidelines should be followed for best results:

A. On-card Syncrhonous Clock Distribution via Transmission Line

1. Use the NOR output in developing clock chains or trees. Do not mix OR and NOR outputs in the chain.
2. Use balanced fanouts on the clock drivers.
3. Overshoot can be reduced by using two parallel drive lines in place of one drive line with twice the lumped load.
4. To minimize clock skewing problems on synchronous sections of the system, line delays should be matched to within 1 ns.
5. Parallel drive gates should be used when clocking repetition rates are high, or when high capacitance loads occur. The bandwidth of a MECL III gate may be extended by paralleling both halves of a dual gate. Approximately 40 or 50 MHz bandwidth can be gained by paralleling two or three clock driver gates.
6. Fanout limits should be applied to clock distribution drivers. Four to six loads should be the maximum load per driver for best high speed performance. Avoid large lumped loads at the end of lines greater than 3 inches. A lumped load, if used, should be four or fewer loads.
7. For wire-OR (emitter dotting), two-way lines (busses) are recommended. To produce such lines, both ends of a transmission line are terminated with 100-ohms impedance. This method should be used when wire-OR connections exceed 1 inch apart on a drive line.

B. Off-Card Clock Distribution

1. The OR/NOR outputs of an MC1660 may be used to drive into twisted pair lines or into flat, fixed-impedance ribbon cable. At the far end of the twisted pair an MC1692 differential line receiver is used. The line should be terminated as shown in Figure 25. This method not only provides high speed, board-to-board clock distribution, but also provides system noise margin advantages. Since the line receiver operates independently of the V_{BB} reference voltage (differential inputs) the noise margin from board to board is also independent of temperature differentials.

LOGIC SHORTCUTS

MECL circuitry offers several logic design conveniences. Among these are:

1. **Wire-OR** (can be produced by wiring MECL output emitters together outside packages).
2. **Complementary Logic Outputs** (both OR and NOR are brought out to package pins in most cases).

An example of the use of these two features to reduce gate and package count is shown in Figure 29.

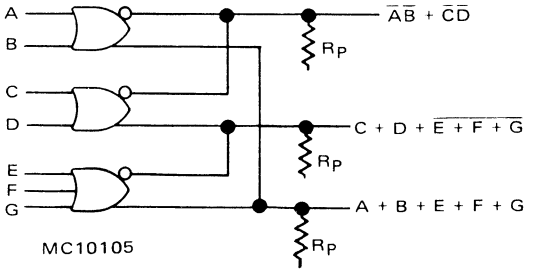


FIGURE 29 – USE OF WIRE-OR AND COMPLEMENTARY OUTPUTS

The connection shown saves several gate circuits over performing the same functions with non-ECL type logic. Also, the logic functions in Figure 29 are all accomplished with one gate propagation delay time for best system speed. Wire-ORing permits direct connections of MECL circuits to busses. (MECL System Design Handbook and Application Note AN-726).

Propagation delay is increased approximately 50 ps per wire-OR connection. In general, wire-OR should be limited to 6 MECL outputs to maintain a proper LOW logic level. The MC10123 is an exception to this rule because it has a special V_{OL} level that allows very high fanout on a bus or wire-OR line. The use of a single output pull-down resistor is recommended per wire-OR, to economize on power dissipation. However, two pull-down resistors per wired-OR can improve fall times and be used for double termination of busses.

Wire-OR should be done between gates in a package or nearby packages to avoid spikes due to line propagation delay. This does not apply to bus lines which activate only one driver at a time.

SYSTEM CONSIDERATIONS – A SUMMARY OF RECOMMENDATIONS

	MECL 10,000	MECL III
Power Supply Regulation	10% or better*	10% or better*
On-Card Temperature Gradient	Less Than 25°C	Less Than 25°C
Maximum Non-Transmission Line Length (No Damping Resistor)	8"	1"
Unused Inputs	Leave Open**	Leave Open**
PC Board	Standard 2-Sided or Multilayer	Multilayer
Special Cooling Requirements	No	No
Bus Connection Capability	Yes (Wire-OR)	Yes (Wire-OR)
MSI/LSI Parts	Yes	Yes (MSI)
Maximum Twisted Pair Length (Differential Drive)	Limited by Cable Response Only, Usually > 1000'	Limited by Cable Response Only, Usually > 1000'
The Ground Plane to Occupy Percent Area of Card	> 50%	> 75%
Wire Wrap may be used	Yes	Not Recommended
Compatible with MECL 10,000	–	Yes

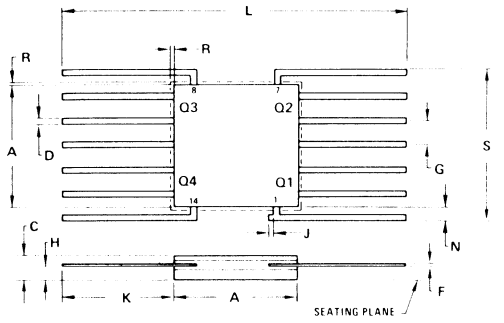
*At the devices.

**Except special functions without input pull-down resistors.

PACKAGE OUTLINE DIMENSIONS

A letter suffix to the MECL logic function part number is used to specify the package style (see drawings below). See appropriate selector guide for specific packaging available for a given device type.

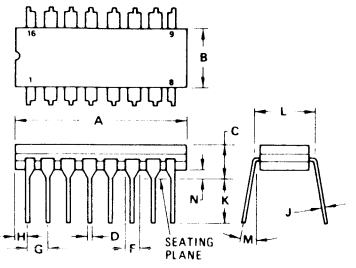
F SUFFIX
CERAMIC PACKAGE
CASE 607-04



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.10	6.99	0.240	0.275
C	0.76	2.03	0.030	0.080
D	0.25	0.48	0.010	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.13	0.89	0.005	0.035
J	–	0.38	–	0.015
K	6.35	–	0.250	–
L	18.80	–	0.740	–
N	0.25	–	0.010	–
R	–	0.38	–	0.015
S	7.62	8.38	0.300	0.330

NOTE
1 LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION RELATIVE TO "A" AT MAXIMUM MATERIAL CONDITION

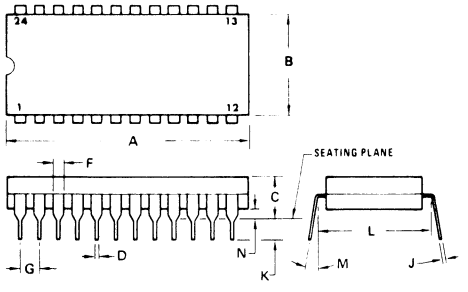
L SUFFIX
CERAMIC PACKAGE
CASE 620-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

NOTES
1 LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE
2 AT MAXIMUM MATERIAL CONDITION' PKG INDEX NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT'
3 DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL'

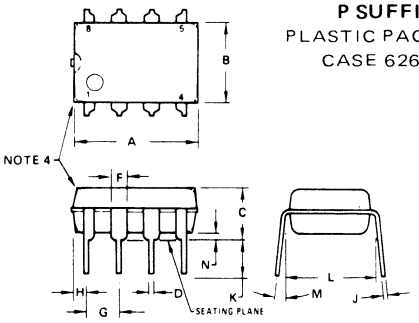
L SUFFIX
CERAMIC PACKAGE
CASE 623-03



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.29	4.06	0.090	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL)

P SUFFIX
PLASTIC PACKAGE
CASE 626-04

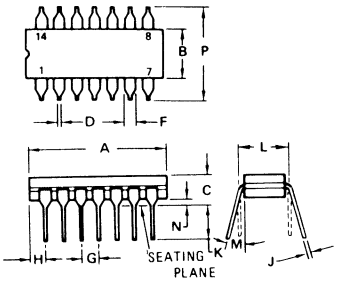


NOTES
1 LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL
3. PACKAGE CONTOUR OPTIONAL (ROUND OR SQUARE CORNERS)

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.10	6.60	0.240	0.260
C	3.94	4.45	0.155	0.175
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	0.76	1.27	0.030	0.050
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	–	10°	–	10°
N	0.51	0.76	0.020	0.030

PACKAGE OUTLINE DIMENSIONS (continued)

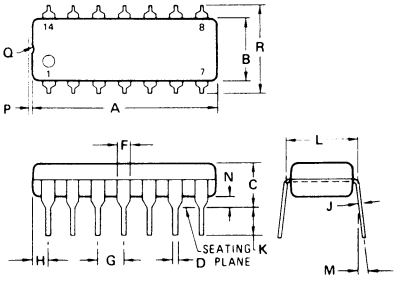
L SUFFIX
CERAMIC PACKAGE
CASE 632-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54 BSC		0.100 BSC	
J	0.203	0.381	0.008	0.015
K	2.54	–	0.100	–
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	0.76	0.020	0.030
P	–	8.25	–	0.325

NOTE: DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

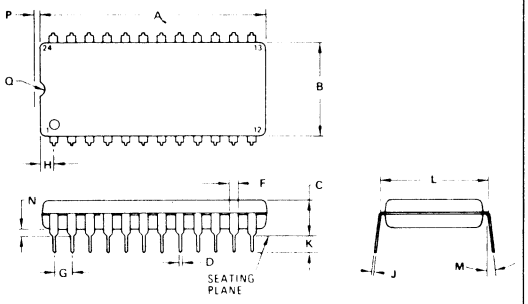
P SUFFIX
PLASTIC PACKAGE
CASE 646-04



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.03	19.56	0.710	0.770
B	6.10	6.60	0.240	0.260
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	1.02	1.78	0.040	0.070
G	2.54 BSC		0.100 BSC	
H	1.32	2.41	0.052	0.095
J	0.20	0.38	0.008	0.015
K	2.92	–	0.115	–
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51		0.020	
R	–	8.26	–	0.325

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. DIMENSION "R" TO BE MEASURED AT THE TOP OF THE LEADS (NOT AT THE TIPS).

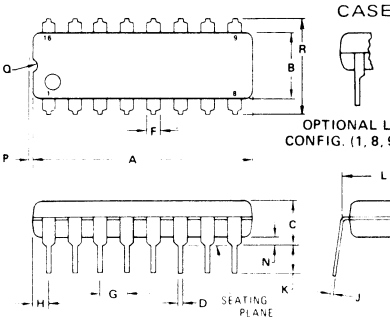
P SUFFIX
PLASTIC PACKAGE
CASE 649-03



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

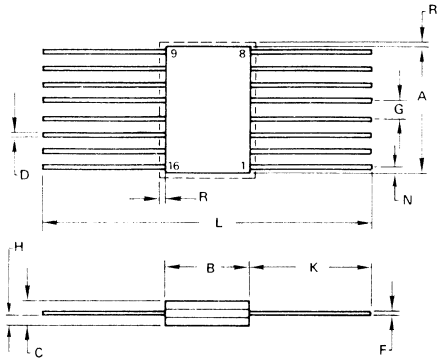
P SUFFIX
PLASTIC PACKAGE
CASE 648-04



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A		22.10	–	0.870
B	6.10	6.60	0.240	0.260
C	–	5.08	–	0.200
D	0.38	0.53	0.015	0.021
F	–	1.78	–	0.070
G	2.54 BSC		0.100 BSC	
H	0.38	2.41	0.015	0.095
J	0.20	0.38	0.008	0.015
K	2.92	–	0.115	–
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	–	0.020	–
R	–	8.26	–	0.325

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION "B" DOES NOT INCLUDE MOLD FLASH.
4. "F" DIMENSION IS FOR FULL LEADS. "HALF" LEADS ARE OPTIONAL AT LEAD POSITIONS 1, 8, 9, and 16).
5. DIMENSION "R" TO BE MEASURED AT THE TOP OF THE LEADS (NOT AT THE TIPS).

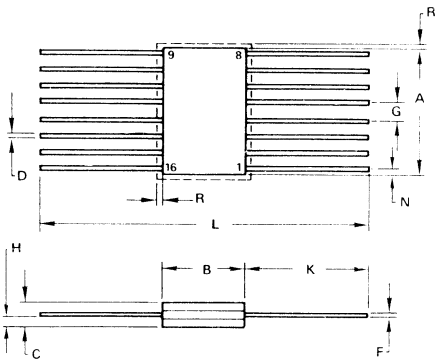
F SUFFIX
CERAMIC PACKAGE
CASE 650-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.22	6.60	0.245	0.260
C	1.52	2.03	0.060	0.080
D	0.38	0.48	0.015	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.64	0.89	0.025	0.035
K	6.35	9.40	0.250	0.370
L	18.92	–	0.745	–
N	–	0.51	–	0.020
R	–	0.38	–	0.015

NOTES:
1. LEAD NO. 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
2. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

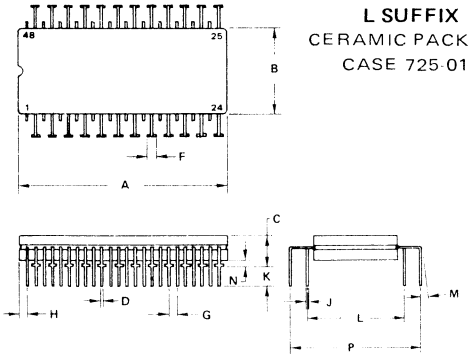
F SUFFIX
CERAMIC PACKAGE
CASE 650-03



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.40	10.16	0.370	0.400
B	6.22	7.24	0.245	0.285
C	1.52	2.03	0.060	0.080
D	0.41	0.48	0.016	0.019
F	0.08	0.15	0.003	0.006
G	1.27 BSC		0.050 BSC	
H	0.64	0.89	0.025	0.035
K	6.35	9.40	0.250	0.370
L	18.92		0.745	
N	–	0.51	–	0.020
R	–	0.38	–	0.015

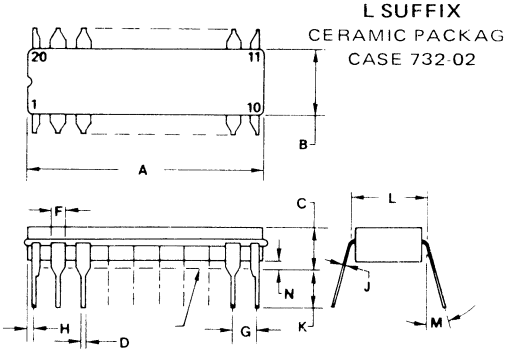
NOTES:
1. LEAD NO. 1 IDENTIFIED BY TAB ON LEAD OR DOT ON COVER.
2. LEADS WITHIN 0.13 mm (0.005) TOTAL OF TRUE POSITION AT MAXIMUM MATERIAL CONDITION.

L SUFFIX
CERAMIC PACKAGE
CASE 725-01



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.57	5.59	0.180	0.220
D	0.38	0.53	0.015	0.021
F	1.14	1.40	0.045	0.055
G	1.27 BSC		0.050 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.54	3.30	0.100	0.130
L	15.24 BSC		0.600 BSC	
M	–	7°	–	7°
N	0.51	1.52	0.020	0.060
P	20.32 BSC		0.800 BSC	

L SUFFIX
CERAMIC PACKAGE
CASE 732-02



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	24.38	25.15	0.960	0.990
B	6.86	7.49	0.270	0.295
C	4.32	5.08	0.170	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	5°	15°	5°	15°
N	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.25 mm (0.010) DIA , TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION.
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS.

SUPPLEMENTARY LITERATURE

1. "Improve Fast-Logic Designs," by Bill Blood, Electronic Design, May 10, 1973.
2. "Interface TTL Systems with ECL Circuits," by George Adams, EDN, September 5, 1973.
3. "Increasing Minicomputer Speed with Emitter-Coupled Logic," by Jon De Laune, Computer Design, February 1974.
4. "An Engineering Comparison Study MECL 10,000 and Schottky TTL," Motorola Inc., 1974.
5. "ECL Circuits Drive Light-Emitting Diodes," by Bill Blood, EDN, January 20, 1974.
6. "Four-Digit BCD Programmability Featured in Variable Modulus 60 MHz Counter," by Tom Balph and Bill Blood, Electronic Design, March 15, 1974.
7. "Build a Low Cost ECL Logic Probe," by Tom Balph, Electronic Design, August 16, 1974.
8. "A CAD Program for High Speed Logic Element Interconnections," by Thomas Balph, William Blood, and Jerry Prioste, Computer Design, May 1975.
9. "Build a Clock Bias Circuit for ECL Flip-Flops," by T. Balph and H. Gnauden, EDN, May 5, 1975.
10. "M10800 Microprogrammed Demonstrator" by T. Balph, Electro 77, Session 31.
11. "Get the Best Processor Performance by Building It From ECL Bit Slices," by Tom Balph and Bill Blood, Electronic Design, June 7, 1977.
12. "M10800, A MECL Microprogrammable On-Line Demonstrator," by Tom Balph, Motorola Inc, 1977.
13. "MECL System Design Handbook," by Bill Blood, Motorola Inc.

APPLICATION NOTES

Copies of these Application Notes and Engineering Bulletins can be obtained from your Motorola representative or authorized distributor, or from Technical Information Center, Motorola Semiconductor Products Inc., P.O. Box 20912, Phoenix, Arizona 85036.

AN-270 Nanosecond Pulse Handling Techniques

AN-417B IC Crystal Controlled Oscillators

AN-504 The MC1600 Series MECL III Gates

AN-532A MTTL and MECL Avionics Digital Frequency Synthesizer

AN-556 Interconnection Techniques for Motorola's MECL 10,000 Series Emitter Coupled Logic

AN-565 Using Shift Registers as Pulse Delay Networks

AN-567 MECL Positive and Negative Logic

AN-579 Testing MECL 10,000 Integrated Logic Circuits

AN-581 An MSI 500 MHz Freuqency Counter Using MECL and MTTL

AN-583 A MECL 10,000 Main Frame Memory Employing Dynamic MOS RAMs

AN-584 Programmable Counters Using the MC10136 and MC10137 MECL 10,000 Universal Counters

AN-586 Measure Frequency and Propagation Delay with High Speed MECL Circuits

AN-592 AC Noise Immunity of MECL 10,000 Integrated Circuits

AN-700 Simulate MECL System Interconnections with a Computer Program

AN-701 Understanding MECL 10,000 DC and AC Data Sheet Specifications

AN-709 MECL 10,000 Arithmetic Elements, MC10179, MC10180, MC10181

AN-720 Interfacing with MECL 10,000 Integrated Circuits

AN-726 Bussing with MECL 10,000 Integrated Circuits

AN-730 A High-Speed FIFO Memory Using the MECL MCM10143 Register File

AN-742 A 200 MHz Autroranging MECL-McMOS Frequency Counter

AN-744 A Phase-Locked Loop Tuning System for Television

AN-746 A 3-1/2 Digit DVM Using an Integrated Circuit Dual Ramp System

AN-774 A Simple High Speed Bipolar Microprocessor Illustrates System Design and Microprogram Techniques

AN-776 The M10800 MECL LSI Processor Family

EB-47 Event Counter and Storage Latches for High Frequency, High Resolution Counters

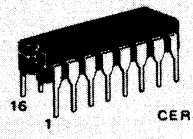
EB-48 A Time Base and Control Logic Subsystem for High Frequency, High Resolution Counters

SELECTOR GUIDES

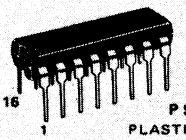
2

MECL 10,000
INTEGRATED CIRCUITS

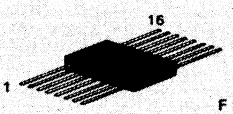
MC10,100/10,200 Series (-30 to +85°C)
MC10,500/10,600 Series (-55 to +125°C)



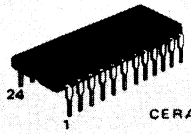
L SUFFIX
CERAMIC PACKAGE
CASE 620



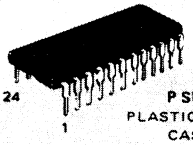
P SUFFIX
PLASTIC PACKAGE
CASE 648



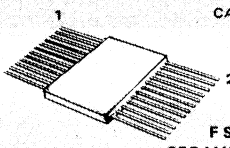
F SUFFIX
CERAMIC PACKAGE
CASE 650



L SUFFIX
CERAMIC PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 649



F SUFFIX
CERAMIC PACKAGE
CASE 652

Function	Device Type		Case
	-30 to +85°C	-55 to +125°C	
NOR GATES			
Quad 2-Input with Strobe	MC10100	MC10500	**620, 648, 650**
Quad 2-Input	MC10102	MC10502	620, 648, 650
Triple 4-3-3-Input	MC10106	MC10506	620, 648, 650
Dual 3-Input 3-Output	MC10111	–	620, 648
(High Speed)	MC10211	MC10611	**620, 648, 650**
OR GATES			
Quad 2-Input	MC10103	MC10503	**620, 648, 650**
Dual 3-Input 3-Output	MC10110	–	620, 648
(High Speed)	MC10210	MC10610	**620, 648, 650**
AND GATES			
Quad 2-Input	MC10104	MC10504	620, 648, 650
Hex	MC10197	MC10597	**620, 648, 650**
COMPLEX GATES			
Quad OR/NOR	MC10101	MC10501	620, 648, 650
Triple 2-3-2 Input OR/NOR	MC10105	MC10505	620, 648, 650
Triple 2-Input Exclusive OR/Exclusive NOR	MC10107	MC10507	620, 648, 650
Dual 4-5-Input OR/NOR	MC10109	MC10509	620, 648, 650
Quad Exclusive OR	MC10113	MC10513	620, 648, 650
Dual 2-Wide 2-3-Input OR-AND/OR-AND-Invert	MC10117	MC10517	620, 648, 650
Dual 2-Wide 3-Input OR-AND	MC10118	MC10518	620, 648, 650
4-Wide 4-3-3-3 Input OR-AND Gate	MC10119	MC10519	620, 648, 650
OR-AND/OR-AND-INVERT Gate	MC10121	MC10521	620, 648, 650
Hex Buffer with Enable	MC10188	–	620, 648
Hex Inverter with Enable	MC10189	–	620, 648
Hex Inverter/Buffer	MC10195	MC10595	620, 648, 650
High-Speed Dual 3-Input 3-Output OR/NOR	MC10212	MC10612	620, 648, 650
TRANSLATORS			
Quad MTTL to MECL	MC10124	MC10524	620, 648, 650
Quad MECL to MTTL	MC10125	MC10525	620, 648, 650
Triple MECL to NMOS	MC10177	–	620
RECEIVERS			
Triple Line	MC10114	MC10514	620, 648, 650
Quad Line	MC10115	MC10515	620, 648, 650
Triple Line	MC10116	MC10516	620, 648, 650
(High Speed)	MC10216	MC10616	**620, 648, 650**
Quad Bus	MC10129	–	620

MECL 10,000 INTEGRATED CIRCUITS (continued)

Function	Device Type		Case
	-30 to +85°C	-55 to +125°C	
FLIP-FLOPS			
Dual Type D Master-Slave	MC10131	MC10531	620, 648, 650
(High Speed)	MC10231	MC10631	620, 648, 650
Dual J-K Master-Slave	MC10135	MC10535	620, 648, 650
Hex D Master-Slave	MC10176	MC10576	620, 648, 650
DRIVERS			
Triple 4-3-3 Input Bus Driver	MC10123	–	620, 648
Bus Driver	MC10128	–	620
PARITY CHECKER			
12-Bit Parity Generator-Checker	MC10160	MC10560	620, 648, 650
ENCODER			
8-Input Encoder	MC10165	MC10565	620, 648, 650
DECODERS			
Binary to 1-8 (low)	MC10161	MC10561	620, 648, 650
Binary to 1-8 (high)	MC10162	MC10562	620, 648, 650
Dual Binary to 1-4 (low)	MC10171	MC10571	620, 648, 650
Dual Binary to 1-4 (high)	MC10172	MC10572	620, 648, 650
DATA SELECTORS/MULTIPLEXERS			
Dual Multiplexer with Latch and Common Reset	MC10132	MC10532	620, 648, 650
Dual Multiplexer with Latch	MC10134	MC10534	620, 648, 650
Quad 2-Input Multiplexer (non-inverting)	MC10158	MC10558	620, 648, 650
Quad 2-Input Multiplexer (inverting)	MC10159	MC10559	620, 648, 650
8-Line Multiplexer	MC10164	MC10564	620, 648, 650
Quad 2-Input Multiplexer/Latch	MC10173	–	620, 648
Dual 4 to 1 Multiplexer	MC10174	MC10574	620, 648, 650
LATCHES			
Quad (common clock)	MC10130	MC10530	620, 648, 650
Quad (negative transition)	MC10133	MC10533	620, 648, 650
Quad (positive transition)	MC10153	MC10553	620, 648, 650
Quad	MC10168	MC10568	620, 648, 650
Quint	MC10175	MC10575	620, 648, 650
MULTIVIBRATORS			
Monostable Multivibrator	MC10198	–	620, 648
SHIFT REGISTERS			
Four-Bit Universal	MC10141	MC10541	620, 648, 650
ERROR DETECTION-CORRECTION			
IBM Code	MC10163	MC10563	620, 648, 650
Motorola Code	MC10193	MC10593	620, 648, 650
COUNTERS			
Universal Hexadecimal	MC10136	MC10536	620, 648, 650
Universal Decade	MC10137	MC10537	620, 648, 650
Bi-Quinary	MC10138	MC10538	620, 648, 650
Binary	MC10178	MC10578	620, 648, 650
GENERATOR-CHECKER			
9 + 2-Bit Parity	MC10170	MC10570	620, 648, 650
Hex "D" Master-Slave/with Reset	MC10186	MC10586	620, 648, 650
Quad MST-to-MECL 10,000	MC10190	MC10590	620, 648, 650
Hex MECL 10,000-to-MST	MC10191	MC10591	620, 648, 650
BUS TRANSCEIVER			
Dual Simultaneous	MC10194	MC10594	620, 648, 650
ARITHMETIC FUNCTIONS			
Look-Ahead Carry Block	MC10179	MC10579	620, 648, 650
Dual High Speed Adder/Subtractor	MC10180	MC10580	620, 648, 650
4-Bit Logic Unit/Function Generator	MC10181	MC10581	623, 649, 652
2-Bit Logic Unit/Function Generator	MC10182	MC10582	620, 648, 650
4 x 2 Multiplier	MC10183	–	623
2 x 1-Bit Array Multiplier (High Speed)	MC10287	MC10687	620, 648, 650

Function	Device Type		Case
	-30 to +85°C	-55 to +125°C	
COMPARATOR			
5-Bit Magnitude	MC10166	MC10566	620, 648 650
MEMORIES			
16-Bit Multiport Register File (RAM) (8 x 2)	MCM10143	—	623
64-Bit Random Access (64 x 1)	MCM10148	MCM10548	620, 650
64-Bit Register File (RAM) (16 x 4)	MCM10145	MCM10545	620, 650
128-Bit Random Access (128 x 1)	MCM10147	MCM10547	620, 650
256-Bit Random Access (256 x 1)	MCM10144	MCM10544	620, 650
256-Bit Random Access (256 x 1)	MCM10152	MCM10552	620, 650
1024-Bit Random Access (1024 x 1)	MCM10146	MCM10546	620, 650
256-Bit Programmable Read Only (32 x 8)	MCM10139	MCM10539	620, 650
1024-Bit Programmable Read Only (256 x 4)	MCM10149	MCM10549	620, 650

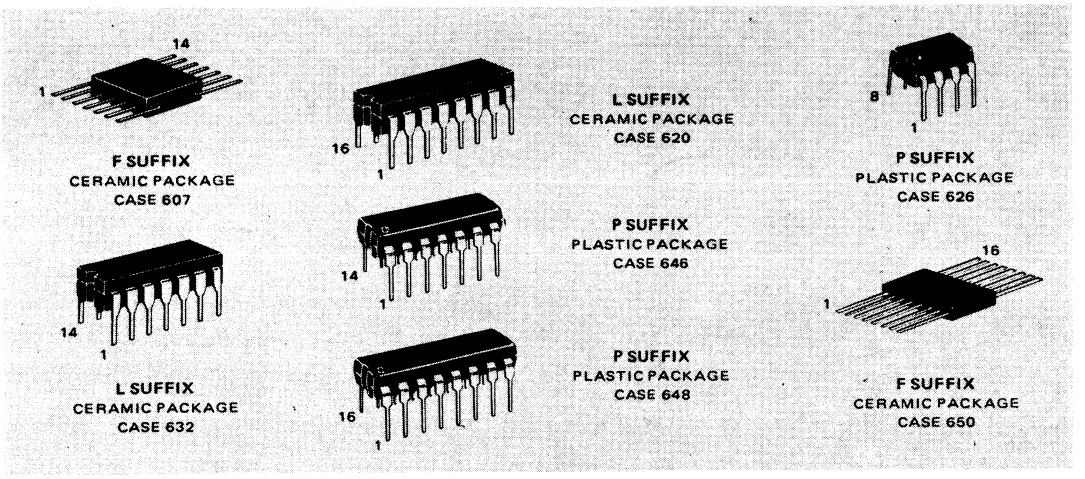
MIL-M-38510 JAN QUALIFIED MECL DEVICES

Function and Standard Equivalent	MIL-M-38510 Device
Quad OR/NOR Gate (MC10501)	JM38510/06001BEB, BFB
Quad 2-Input NOR Gate (MC10502)	JM38510/06002BEB, BFB
Triple 2-3-2 OR/NOR Gate (MC10505)	JM38510/06003BEB, BFB
Triple 4-3-3 NOR Gate (MC10506)	JM38510/06004BEB, BFB
Triple Exclusive OR/NOR Gate (MC10507)	JM38510/06005BEB, BFB
Dual 4-5 Input OR/NOR Gate (MC10509)	JM38510/06006BEB, BFB
Dual D Flip-Flop (MC10531)	JM38510/06101BEB, BFB
Dual D Flip-Flop (MC10631)	JM38510/06102BEB, BFB
Hex D Flip-Flop (MC10576)	JM38510/06103BEB, BFB
Dual J-K Flip-Flop (MC10535)	JM38510/06104BEB, BFB

MIL-M-38510 PROCESSED MECL CIRCUITS are also available. Contact your Motorola sales representative or authorized distributor for details.

MECL III
INTEGRATED CIRCUITS

MC1600 Series (-30 to +85°C)



Function	Device Type -30° to +85°C	Case
GATES		
Dual 4-Input OR/NOR	MC1660	620, 650
Dual 4-5-Input OR/NOR	MC1688	650
Quad 2-Input NOR	MC1662	620, 650
Triple 2-Input Exclusive NOR	MC1674	620, 650
Quad 2-Input OR	MC1664	620, 650
Triple 2-Input Exclusive OR	MC1672	620, 650
FLIP-FLOPS		
Dual Clocked R-S	MC1666	620, 650
Dual Clocked Latch	MC1668	620, 650
Master-Slave Type D	MC1670	620, 650
UHF Prescaler Type D	MC1690	620, 650
COUNTERS		
Binary	MC1654	620
Bi-Quinary	MC1678	620
1 GHz Divide-by-Four	MC1699	620, 650
SHIFT REGISTER		
4-Bit Shift	MC1694	620
MULTIVIBRATOR		
Voltage-Controlled	MC1658	620,648,650
OSCILLATOR		
Emitter Coupled	MC1648	607,632,646
COMPARATOR		
Dual A/D	MC1650/MC1651	620, 650
RECEIVER		
Quad Line	MC1692	620, 650
PRESCALER		
1 GHz Divide-by-Four	MC1697	626

COMPUTER SLICES

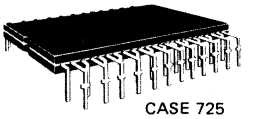
The MECL 10800
ECL 4-bit slice processor family

LSI INTEGRATED CIRCUITS

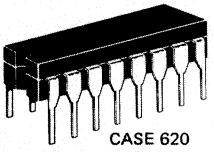
2

MC10800 series (−30 °C to +85 °C)
MC10800 M series (−55 °C to +150 °C T_J)

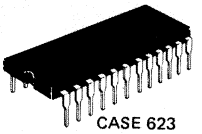
New Package: QUIL—48 pins



CASE 725
L Suffix
Ceramic Package



CASE 620
L Suffix
Ceramic Package



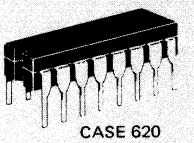
CASE 623
L Suffix
Ceramic Package

CASE 729
L Suffix
Ceramic Package

Function	Device Type	Case
4-bit Processor Slice	MC10800	725
Microprogram Control Function	MC10801	725
Timing Function	MC10802	623
Memory Interface Function	MC10803	725
4-bit Bidirectional Translator with Latch (ECL ↔ TTL)	MC10804	620
5-bit Bidirectional Translator with Latch (ECL ↔ TTL)	MC10805	729
Dual Access Stack	MC10806	725
5-bit Bidirectional MECL Transceiver with Latch	MC10807	620
Multibit Shifter (16 bits)	MC10808	725

PHASE-LOCKED LOOP

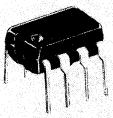
CASE 607
Plastic Package



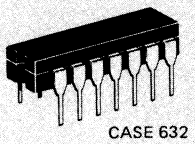
CASE 620
Ceramic Package

Motorola offers the designer a choice of specially designed integrated circuits for performing phase-locked loop functions: phase detection, frequency division, filtering, and voltage-controlled signal generation. In addition, the choice of circuits permits the designer to select TTL circuits where speed is not critical (<25 MHZ), or ECL circuits where high speed is required. The MC12000 series circuits will operate at either −5.0 V or −5.2 V, and translators are included where needed so that all functions are compatible.

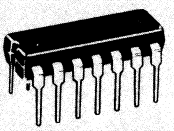
2



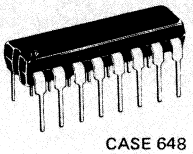
CASE 626
Plastic Package



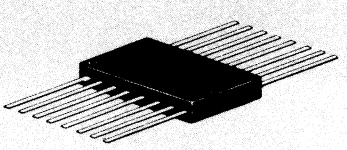
CASE 632
Ceramic Package



CASE 646
Plastic Package



CASE 648
Plastic Package



Logic Products for Phase-Locked Loop Applications

FUNCTIONS AND CHARACTERISTICS

	Temperature Range			Family	Frequency MHz (typ.)	Power Dissip. mW (typ./pkg.)	Case
	0 to 75 °C	−30 to +85 °C	−55 to +125 °C				
Voltage Controlled Oscillator		MC1648	MC1648M	MECL	225	150	607, 632, 646
Voltage Controlled Multivibrator		MC1658		MECL	150	125	620, 648, 650
÷4 Prescaler (Low Cost)	MC1697			MECL	1200	320	626
÷4 Prescaler		MC1699		MECL	1200	320	620, 650
Dual Voltage Controlled Multivibrator	MC4024		MC4324	MTTL	30	150	607, 632, 646
Programmable ÷ N Decade (÷0-9)	MC4016		MC4316	MTTL	10	250	620, 648, 650
Two programmable ÷ N (÷0-1, ÷0-4)	MC4017		MC4317	MTTL	10	250	620, 648, 650
Programmable ÷ N Hexadecimal (÷0-15)	MC4018		MC4318	MTTL	10	250	620, 648, 650
Two programmable ÷ N (÷0-3, ÷0-3)	MC4019		MC4319	MTTL	10	250	620, 648, 650
Universal (÷2-12 except 7 and 11)	MC4023		MC4323	MTTL	30	200	632, 646, 607
Phase Frequency Detector	MC4044		MC4344	MTTL	8	85	607, 632, 646
Digital Mixer/Translator	MC12000			MECL	250	425	632, 646
Analog Mixer		MC12002	MC12502	MECL	300	60	632, 646
2-Modulus Prescaler (÷5, ÷6)		MC12009	MC12509	MECL	500	310	TBA* 620, 648
2-Modulus Prescaler (÷8, ÷9)		MC12011	MC12511	MECL	600	310	TBA* 620, 648
Prescaler (÷2, ÷5/6, ÷10/11, ÷10/12)	MC12012			MECL	200	495	620, 648
2-Modulus Prescaler (÷10, ÷11)		MC12013	MC12513	MECL	600	310	620, 648
Counter Control Logic	MC12014		MC12514	MECL	25	150	620, 648
Offset Control Logic		MC12020	MC12520	MECL		35	632, 646
Offset Programmer		MC12021	MC12521	MECL		35	620, 648
Analog Loop		MC12030	MC12530	MECL	50		TBA*
Phase Frequency Detector	MC12040		MC12540	MECL	70	520	632, 646, 607
Crystal Oscillator	MC12060		MC12560	MECL	0.1 to 2.0	175	620, 648
Crystal Oscillator	MC12061		MC12561	MECL	2.0 to 20	210	620, 648

*TBA: To be announced

– other parts for PLL Application are available in TTL-LS and C-MOS –

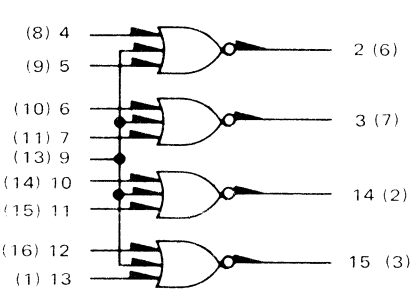
2

MECL 10,000 Logic

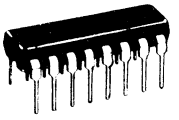
3

MC10100/MC10500

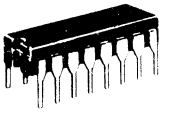
QUAD 2-INPUT NOR GATE WITH STROBE



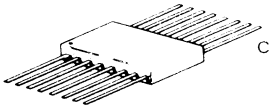
V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10100 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10500 only

P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
$t+, t-$ = 2.0 ns typ (20% to 80%)

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	29	–	29	–	26	–	29	–	29	mAdc
Input Current	I_{inH}											μAdc
Independent Inputs		–	415	–	390	–	245	–	245	–	245	
Common Input		–	800	–	750	–	470	–	490	–	470	
Switching Times												ns
Propagation Delay	t_{pd}	1.0	3.7	1.0	3.1	1.0	2.9	1.0	3.3	1.0	3.7	
Rise Time, Fall Time (20% to 80%)	t+,t−	1.0	4.0	1.1	3.6	1.1	3.3	1.1	3.7	1.0	4.0	ns

−55°C and +125°C test values apply to MC105xx devices only.

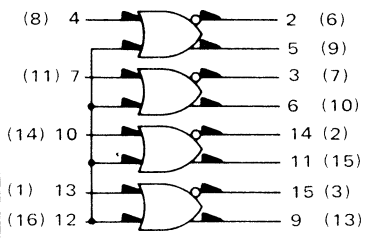
MC10101/MC10501

QUAD OR/NOR GATE

MC10102/MC10502

QUAD 2-INPUT NOR GATE

MC10101/MC10501



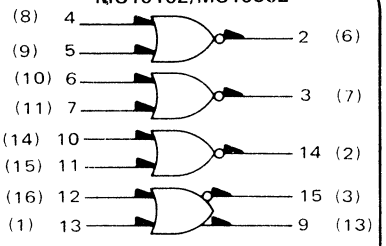
P_D = 25 mW typ/gate (No Load)

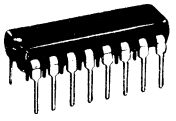
t_{pd} = 2.0 ns typ

t^+, t^- = 2.0 ns typ (20% to 80%)

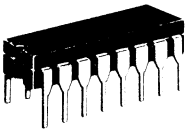
V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

MC10102/MC10502

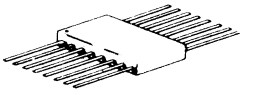




P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10101 and
MC10102 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10501 and
MC10502 only

3

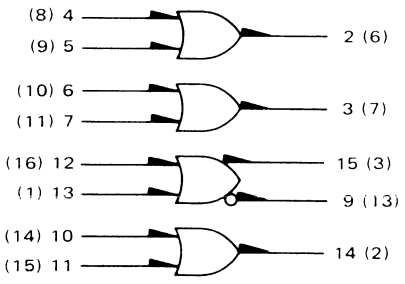
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	29	–	29	–	26	–	29	–	29	mAdc
Input Current	I_{inH}											µAdc
Independent Inputs		–	450	–	425	–	265	–	265	–	245	
Common Input (MC10101/10501)		–	910	–	850	–	535	–	535	–	535	
Switching Times												ns
Propagation Delay	t_{pd}	1.0	3.7	1.0	3.1	1.0	2.9	1.0	3.3	1.0	3.7	
Rise Time, Fall Time (20% to 80%)	t^+, t^-	1.0	4.0	1.1	3.6	1.1	3.3	1.1	3.7	1.0	4.0	ns

−55°C and +125°C test values apply to MC105xx devices only.

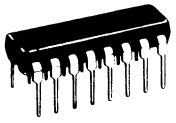
MC10103/MC10503

QUAD 2-INPUT OR GATE

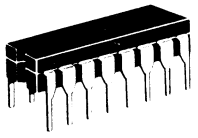


P_D = 25 mW typ/gate (No Load)
t_{pd} = 2.0 ns typ
t+, t− = 2.0 ns typ (20% − 80%)

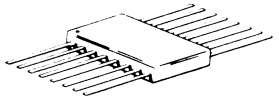
V_{CC1} Pin 1 (5)
V_{CC2} Pin 16 (4)
V_{EE} Pin 8 (12)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10103 only



L SUFFIX
CERAMIC PACKAGE
CASE 620

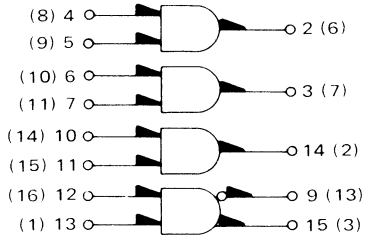


F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10503 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

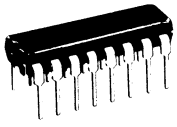
Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	29	–	29	–	26	–	29	–	29	mAdc
Input Current	I_{inH}	–	415	–	390	–	245	–	245	–	245	μAdc
Switching Times												ns
Propagation Delay	t_{pd}	1.0	3.7	1.0	3.1	1.0	2.9	1.0	3.3	1.0	3.7	
Rise Time, Fall Time (20% to 80%)	t+,t−	1.1	4.0	1.1	3.6	1.1	3.3	1.1	3.7	1.1	4.0	ns

−55°C and +125°C test values apply to MC105xx devices only.

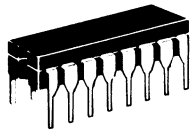


P_D = 35 mW typ/gate (No load)
t_{pd} = 2.7 ns typ
t+, t− = 2.0 ns typ (20% − 80%)

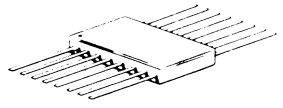
V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10104 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10504 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C Min	−55°C Max	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	I_E	–	39	–	39	–	35	–	39	–	39	mAdc
Input Current	I_{inH}											μAdc
Pins 4, 7, 10, 13		–	450	–	425	–	265	–	265	–	265	
Pins 5, 6, 11, 12		–	375	–	350	–	220	–	220	–	220	
Switching Times												ns
Propagation Delay	t_{pd}	1.0	4.3	1.0	4.3	1.0	4.0	1.0	4.2	1.0	4.7	
Rise Time, Fall Time (20% to 80%)	t+, t−	1.3	3.8	1.5	3.7	1.5	3.5	1.5	3.6	1.2	4.1	ns

−55°C and +125°C test values apply to MC105xx devices only.

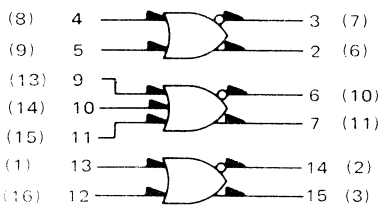
MC10105/MC10505

TRIPLE 2-3-2 INPUT OR/NOR GATE

MC10106/MC10506

TRIPLE 4-3-3 INPUT NOR GATE

MC10105/MC10505



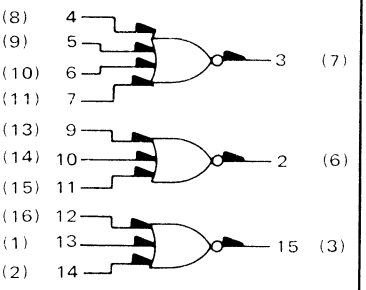
P_D = 30 mW typ/gate (No Load)

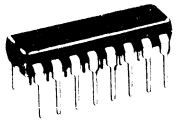
t_{pd} = 2.0 ns typ

t_+, t_- = 2.0 ns typ (20% to 80%)

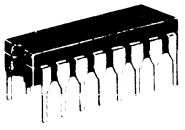
V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

MC10106/MC10506

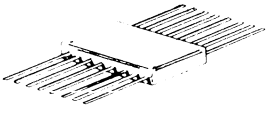




P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10105 and
MC10106 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10505 and
MC10506 only

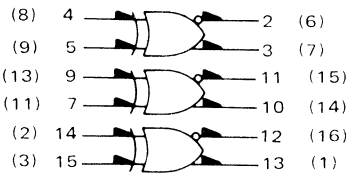
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	24	–	23	–	21	–	23	–	24	mAdc
Input Current	I_{inH}	–	450	–	425	–	265	–	265	–	265	μAdc
Switching Times												ns
Propagation Delay	t_{pd}	1.0	3.7	1.0	3.1	1.0	2.9	1.0	3.3	1.0	3.7	
Rise Time, Fall Time (20% to 80%)	t_+, t_-	1.0	4.0	1.1	3.6	1.1	3.3	1.1	3.7	1.0	4.0	ns

-55°C and +125°C test values apply to MC105xx devices only.

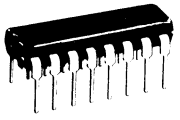
MC10107/MC10507

TRIPLE 2-INPUT EXCLUSIVE OR/EXCLUSIVE NOR

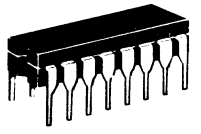


P_D = 40 mW typ/gate (No Load)
t_{pd} = 2.8 ns typ
t^+, t^- = 2.5 ns typ (20% to 80%)

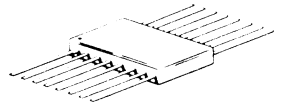
V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)



P SUFFIX
CERAMIC PACKAGE
CASE 648
MC10107 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10507 only

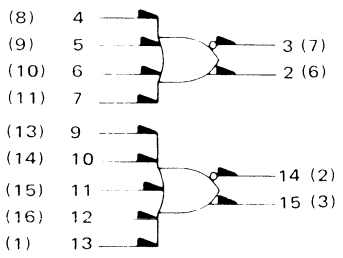
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	--	31	--	31	--	28	--	31	--	31	mAdc
Input Current	I_{inH}											μAdc
Pins 4, 9, 14		--	450	--	425	--	265	--	265	--	265	
Pins 5, 7, 15		--	375	--	350	--	220	--	220	--	220	
Switching Times												ns
Propagation Delay	t_{pd}	1.0	4.5	1.1	3.8	1.1	3.7	1.1	4.0	1.0	4.5	
Rise Time, Fall Time (20% to 80%)	t^+, t^-	1.0	4.3	1.1	3.5	1.1	3.5	1.1	3.8	1.0	4.3	ns

-55°C and +125°C test values apply to MC105xx devices only.

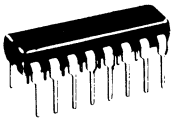
MC10109/MC10509

DUAL 4-5 INPUT OR/NOR GATE

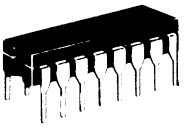


t_{pd} = 2.0 ns typ
P_D = 30 mW typ/gate (No Load)
t+, t- = 2.0 ns typ (20% to 80%)

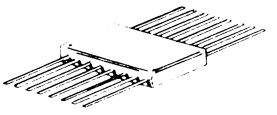
V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10109 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10509 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	16	–	15	–	14	–	15	–	16	mAdc
Input Current	I_{inH}	–	450	–	425	–	265	–	265	–	265	μAdc
Switching Times												ns
Propagation Delay	t_{pd}	1.0	3.7	1.0	3.1	1.0	2.9	1.0	3.3	1.0	3.7	
Rise Time, Fall Time (20% to 80%)	t+, t-	1.0	4.0	1.1	3.6	1.1	3.3	1.1	3.7	1.0	4.0	ns

-55°C and +125°C test values apply to MC105xx devices only.

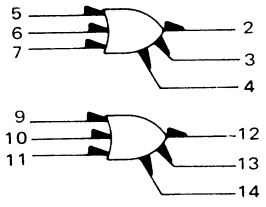
MC10110

DUAL 3-INPUT 3-OUTPUT OR GATE

MC10111

DUAL 3-INPUT 3-OUTPUT NOR GATE

MC10110

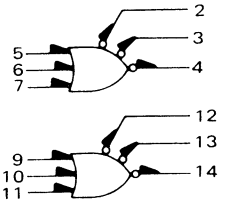


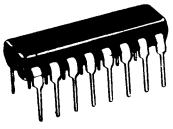
P_D = 80 mW typ/gate (No Load)
t_{pd} = 2.4 ns typ (All Outputs Loaded)
t+, t- = 2.2 ns typ (20% to 80%) (All Outputs Loaded)

V_{CC1} = 1.15
V_{CC2} = 16
V_{EE} = 8

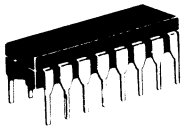
Three V_{CC} pins are provided and each one should be used.

MC10111





P SUFFIX
PLASTIC PACKAGE
CASE 648



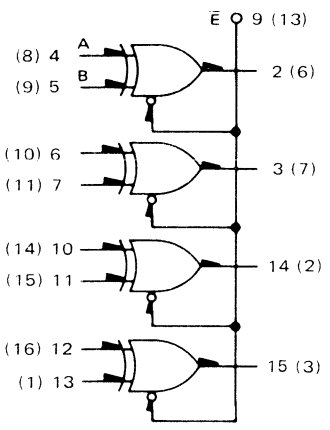
L SUFFIX
CERAMIC PACKAGE
CASE 620

Numbers at ends of terminals denote pin numbers for L and P packages.

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	42	–	38	–	42	mAdc
Input Current	I_{inH}	–	680	–	425	–	425	μAdc
Switching Times								ns
Propagation Delay	t_{pd}	1.4	3.5	1.4	3.5	1.5	3.8	
Rise Time, Fall Time (20% to 80%)	t+, t-	1.0	3.5	1.1	3.5	1.2	3.8	ns

MC10113/MC10513

QUAD EXCLUSIVE OR GATE



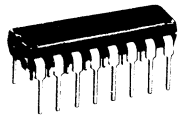
TRUTH TABLE

A	B	Ē	OUTPUT
L	L	L	L
L	H	L	H
H	L	L	H
H	H	L	L
ϕ	ϕ	H	L

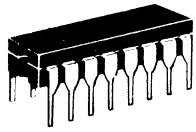
ϕ = Don't Care

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

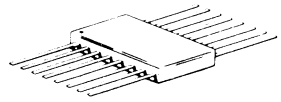
P_D = 175 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ
t^+, t^- = 2.0 ns typ (20% – 80%)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10113 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10513 only

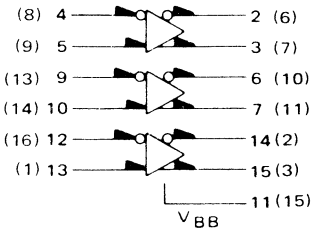
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	46	–	46	–	42	–	46	–	46	mAdc
Input Current	I_{inH}											μAdc
Pins 4, 7, 10, 13		–	450	–	425	–	265	–	265	–	265	
Pins 5, 6, 11, 12		–	375	–	350	–	220	–	220	–	220	
Pin 9		–	925	–	870	–	545	–	545	–	545	
Switching Times												ns
Propagation Delay	t_{pd}											
Independent Inputs		1.1	4.9	1.1	4.7	1.3	4.5	1.3	5.0	1.3	5.3	
Enable Input		1.3	5.2	1.3	5.2	1.5	5.0	1.5	5.5	1.5	5.8	
Rise Time, Fall Time (20% to 80%)	t^+, t^-	1.1	4.3	1.1	4.2	1.1	3.9	1.1	4.4	1.1	4.6	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10114/MC10514

TRIPLE LINE RECEIVER



V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

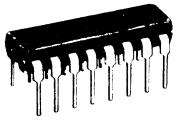
t_{pd} = 2.4 ns typ (Single-Ended Input)
t_{pd} = 2.0 ns typ (Differential Input)
P_D = 145 mW typ/pkg

The MC10114/MC10514 is designed for use in sensing differential signals over long lines. An active current source and translated emitter follower inputs provide the line receiver with a common mode noise rejection limit of one volt in either the positive or the negative direction. This allows a large amount of common mode noise immunity for extra long lines.

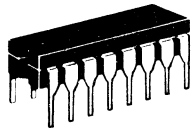
Another feature is that the NOR outputs go to a logic low level whenever the inputs are left floating.

This device is useful in high speed central processors, minicomputers, peripheral controllers, digital communication systems, testing and instrumentation systems. It can also be used for MOS to MECL interfacing and is ideal as a sense amplifier for MOS RAMs.

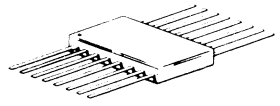
A V_{BB} reference is provided which is useful in making a Schmitt trigger, allowing single-ended driving of the inputs, or other applications where a stable reference voltage is necessary.



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10114 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10514 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

ELECTRICAL CHARACTERISTICS

@ Test Temperature	TEST VOLTAGE VALUES (Volts)									
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{BB}	V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{EE}
MC10114										
-30°C	-0.890	-1.890	-1.205	-1.500	From	+0.110	-0.890	-1.890	-2.890	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	Pin	+0.190	-0.850	-1.810	-2.850	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	11	+0.300	-0.825	-1.700	-2.825	-5.2
MC10514										
-55°C	-0.880	-1.920	-1.255	-1.510	From	+0.120	-0.920	-1.880	-2.920	-5.2
+25°C	-0.780	-1.850	-1.105	-1.475	Pin 11	+0.220	-0.850	-1.780	-2.850	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	(15)	+0.370	-0.820	-1.630	-2.820	-5.2

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Power Supply Drain Current	I_E	–	39	–	39	–	35	–	39	–	39	mAdc	V_{in} = $V_{IH\ max}$ (Pins 4, 9, 12), $V_{IL\ min}$ (Pins 5, 10, 13)
Input Current	I_{inH}	–	80	–	70	–	45	–	45	–	45	μAdc	Test one input at a time. V_{in} = $V_{IH\ max}$ to P.U.T. and $V_{IL\ min}$ to the other input of that gate.
	I_{CBO}	–	1.5	–	1.5	–	1.0	–	1.0	–	1.0	μAdc	Test one input at a time. V_{in} = V_{EE}
Reference Voltage	V_{BB}	-1.440	-1.320	-1.420	-1.280	-1.350	-1.230	-1.295	-1.150	-1.240	-1.120	Vdc	One input from each gate tied to V_{BB} (Pin 11).
Common Mode Rejection Test*													
MC10114	V_{OH}	–	–	-1.060	-0.890	-0.960	-0.810	-0.890	-0.700	–	–	Vdc	V_{in} = V_{IHH} or V_{IHL} to one input of each gate under test and V_{ILH} or V_{ILL}, respectively, to the other input of each gate.
MC10514		-1.080	-0.880	–	–	-0.930	-0.780	–	–	-0.825	-0.630		
MC10114	V_{OL}	–	–	-1.890	-1.675	-1.850	-1.650	-1.825	-1.615	–	–	Vdc	
MC10514		-1.920	-1.655	–	–	-1.850	-1.620	–	–	-1.820	-1.545		
Switching Times													
Propagation Delay	t_{pd}	1.0	4.3	1.0	4.4	1.0	4.0	0.9	4.3	1.0	4.7	ns	For single-ended input testing, one input from each gate must be tied to V_{BB} (Pin 11).
Rise Time, Fall Time	t+, t-	1.3	3.8	1.5	3.8	1.5	3.5	1.5	3.7	1.2	4.1	ns	20% to 80%

*V_{IHH} = Input logic "1" level shifted positive one volt for common mode rejection tests.
V_{ILH} = Input logic "0" level shifted positive one volt for common mode rejection tests.
V_{IHL} = Input logic "1" level shifted negative one volt for common mode rejection tests.
V_{ILL} = Input logic "0" level shifted negative one volt for common mode rejection tests.

-55°C and +125°C test values apply to MC105xx devices only.

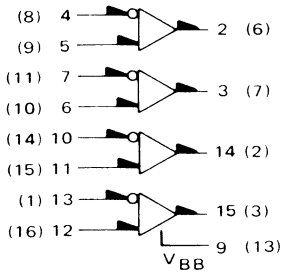
MC10115/MC10515

QUAD LINE RECEIVER

MC10116/MC10516

TRIPLE LINE RECEIVER

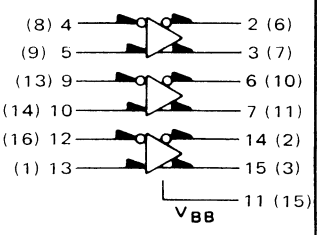
MC10115/MC10515



These receivers are designed for use in sensing differential signals over long lines. The bias supply (V_{BB}) is made available to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

Active current sources provide these receivers with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} to prevent upsetting the current source bias network.

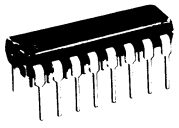
MC10116/MC10516



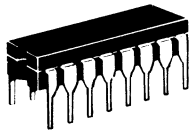
t_{pd} = 2.0 ns typ
P_D = 110 mW typ/pkg (No Load)

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

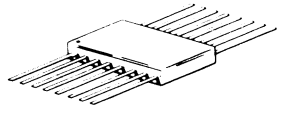
t_{pd} = 2.0 ns typ
P_D = 85 mW typ/pkg (No Load)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10115 and
MC10116 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10515 and
MC10516 only

Numbers at ends of terminals denote pin numbers for L and P package
Numbers in parenthesis denote pin numbers for F package

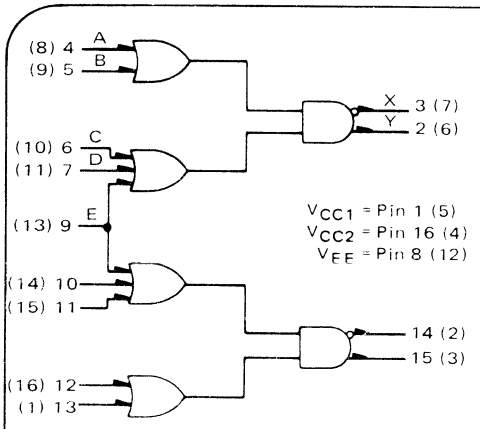
One input from each gate must be tied to V_{BB} during testing.

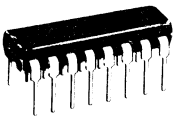
Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E											mAdc
MC10115/10515			29		29		26		29		29	
MC10116/10516			24		23		21		23		24	
Input Current	I_{inH}		165		150		95		95		95	μAdc
	I_{CBO}		1.5		1.5		1.0		1.0		1.0	μAdc
Reference Voltage	V_{BB}	-1.440	-1.320	-1.420	-1.280	-1.350	-1.230	-1.295	-1.150	-1.240	-1.120	Vdc
Switching Times												ns
Propagation Delay	t_{pd}	1.0	3.5	1.0	3.1	1.0	2.9	1.0	3.3	1.0	4.0	
Rise Time, Fall Time (20% to 80%)	t^+, t^-	1.0	3.9	1.1	3.6	1.1	3.3	1.1	3.7	1.0	4.4	ns

55°C and +125°C test values apply to MC105xx devices only.

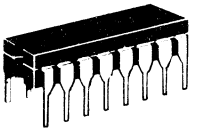
MC10117/MC10517

DUAL 2-WIDE 2-3-INPUT OR-AND/OR-AND-INVERT GATE

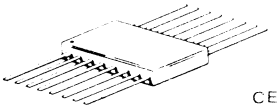




P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10117 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10517 only

P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ
t^+, t^- = 2.2 ns typ (20% to 80%)

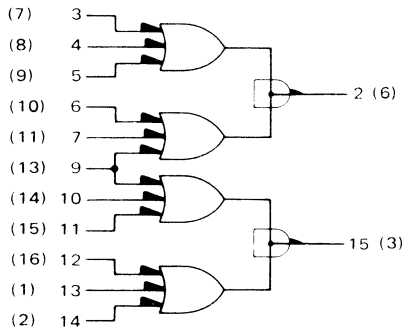
Numbers at ends of terminals denote pin numbers for L and P package
Numbers in parenthesis denote pin numbers for F package

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	29	–	29	–	26	–	29	–	29	mAdc
Input Current	I_{inH}											µAdc
Pins 4, 5, 12, 13		–	415	–	390	–	245	–	245	–	245	
Pins 6, 7, 10, 11		–	450	–	425	–	265	–	265	–	265	
Pin 9		–	595	–	560	–	350	–	350	–	350	
Switching Times												ns
Propagation Delay	t_{pd}	1.1	3.5	1.4	3.9	1.4	3.4	1.4	3.8	1.2	3.5	
Rise Time, Fall Time (20% to 80%)	t^+, t^-	1.0	4.1	0.9	4.1	1.1	4.0	1.1	4.6	0.9	4.1	ns

-55°C and +125°C test values apply to MC105xx devices only.

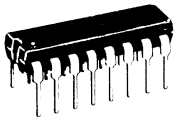
MC10118/MC10518

DUAL 2-WIDE 3-INPUT OR-AND GATE

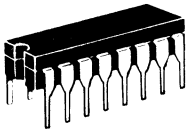


P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ
t+, t− = 2.5 ns typ (20% to 80%)

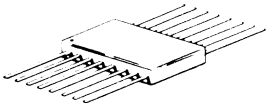
V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10118 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10518 only

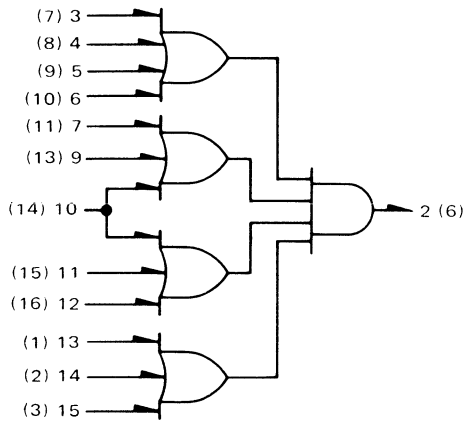
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	29	–	29	–	26	–	29	–	29	mAdc
Input Current	I_{inH}											μAdc
Pins 3, 4, 5, 12, 13, 14		–	415	–	390	–	245	–	245	–	245	
Pins 6, 7, 10, 11		–	450	–	425		265	–	265	–	265	
Pin 9		–	595	–	560	–	350	–	350	–	350	
Switching Times												ns
Propagation Delay	t_{pd}	1.1	3.5	1.4	3.9	1.4	3.4	1.4	3.8	1.2	3.5	
Rise Time, Fall Time (20% to 80%)	t^+, t^-	1.3	4.1	0.8	4.1	1.5	4.0	1.5	4.6	1.2	4.0	

55°C and +125°C test values apply to MC105xx devices only.

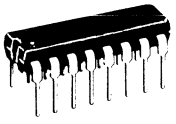
MC10119/MC10519

4-WIDE 4-3-3-3-INPUT OR-AND GATE

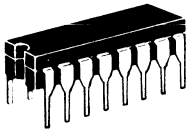


V_{CC1} = 1 (5)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)

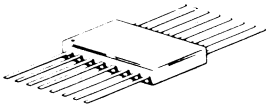
P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ
t^+, t^- = 2.5 ns typ (20% to 80%)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10119 only



L SUFFIX
CERAMIC PACKAGE
CASE 620

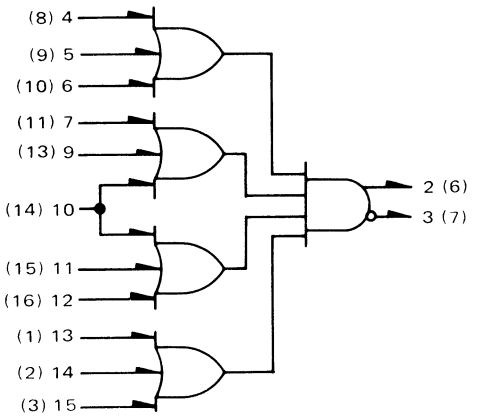


F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10519 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

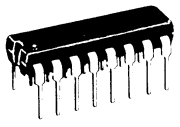
Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	29	–	29	–	26	–	29	–	29	mAdc
Input Current	I_{inH}											μAdc
Pins 3, 4, 5, 6, 7, 9, 11, 12, 13, 14, 15		–	415	–	390	–	245	–	245	–	245	
Pin 10		–	525	–	495	–	310	–	310	–	310	
Switching Times												ns
Propagation Delay	t_{pd}	1.1	3.5	1.4	3.9	1.4	3.4	1.4	3.8	1.2	3.5	
Rise Time, Fall Time (20% to 80%)	t^+, t^-	1.3	4.1	0.8	4.1	1.5	4.0	1.5	4.6	1.2	4.3	ns

-55°C and +125°C test values apply to MC105xx devices only.

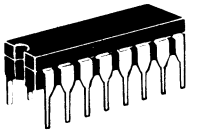


V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

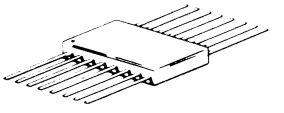
P_D = 100 mW typ/pkg (No Load)
t_{pd} = 2.3 ns typ
t^+, t^- = 2.5 ns typ (20% to 80%)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10121 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10521 only

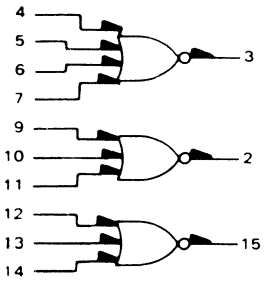
Numbers at ends of terminals denote pin number for L and P package
Numbers in parenthesis denote pin numbers for F package

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	29	–	29	–	26	–	29	–	29	mAdc
Input Current	I_{inH}											μAdc
Pins 3, 4, 5, 6, 7, 9, 11, 12, 13, 14, 15		–	415	–	390	–	245	–	245	–	245	
Pin 10		–	525	–	495	–	310	–	310	–	310	
Switching Times												ns
Propagation Delay	t_{pd}	1.2	3.6	1.4	3.9	1.4	3.4	1.4	3.8	1.1	3.5	
Rise Time, Fall Time (20% to 80%)	t^+, t^-	1.0	4.5	0.9	4.1	1.1	4.0	1.1	4.6	0.9	4.4	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10123

TRIPLE 4-3-3 INPUT BUS DRIVER



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

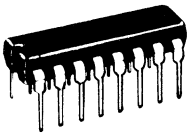
P_D = 310 mW typ/pkg (No Load)

t_{pd} = 3.0 ns typ

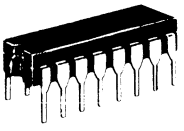
t_+, t_- = 2.5 ns typ (20% to 80%)

The MC10123 consists of three NOR gates designed for bus driving applications on card or between cards. Output low logic levels are specified with $V_{OL} \leq -2.0$ Vdc so that the bus may be terminated to −2.0 Vdc. The gate output, when low, appears as a high impedance to the bus, because the output emitter-followers of the MC10123 are "turned-off". This eliminates discontinuities in the characteristic impedance of the bus.

The V_{OH} level is specified when driving a 25-ohm load terminated to −2.0 Vdc, the equivalent of a 50-ohm bus terminated at both ends. Although 25 ohms is the lowest characteristic impedance that can be driven by the MC10123, higher impedance values may be used with this part. A typical 50-ohm bus is shown in Figure 1.

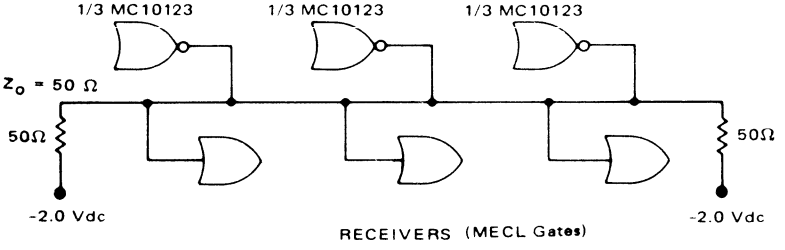


P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

FIGURE 1 – 50-OHM BUS DRIVER

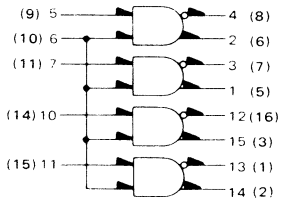


Outputs are terminated through a 25-ohm resistor to −2.1 volts.

Characteristic	Symbol	−30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	82	–	75	–	82	mAdc
Input Current	I_{inH}	–	350	–	220	–	220	μAdc
Logic "0" Output Voltage	V_{OL}	-2.100	-2.030	-2.100	-2.030	-2.100	-2.030	Vdc
Logic "0" Threshold Voltage	V_{OLA}	–	-2.010	–	-2.010	–	-2.010	Vdc
Switching Times								ns
Propagation Delay	tpd	1.2	4.6	1.2	4.4	1.2	4.8	
Rise Time, Fall Time (20% to 80%)	t_-, t_+	1.0	3.7	1.0	3.5	1.0	3.9	ns

MC10124/MC10524

QUAD TTL-TO-MECL TRANSLATOR



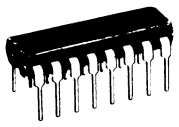
Gnd = Pin 16 (4)
V_{CC} (+5.0 Vdc) = Pin 9 (13)
V_{EE} (−5.2 Vdc) = Pin 8 (12)
V_{CCmax} = 7.0 Vdc

P_D = 380 mW typ/pkg (No Load)
t_{pd} = 3.5 ns typ (+1.5 Vdc in to 50% out)
t+, t− = 2.5 ns typ (20% to 80%)

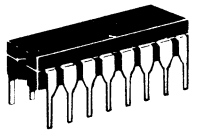
The MC10124/MC10524 is a quad translator for interfacing data and control signals between a saturated logic section and the MECL section of digital systems. The device has TTL compatible inputs, and MECL complementary open-emitter outputs that allow use as an inverting/non-inverting translator or as a differential line driver. When the common strobe input is at the low logic level, it forces all true outputs to a MECL low logic state and all inverting outputs to a MECL high logic state.

Power supply requirements are ground, +5.0 Volts, and −5.2 Volts. The dc levels are standard or Schottky TTL in, MECL 10,000 out.

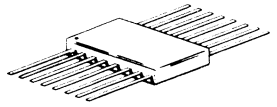
An advantage of this device is that TTL level information can be transmitted differentially, via balanced twisted pair lines, to the MECL equipment, where the signal can be received by any of the MECL line receivers or the MC10125 MECL to TTL translator or the MC10177 MECL to MOS translator.



P SUFFIX
CERAMIC PACKAGE
CASE 648
MC10124 only



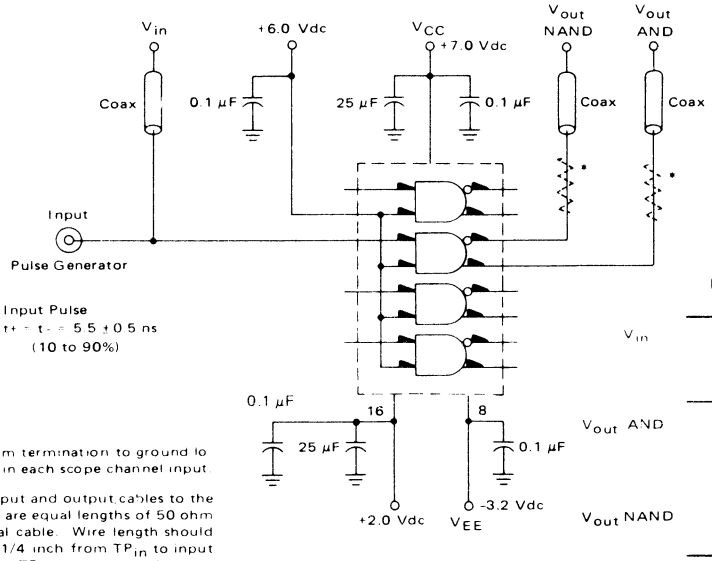
L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10524 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



NOTE: All power supply and logic levels are shown shifted 2 volts positive.

ELECTRICAL CHARACTERISTICS

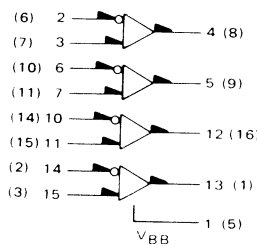
@ Test Temperature	TEST VOLTAGE/CURRENT VALUES								
	Volts							mA	
	V_{IHmin}	V_{ILmax}	V_{RH}	V_F	V_R	V_{CC}	V_{EE}	I_{I1}	I_{I2}
MC10124									
-30°C	+2.0	+1.1	+4.0	+0.4	+2.4	+5.0	-5.2	-10	-20
+25°C	+1.8	+1.1	+4.0	+0.4	+2.4	+5.0	-5.2	-10	-20
+85°C	+1.8	+0.8	+4.0	+0.4	+2.4	+5.0	-5.2	-10	-20
MC10524									
-55°C	+2.0	+1.1	+4.0	+0.4	+2.4	+5.0	-5.2	-10	-20
+25°C	+1.8	+1.1	+4.0	+0.4	+2.4	+5.0	-5.2	-10	-20
+125°C	+1.8	+0.8	+4.0	+0.4	+2.4	+5.0	-5.2	-10	-20

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Negative Power Supply Drain Current	I_E	–	72	–	72	–	66	–	72	–	72	mAdc	All inputs and outputs open.
Positive Power Supply Drain Current	I_{CCH}	–	16	–	16	–	16	–	18	–	18	mAdc	$V_{in} = V_{RH}$ all inputs.
	I_{CCL}	–	25	–	25	–	25	–	25	–	25	mAdc	V_{in} (strobe) = V_F
Reverse Current Strobe Input	I_R	–	200	–	200	–	200	–	200	–	200	μAdc	$V_{in} = V_R$ (strobe), V_F (single inputs)
Single Inputs		–	50	–	50	–	50	–	50	–	50		$V_{in} = V_F$ (strobe), V_R (P.U.T.)
Forward Current Strobe Input	I_F	–	-12.8	–	-12.8	–	-12.8	–	-12.8	–	-12.8	mAdc	$V_{in} = V_F$ (strobe), V_R (single inputs)
Single Inputs		–	-3.2	–	-3.2	–	-3.2	–	-3.2	–	-3.2		$V_{in} = V_R$ (strobe), V_F (P.U.T.)
Input Breakdown Voltage	BV_{in}	5.5	–	5.5	–	5.5	–	5.5	–	5.5	–	Vdc	At I_{in} = +1.0 mAdc. V_{in} (strobe) = V_F while testing single inputs.
Clamp Input Voltage	V_I	–	-1.5	–	-1.5	–	-1.5	–	-1.5	–	-1.5	Vdc	Test one input at a time. I_{I1} (single inputs), I_{I2} (strobe).
Switching Times Propagation Delay	t_{pd}	1.0	8.0	1.0	6.8	1.0	6.0	1.0	6.8	1.0	8.0	ns	+1.5 Vdc in to 50% out
Rise Time, Fall Time	t+, t-	1.0	4.5	1.0	4.2	1.1	3.9	1.1	4.3	1.0	4.5		20% to 80%

-55°C and +125°C test values apply to MC105XX devices only.

MC10125/MC10525

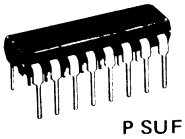
QUAD MECL-TO-TTL TRANSLATOR



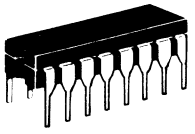
Gnd = Pin 16 (4)
V_{CC} (+5.0 Vdc) = Pin 9 (13)
V_{EE} (−5.2 Vdc) = Pin 8 (12)

P_D = 380 mW typ/pkg (No Load)
t_{pd} = 4.5 ns typ (50% to +1.5 Vdc out)
t+, t− = 2.5 ns typ (1 V to 2 V)

V_{CCmax} = +7.0 Vdc



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10125 only

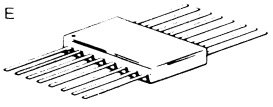


L SUFFIX
CERAMIC PACKAGE
CASE 620

The MC10125/MC10525 is a quad translator for interfacing data and control signals between the MECL section and saturated logic sections of digital systems. The MC10125 incorporates differential inputs and Schottky TTL "totem pole" outputs. Differential inputs allow for use as an inverting/non-inverting translator or as a differential line receiver. The V_{BB} reference voltage is availabe on pin 1 for use in single-ended input biasing. The outputs go to a low logic level whenever the inputs are left floating.

Power supply requirements are ground, +5.0 Volts and −5.2 Volts. The MC10125 has a fanout of 10 TTL loads. The dc levels are MECL 10,000 in and Schottky TTL or standard TTL out. This device has an input common mode noise rejection of ± 1.0 Volt.

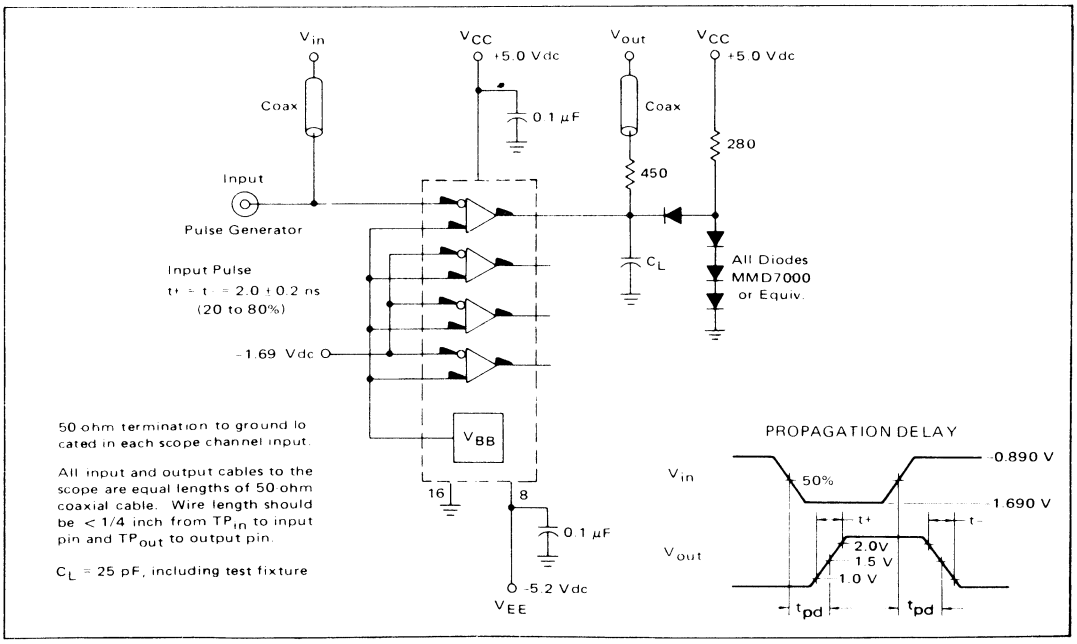
An advantage of this device is that MECL level information can be received, via balanced twisted pair lines, in the TTL equipment. This isolates the MECL logic from the noisy TTL environment.



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10525 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



ELECTRICAL CHARACTERISTICS

@ Test Temperature	TEST VOLAGE AND CURRENT VALUES												
	Volts											mA	
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{BB}	V_{CC}	V_{EE}	I_{OH}	I_{OL}
MC10125													
-30°C	-0.890	-1.890	-1.205	-1.500	+0.110	-0.890	-1.890	-2.890	From	+5.0	-5.2	-2.0	+20
+25°C	-0.810	-1.850	-1.105	-1.475	+0.190	-0.850	-1.810	-2.850	Pin	+5.0	-5.2	-2.0	+20
+85°C	-0.700	-1.825	-1.035	-1.440	+0.300	-0.825	-1.700	-2.825	1	+5.0	-5.2	-2.0	+20
MC10525													
-55°C	-0.880	-1.920	-1.255	-1.510	+0.120	-0.920	-1.880	-2.920	From	+5.0	-5.2	-2.0	+12
+25°C	-0.780	-1.850	-1.105	-1.475	+0.220	-0.850	-1.780	-2.850	Pin	+5.0	-5.2	-2.0	+12
+125°C	-0.630	-1.820	-1.000	-1.400	+0.370	-0.820	-1.630	-2.820	1	+5.0	-5.2	-2.0	+12

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Negative Power Supply Drain Current	I_E	–	44	–	44	–	40	–	44	–	44	mAdc	$V_{in} = V_{BB}$ (Pins 3, 7, 11, 15), V_{EE} (Pins 2, 6, 10, 14)
Positive Power Supply Drain Current	I_{CCH}	–	52	–	52	–	52	–	52	–	52	mAdc	$V_{in} = V_{BB}$ (Pins 3, 7, 11, 15), $V_{IH\ max}$ (Pins 2, 6, 10, 14)
	I_{CCL}	–	39	–	39	–	39	–	39	–	39	mAdc	$V_{in} = V_{BB}$ (Pins 3, 7, 11, 15), V_{EE} (Pins 2, 6, 10, 14)
Input Current	I_{inH}	–	195	–	180	–	115	–	115	–	115	μAdc	One input from each gate tied to V_{BB} while the other inputs are tested one at a time, $V_{in} = V_{IH}$ max.
Input Leakage Current	I_{CBO}	–	1.5	–	1.5	–	1.0	–	1.0	–	1.0	μAdc	One input from each gate tied to V_{BB} while the other inputs are tested one at a time, $V_{in} = V_{EE}$.
Short-Circuit Current	I_{OS}	40	100	40	100	40	100	40	100	40	100	mA	$V_{in} = V_{BB}$ (Pins 3, 7, 11, 15), $V_{IL\ min}$ (Pins 2, 6, 10, 14). Connect outputs to ground, one at a time.

-55°C and +125°C test values apply to MC105XX devices only.

(continued on next page)

ELECTRICAL CHARACTERISTICS (continued)

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
High Output Voltage	V_{OH}	2.5	–	2.5	–	2.5	–	2.5	–	2.5	–	Vdc	$V_{in} = V_{IL\ min}$ (Pins 2, 6, 10, 14), $V_{IH\ max}$ (Pins 3, 7, 11, 15).
Low Output Voltage	V_{OL}	–	0.5	–	0.5	–	0.5	–	0.5	–	0.5	Vdc	$V_{in} = V_{IL\ min}$ (Pins 3, 7, 11, 15), $V_{IH\ max}$ (Pins 2, 6, 10, 14).
High Threshold Voltage	V_{OHA}	2.5	–	2.5	–	2.5	–	2.5	–	2.5	–	Vdc	$V_{in} = V_{BB}$ (Pins 3, 7, 11, 15), $V_{ILA\ max}$ (Pins 2, 6, 10, 14, one at a time).
Low Threshold Voltage	V_{OLA}	–	0.5	–	0.5	–	0.5	–	0.5	–	0.5	Vdc	$V_{in} = V_{BB}$ (Pins 3, 7, 11, 15), $V_{IHA\ max}$ (Pins 2, 6, 10, 14, one at a time).
Indeterminate Input Protection Tests	V_{OLS1}	–	0.5	–	0.5	–	0.5	–	0.5	–	0.5	Vdc	$V_{in} = V_{EE}$ to both inputs of each gate, one gate at a time.
	V_{OLS2}	–	0.5	–	0.5	–	0.5	–	0.5	–	0.5	Vdc	All inputs open.
Reference Voltage	V_{BB}	−1.440	−1.320	−1.420	−1.280	−1.350	−1.230	−1.295	−1.150	−1.240	−1.120	Vdc	One input from each gate tied to V_{BB} (Pin 1).
Common Mode Rejection Tests*	V_{OH}	2.5	–	2.5	–	2.5	–	2.5	–	2.5	–	Vdc	$V_{in} = V_{IHH}$ or V_{IHL} to one input of each gate under test and V_{ILH} or V_{ILL}, respectively, to the other input of each gate.
	V_{OL}	–	0.5	–	0.5	–	0.5	–	0.5	–	0.5	Vdc	
Switching Times Propagation Delay	t_{pd}	1.0	6.5	1.0	6.0	1.0	6.0	1.0	6.0	1.0	7.0	ns	50% in to +1.5 Vdc out. For single-ended input testing, one input from each gate must be tied to V_{BB} (Pin 1).
Rise Time, Fall Time	t+, t−	–	4.5	–	3.3	–	3.3	–	3.3	–	5.3	ns	+1.0 Vdc to +2.0 Vdc

*V_{IHH} = Input logic "1" level shifted positive one volt for common mode rejection tests.
V_{ILH} = Input logic "0" level shifted positive one volt for common mode rejection tests.
V_{IHL} = Input logic "1" level shifted negative one volt for common mode rejection tests.
V_{ILL} = Input logic "0" level shifted negative one volt for common mode rejection tests.

−55°C and +125°C test values apply to MC105XX devices only.

MC10128

DUAL BUS DRIVER
(MECL 10,000 TO TTL/IBM)

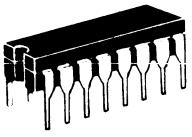
The MC10128 is designed to provide outputs which are compatible with IBM-type bus levels; or, if desired, it will drive TTL type loads and/or provide TTL three-state outputs. The inputs accept MECL 10,000 levels. The MC10128 output levels can be accepted by the MC10129 Bus Receiver.

The operating mode (IBM or TTL) is selected by tying the external control pins to ground or leaving them open. Leaving a control pin open selects the TTL mode, and tying a control pin to ground selects the IBM mode.

The TTL mode will drive a 25-ohm load, terminated to +1.5 Vdc or a 50-ohm load, terminated to ground. The device has totem-pole type outputs, but it also has a disable input for three-state logic operation when the circuit is used in the TTL mode. When in the high state the disable input causes the output to exhibit a high impedance state when it would normally be a positive logic "1" state. When the strobe is in the high state it inhibits the output data to the low state.

Latches are provided on each data input for temporary storage. When the clock input is in the low logic state, information present at the data inputs D1 and D2 will be fed directly to the latch output. When the clock goes high, the input data is latched. The outputs are gated to allow full bus driving and strobing capability.

The MC10128 is useful in interfacing and bus applications in central processors, minicomputers, and peripheral equipment.

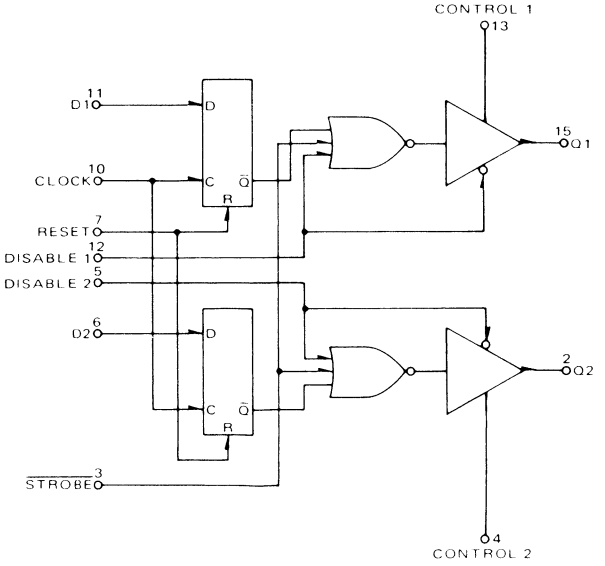


L SUFFIX
CERAMIC PACKAGE
CASE 620

V_{CC} = Pin 14
Gnd 1 = Pin 16
Gnd 2 = Pin 1
Gnd 3 = Pin 9
V_{EE} = Pin 8

P_D = 700 mW pkg/typ (No Load)
t_{pd} = 12 ns typ

V_{CC} Max = +7.0 Vdc



TTL MODE

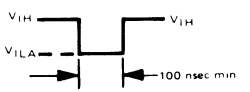
TEST VOLTAGE/CURRENT VALUES

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{CC}	mAdc I_{OH1}	μAdc I_{OH2}	mAdc I_{OL}
–30°C	-0.890	-1.890	-1.205	-1.500	-5.2	+5.00	-50	-100	+56
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	+5.00	-50	-100	+56
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	+5.00	-50	-100	+56

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	Conditions
Negative Power Supply Drain Current	I_E	–	–	–	91	–	–	mAdc	V_{IHmax} to Data Inputs (Pins 6 and 11)
Positive Power Supply Drain Current	I_{CC}	–	–	–	50	–	–	mAdc	
Input Leakage Current	I_{inH}							μAdc	Test one input at a time. V_{IHmax} to P.U.T.
Pin 3		–	–	–	620	–	–		
Pin 7		–	–	–	350	–	–		
Pins 6, 10, 11		–	–	–	265	–	–		
Pins 5, 12		–	–	–	485	–	–		
Logic "1" Output Voltage	V_{OH}	–	–	2.5	–	–	–	Vdc	V_{IHmax} to Data Inputs, $I_{out} = I_{OH1}$
		–	–	2.7	–	–	–		V_{IHmax} to Data Inputs, $I_{out} = I_{OH2}$
Logic "0" Output Voltage	V_{OL}	–	–	–	0.5	–	–	Vdc	V_{IHmax} to Strobe Input, $I_{out} = I_{OL}$
Logic "1" Threshold Voltage	V_{OHA}	–	–	2.5	–	–	–	Vdc	V_{IHmax} to Data Inputs, apply pulse ①, or V_{IHAmin} to Data Inputs (one at a time.)
Logic "0" Threshold Voltage	V_{OLA}	–	–	–	0.5	–	–	Vdc	V_{ILAmax} to Data Inputs (one at a time), or V_{IHmax} to Data Inputs and V_{IHAmin} to Strobe.
Output Short Circuit Current	I_{SC}	–	–	–	260	–	–	mAdc	V_{IHmax} to Data Inputs, connect outputs to ground (one at a time).
Switching Times								ns	50% in to +1.5 V out. See switching circuit and waveforms.
Propagation Delay	tpd								
Data, $\overline{\text{Strobe}}$		–	–	1.0	18	–	–		
Clock, Reset		–	–	1.0	20	–	–		
Setup Time	t_{set}	–	–	–	–	–	–	ns	
Hold Time	t_{hold}	–	–	–	–	–	–	ns	
Rise Time, Fall Time	t+,t–	–	–	–	8.0	–	–	ns	+1.0 Vdc to +2.0 Vdc.

① A pulse is applied to pin 10.



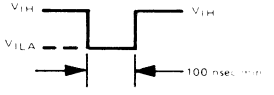
IBM MODE

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES								
	TEST VOLTAGE VALUES						mAdc	μAdc	
	Volts								
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{CC}	I_{OH1}	I_{OH2}	I_{OL}
−30°C	-0.890	-1.890	-1.205	-1.500	-5.2	+6.00	-59.3	-30	-240
+25°C	-0.810	-1.850	-1.105	-1.475	-5.2	+6.00	-59.3	-30	-240
+85°C	-0.700	-1.825	-1.035	-1.440	-5.2	+6.00	-59.3	-30	-240

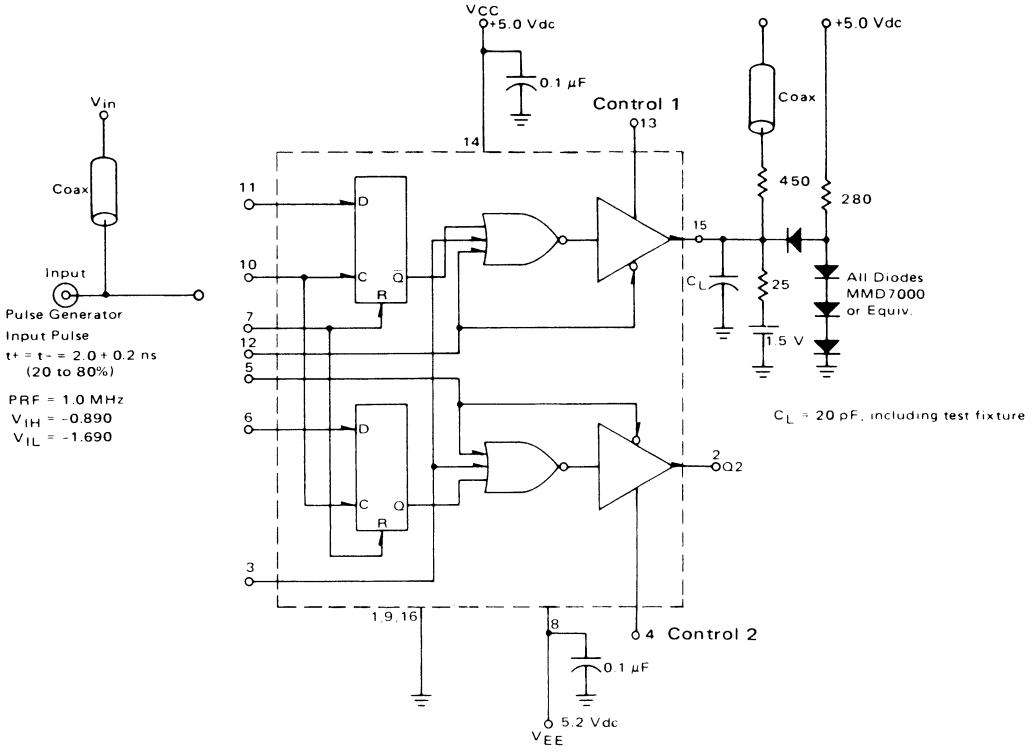
ELECTRICAL CHARACTERISTIC

Characteristic	Symbol	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	Conditions
Negative Power Supply Drain Current	I_E	–	–	–	97	–	–	mAdc	V_{IHmax} to Data Inputs (Pins 6 and 11).
Positive Power Supply Drain Current	I_{CC}	–	–	–	73	–	–	mAdc	V_{IHmax} to $\overline{\text{Strobe}}$ Input (Pin 3).
Input Leakage Current	I_{inH}							μAdc	Test one input at a time. V_{IHmax} to P.U.T.
Pin 3		–	–	–	620	–	–		
Pin 7		–	–	–	350	–	–		
Pins 6, 10, 11		–	–	–	265	–	–		
Pins 5, 12		–	–	–	485	–	–		
Logic "1" Output Voltage	V_{OH}	–	–	3.11	–	–	–	Vdc	V_{IHmax} to Data Inputs, $I_{out} = I_{OH1}$
		–	–	–	5.85	–	–		V_{IHmax} to Data Inputs, $I_{out} = I_{OH2}$
Logic "0" Output Voltage	V_{OL}	–	–	-0.5	0.15	–	–	Vdc	V_{IHmax} to $\overline{\text{Strobe}}$ Input, $I_{out} = I_{OL}$
Logic "1" Threshold Voltage	V_{OHA}	–	–	–	2.9	–	–	Vdc	V_{IHmax} to Data Inputs, apply pulse (1), or V_{IHAmin} to Data Inputs (one at a time).
Logic "0" Threshold Voltage	V_{OLA}	–	–	-0.5	0.15	–	–	Vdc	V_{ILAmax} to Data Inputs (one at a time), or V_{IHmax} to Data Inputs and V_{IHAmin} to $\overline{\text{Strobe}}$.
Output Short Circuit Current	I_{SC}	–	–	–	320	–	–	mAdc	V_{IHmax} to Data Inputs, connect outputs to ground (one at a time).
Switching Times									
Propagation Delay	tpd							ns	50% in to +1.5 V out. See switching circuit and waveforms.
Data, $\overline{\text{Strobe}}$		–	–	1.0	23	–	–		
Clock, Reset		–	–	1.0	23	–	–		
Setup Time	t_{set}	–	–	–	–	–	–	ns	
Hold Time	t_{hold}	–	–	–	–	–	–	ns	
Rise Time, Fall Time	t+,t-	–	–	–	8.0	–	–	ns	+1.0 Vdc to +2.0 Vdc

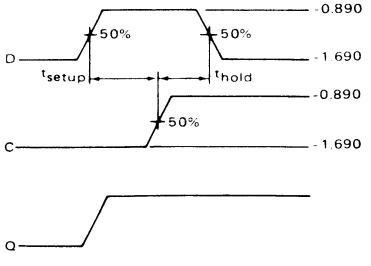
(1) A pulse is applied to pin 10.



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C – TTL MODE



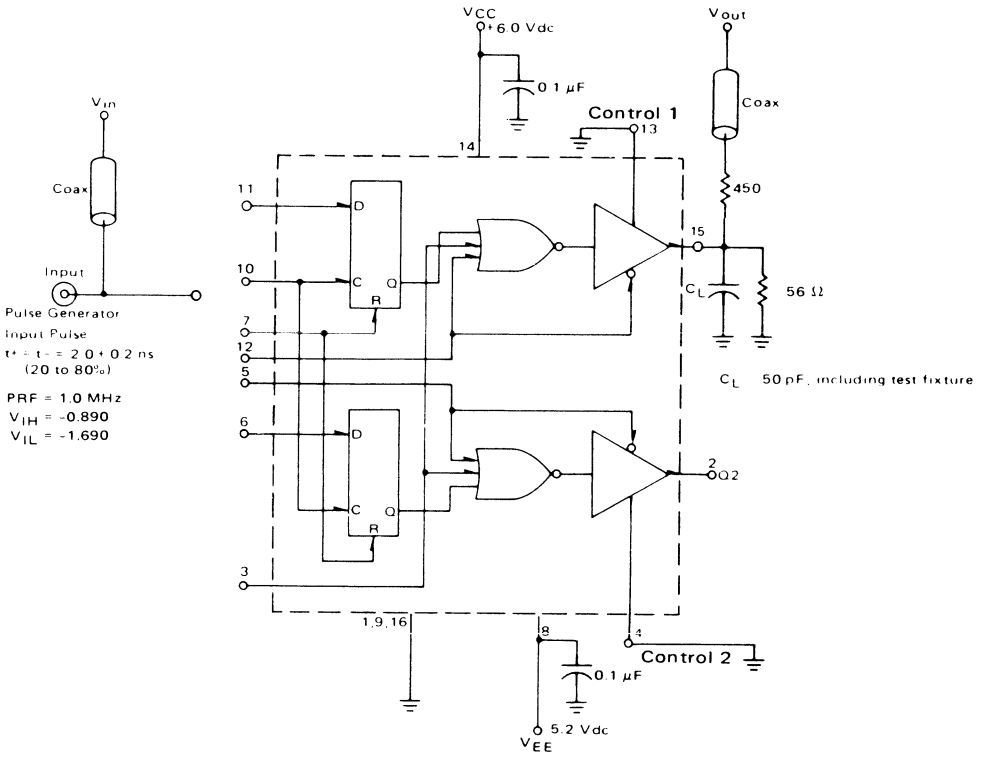
Control pins open for TTL Mode



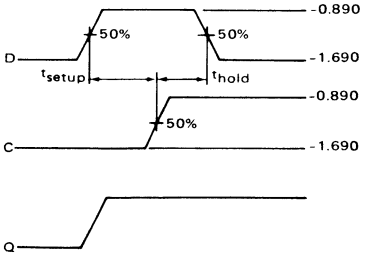
50 ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C – IBM MODE



Control pins grounded for IBM Mode

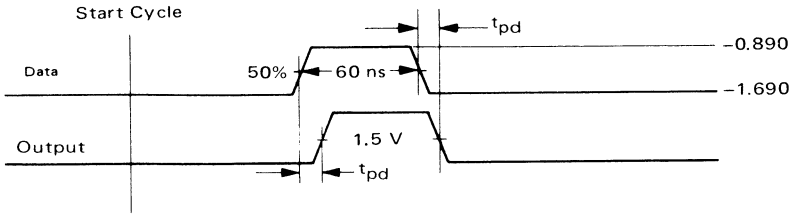


50-ohm termination to ground located in each scope channel input.

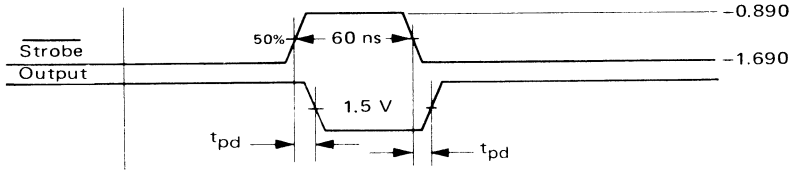
All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

SWITCHING WAVEFORMS

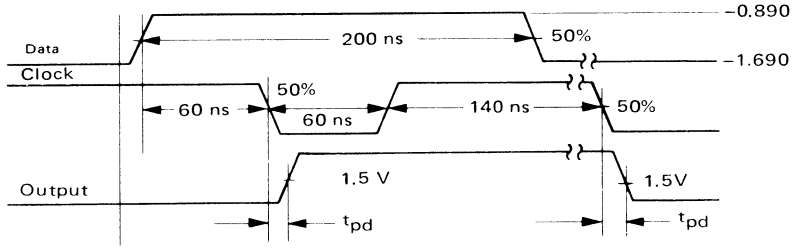
DATA INPUT



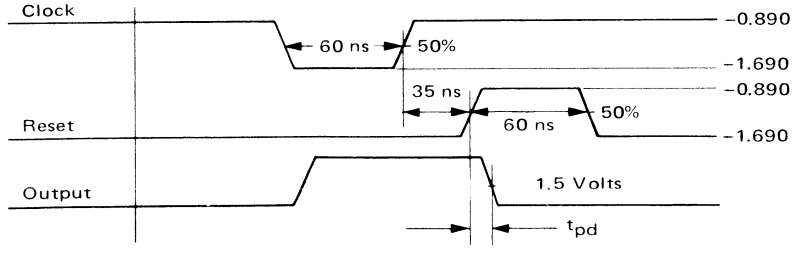
STROBE INPUT



CLOCK INPUT



RESET INPUT



TTL – MODE
V_{OL} = 0.5 Volts Max
V_{OH} = 2.5 Volts Min

IBM – MODE
V_{OL} = 0.15 Volts Max
V_{OH} = 3.11 Volts Min

MC10129

QUAD BUS RECEIVER (TTL/IBM TO MECL 10,000)

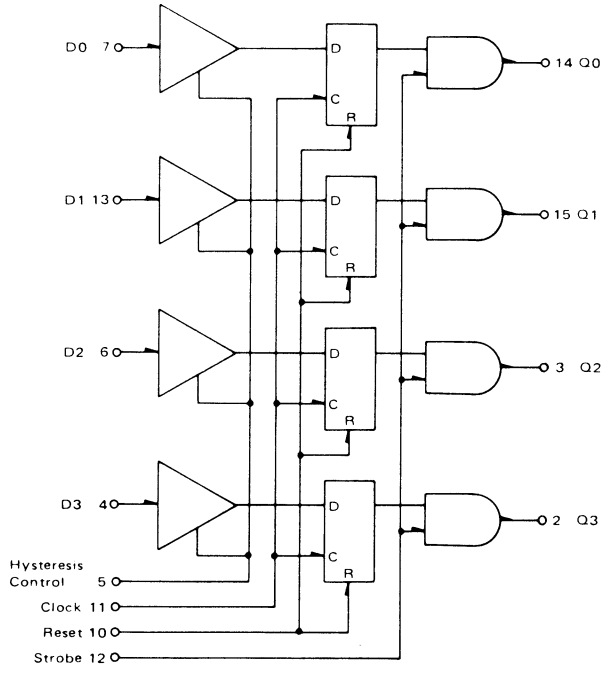
The MC10129 bus receiver works in conjunction with the MC10128 to allow interfacing of MECL 10,000 to other forms of logic and logic buses. The data inputs are compatible with, and accept TTL logic levels as well as levels compatible with IBM-type buses. The clock, strobe, and reset inputs accept MECL 10,000 logic levels.

The data inputs include internal latches to provide temporary storage of the information after receiving it from the bus. The outputs can be strobed to allow accurate synchronization of signals and/or connection to MECL 10,000 level buses. When the clock is low, the outputs will follow the D inputs, and the reset input is disabled. The latches will store the data on the rising edge of the clock. The outputs are enabled when the strobe input is high. Unused D inputs must be tied to V_{CC} or Gnd. The clock, strobe, and reset inputs each have 50k ohm pulldown resistors to V_{EE}. Clock and reset may be left floating, if not used. Strobe should be tied to V_{OH} if unused.

The MC10129 will operate in either of two modes. The first mode is obtained by tying the hysteresis control input to V_{EE}. In this mode, the input threshold points of the D inputs are fixed. The second mode is obtained by tying the hysteresis control input to ground. In this mode, input hysteresis is achieved as shown in the test table. This hysteresis is desirable where extra noise margin is required on the D inputs. The other input pins are unaffected by the mode of operation used.

The outputs are standard MECL 10,000 logic levels regardless of input levels or mode of operation used.

The MC10129 is especially useful in interface applications for central processors, minicomputers, and peripheral equipment.



TRUTH TABLE

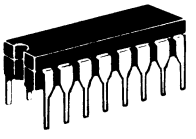
D	C	STROBE	RESET	Q_{n+1}
ϕ	ϕ	L	ϕ	L
ϕ	H	ϕ	H	L
L	L	H	ϕ	L
ϕ	H	H	L	Q_n
H	L	H	ϕ	H

ϕ = Don't Care

P_D = 750 mW typ/pkg (No Load)
t_{pd} = 10 ns typ

V_{CC} Max = +7.0 Vdc

V_{CC} = Pin 9
Gnd = Pins 1 and 16
V_{EE} = Pin 8



L SUFFIX
CERAMIC PACKAGE
CASE 620

	TEST VOLTAGE VALUES (Volts)																	
	MECL 10,000 INPUT LEVELS				*MTTL INPUT LEVELS (1)				*IBM INPUT LEVELS (1)				HYSTERESIS MODE INPUT LEVELS (2)					
@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	$V_{IHA'}$	$V_{ILA'}$	V_{IH}	V_{IL}	$V_{IHA'}$	$V_{ILA'}$	$V_{IHA''}$	$V_{ILA''}$	$V_{IHA'''}$	$V_{ILA'''}$	V_{CC} (3)	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	3.000	0.400	2.000	0.800	3.11	0.150	–	–	2.900	2.000	2.200	1.300	+5.0	-5.2
+25°C	-0.810	-1.850	-1.105	-1.475	3.000	0.400	2.000	0.800	3.11	0.150	1.700	1.10	2.600	1.700	1.900	1.000	+5.0	-5.2
+85°C	-0.700	-1.825	-1.035	-1.440	3.000	0.400	2.000	0.800	3.11	0.150	–	–	2.300	1.400	1.600	0.700	+5.0	-5.2

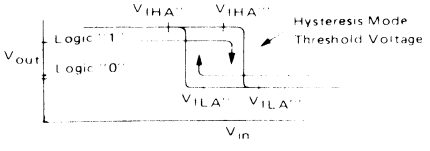
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	Conditions
Negative Power Supply Drain Current	I_E	–	167	–	152	–	167	mAdc	Pin 5 grounded, V_{IH} to Clock, Reset open, V_{IL} to all other inputs.
		–	189	–	172	–	189	mAdc	Pin 5 to V_{EE}, V_{IH} to Clock, Reset open, V_{IL} to all other inputs.
Positive Power Supply Drain Current	I_{CC}	–	8.0	–	8.0	–	8.0	mAdc	Pin 5 to V_{EE}, V_{IL} to Data inputs.
Input Current	I_{inH}							μAdc	Pin 5 to V_{EE}, V_{IH} to P.U.T., one input at a time.
Data			150		95	–	95		
Reset		–	720	–	450	–	450		
Clock, Strobe			390		245		245		
Data	I_{CBO}	–	1.5	–	1.0	–	1.0	μAdc	Pin 5 to V_{EE}, V_{IL} to Data inputs, one at a time.
Reset, Clock, Strobe	I_{inL}	0.5	–	0.5	–	0.3	–	μAdc	Pin 5 to V_{EE}, V_{IL} to P.U.T., V_{IH} to all other inputs.
Switching Times (See Figures 1 thru 5)									
Propagation Delay	t_{pd}							ns	
Data t++		6.0	20	6.6	20	6.6	30		1.5 Vdc in to 50% out.
t--		3.7	15	3.7	15	3.7	40		
Clock		2.7	11	2.7	9.0	2.7	11		50% to 50%
Strobe		1.6	8.0	1.6	7.0	1.6	8.0		
Reset		2.0	8.0	2.0	6.5	2.0	8.0		
Rise Time, Fall Time	t_+, t_-	1.5	5.0	1.5	4.3	1.5	5.0	ns	20% to 80%
Setup Time	t_{set}	27	–	20	–	27	–	ns	50% to 50%
Hold Time	t_{hold}	0	–	-2.0		-2.0	–	ns	
Hysteresis Mode Propagation Delay	t_{pd}							ns	
Data t++		6.6	30	6.7	25	6.6	30		1.5 Vdc in to 50% out.
t--		3.7	17	3.7	15	3.7	40		
Setup Time	t_{set}	30	–	25		30	–	ns	50% to 50%
Hold Time	t_{hold}	0		2.0		2.0		ns	

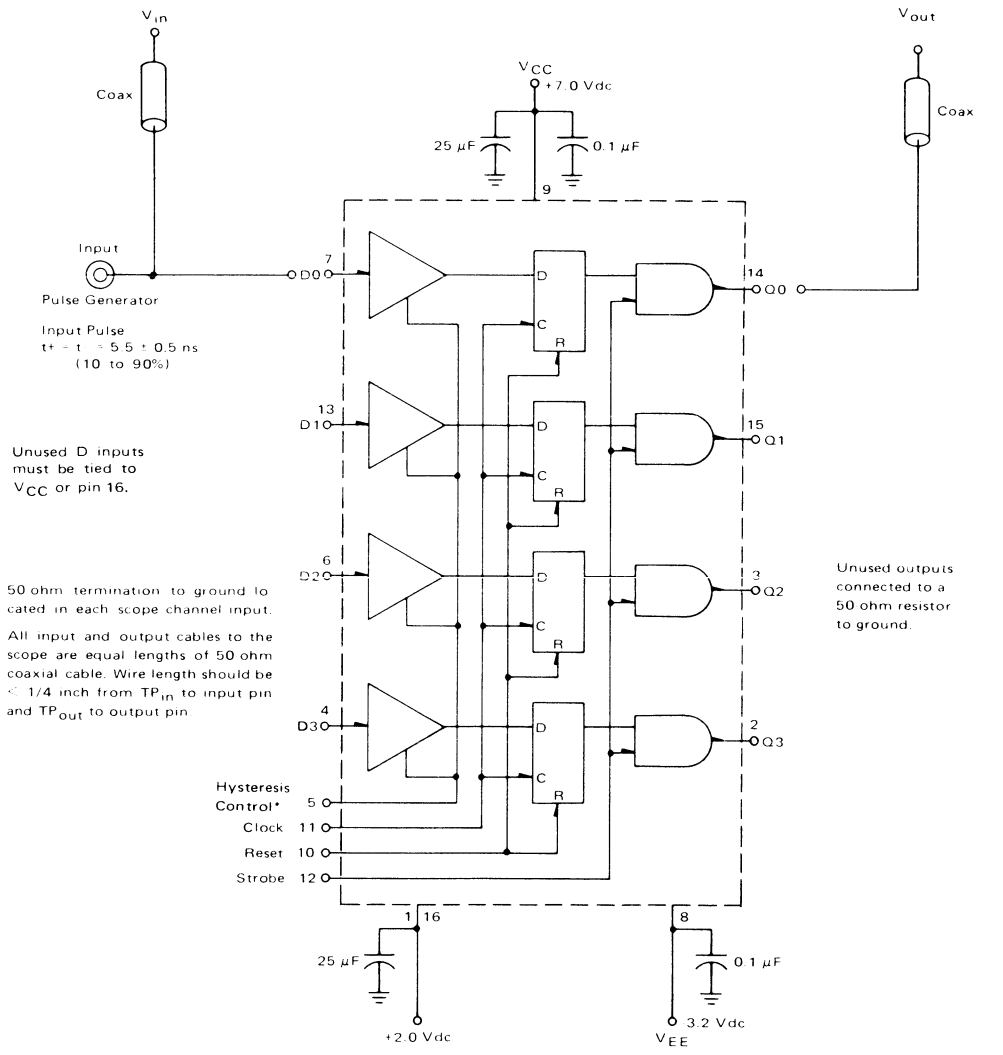
(1) When testing choose either MTTL or IBM Input Levels.

(2) $V_{IHA''}$, $V_{ILA''}$, $V_{IHA'''}$, and $V_{ILA'''}$, are logic "1" and logic "0" threshold voltages in the hysteresis mode as shown in diagram.

(3) Operation and limits shown also apply for V_{CC} = +6.0 V.



SWITCHING TIME TEST CIRCUIT



*Hysterisis Control tied to V_{EE} for fixed input reference, tied to pin 16 for input hysterisis mode.

Note: All power supply and logic levels are shown shifted 2 volts positive.

SWITCHING WAVEFORMS @ 25°C

FIGURE 1 – DATA to OUTPUT
(Clock and Reset are low, Strobe is high)

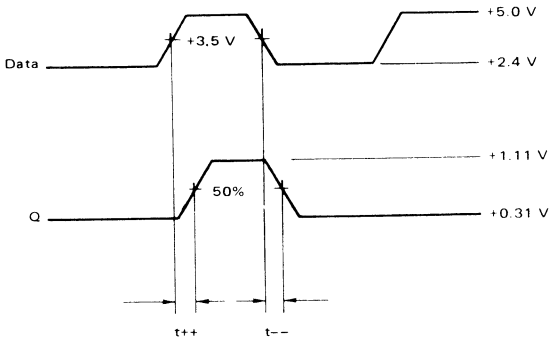


FIGURE 2 – STROBE to OUTPUT
(Data is high, Clock and Reset are low)

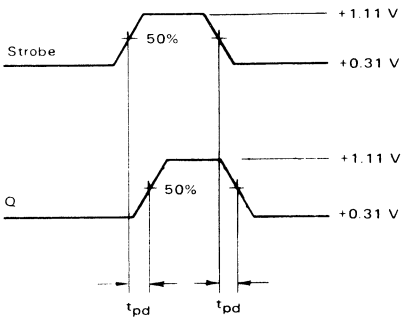


FIGURE 3 – RESET to OUTPUT
(Data and Strobe are high)

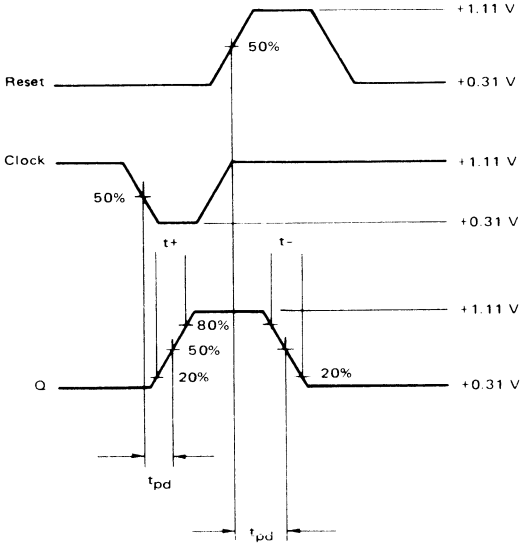


FIGURE 4 – CLOCK to OUTPUT
(Reset is low, Strobe is high)

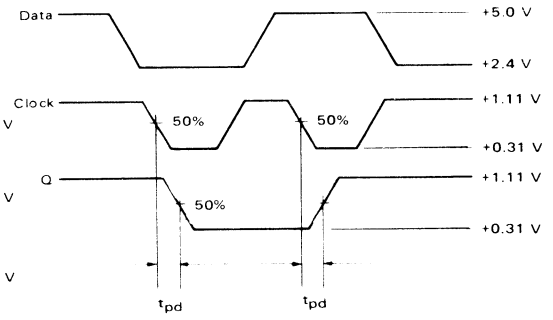
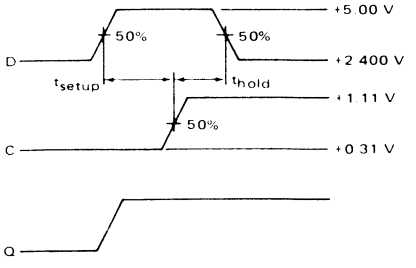


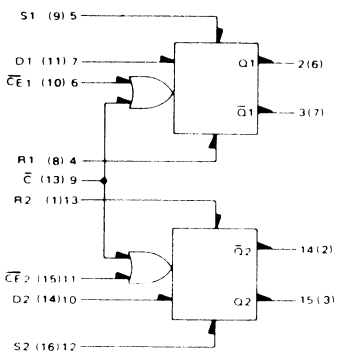
FIGURE 5 – $T_{SET\ UP}$ AND T_{HOLD} WAVEFORMS



Note: All power supply and logic levels are shown shifted 2 volts positive.

MC10130/MC10530

DUAL LATCH



TRUTH TABLE

D	$\bar{C}$	$\overline{CE}$	Q_{n+1}
L	L	L	L
H	L	L	H
Φ	L	H	Q_n
Φ	H	L	Q_n
Φ	H	H	Q_n

Φ = Don't Care

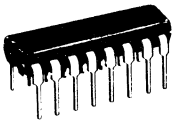
V_{CC} = Pin 1(5)
V_{CC2} = Pin 16(4)
V_{EE} = Pin 8(12)

The MC10130/MC10530 is a clocked dual D type latch. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock ($\bar{C}$).

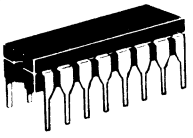
Any change at the D input will be reflected at the output while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

The set and reset inputs do not override the clock and D inputs. They are effective only when either $\bar{C}$ or $\overline{CE}$ or both are high.

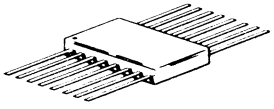
P_D = 155 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ
t_+, t_- = 2.7 ns typ (20%–80%)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10130 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10530 only

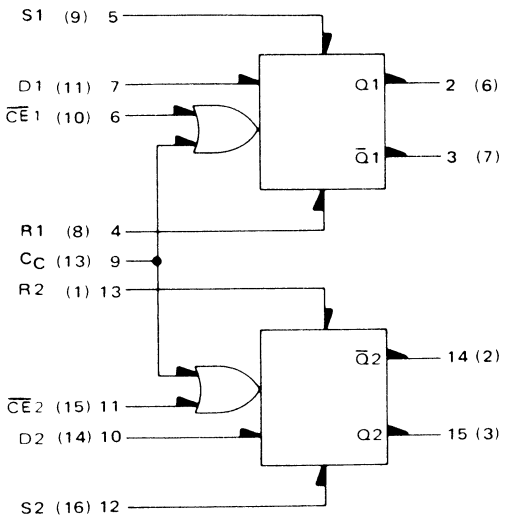
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	39	–	38	–	35	–	38	–	39	mAdc
Input Current	I_{inH}											μAdc
Pins 6,11		–	375	–	350	–	220	–	220	–	220	
Pin 9		–	450	–	425	–	265	–	265	–	265	
Pins 4,5,7,10,12,13		–	485	–	455	–	285	–	285	–	285	
Switching Times												ns
Propagation Delay	t_{pd}											
Data		1.0	3.9	1.0	3.6	1.0	3.5	1.0	3.8	1.0	4.1	
Set, Reset		1.0	3.9	1.0	3.6	1.0	3.5	1.0	3.9	1.0	4.1	
Clock		1.0	4.3	1.0	4.3	1.0	4.0	1.0	4.1	1.0	4.7	
Rise Time, Fall Time (20% to 80%)	t_+,t_-	1.0	3.9	1.0	3.6	1.1	3.5	1.1	3.8	1.0	4.1	ns
Setup Time	t_{set}	2.5	–	2.5	–	2.5	–	2.5	–	2.5	–	ns
Hold Time	t_{hold}	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	ns

−55°C and +125°C test values apply to MC105xx devices only.

MC10131/MC10531

DUAL TYPE D MASTER-SLAVE FLIP-FLOP



The MC10131/MC10531 is a dual master-slave type D flip-flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and $\overline{\text{Clock Enable}}$ ($\overline{CE}$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the $\overline{\text{Clock Enable}}$ inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

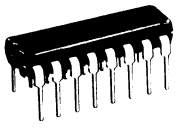
CLOCKED TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	L	L
H	H	H

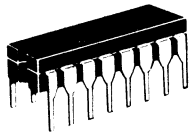
ϕ = Don't Care
$C = \bar{C}_E + C_C$
A clock H is a clock transition from a low to a high state.

P_D = 235 mW typ/pkg (No Load)
f_{Tog} = 160 MHz typ
t_{pd} = 3.0 ns typ
t_+, t_- = 2.5 ns typ (20% -80%)

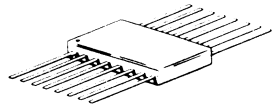
V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10131 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10531 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

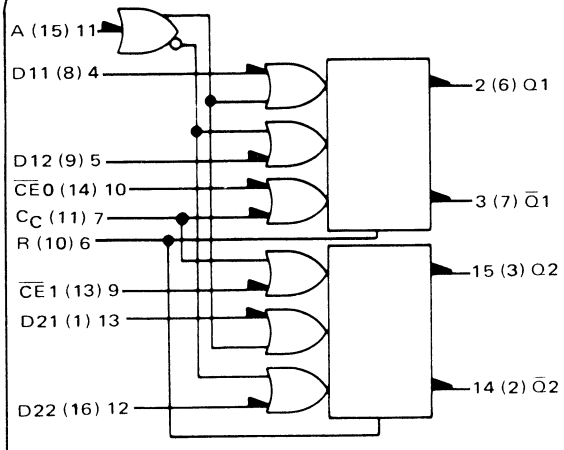
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	62	–	62	–	56	–	62	–	62	mAdc
Input Current	I_{inH}											μAdc
Pins 4, 5, 12, 13		–	565	–	525	–	330	–	330	–	330	
Pins 6, 11		–	375	–	350	–	220	–	220	–	220	
Pins 7, 10		–	415	–	390	–	245	–	245	–	245	
Pin 9		–	450	–	425	–	265	–	265	–	265	
Switching Times												ns
Propagation Delay	t_{pd}											
Clock		1.7	4.6	1.7	4.6	1.8	4.5	1.8	5.0	1.8	5.0	
Set, Reset		1.7	4.5	1.7	4.4	1.8	4.3	1.8	4.8	1.8	4.9	
Rise Time, Fall Time (20% to 80%)	t+, t–	1.0	4.6	1.0	4.6	1.1	4.5	1.1	4.9	1.1	4.9	
Setup Time	t_{set}	2.5	–	2.5	–	2.5	–	2.5	–	2.5	–	ns
Hold Time	t_{hold}	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	ns
Toggle Frequency	f_{Tog}	115	–	125	–	125	–	125	–	125	–	MHz

-55°C and +125°C test values apply to MC105xx devices only.

MC10132/MC10532

DUAL MULTIPLEXER WITH LATCH AND COMMON RESET



$D = (\overline{A} \bullet D11) + (A \bullet D12)$

TRUTH TABLE

R	D	C_C	$\overline{CE}$	Q_{n+1}
ϕ	L	L	L	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	H	Q_n
ϕ	H	L	L	H
L	H	L	H	Q_n
L	H	H	L	Q_n
L	H	H	H	Q_n
H	ϕ	ϕ	H	L

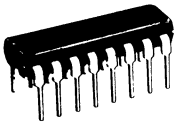
ϕ = Don't Care

The MC10132/MC10532 is a dual multiplexer with clocked D type latches. It incorporates common data select and reset inputs. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for a clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock (C_C).

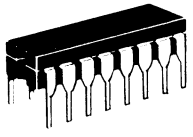
The data select (A) input determines which data input is enabled. A high (H) level enables data inputs D12 and D22 and a low (L) level enables data inputs D11 and D21. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled when the clock is in the high state, and disabled when the clock is low.

P_D = 225 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ

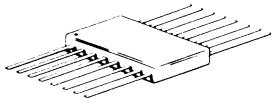
V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10132 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10532 only

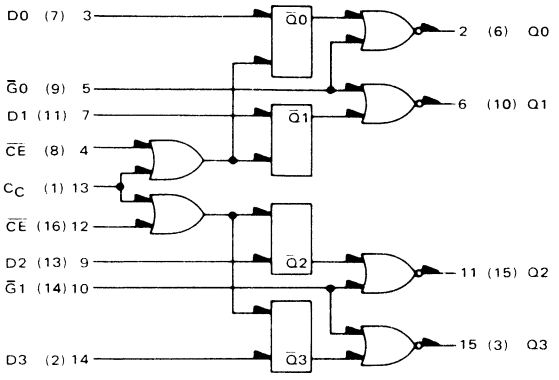
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	61	–	60	–	55	–	60	–	61	mAdc
Input Current	I_{inH}											μAdc
Pins 4, 5, 7, 12, 13		–	495	–	460	–	290	–	290	–	290	
Pin 6		–	660	–	620	–	390	–	390	–	390	
Pins 9, 10, 11		–	450	–	425	–	265	–	265	–	265	
Switching Times												ns
Propagation Delay	t_{pd}											
Data		1.0	3.7	1.0	3.6	1.0	3.3	1.0	3.7	1.0	3.9	
Reset		1.0	4.1	1.0	4.0	1.0	3.8	1.0	4.2	1.0	4.8	
Clock		1.0	6.2	1.0	6.0	1.0	5.7	1.0	6.3	1.0	6.7	
Select		1.0	5.0	1.0	4.8	1.0	4.6	1.0	5.0	1.0	5.8	
Rise Time, Fall Time (20% to 80%)	t+,t–	1.5	3.8	1.5	3.7	1.5	3.5	1.5	3.8	1.5	4.1	ns
Setup Time	t_{set}											ns
Data		2.5	–	2.5	–	2.5	–	2.5	–	2.5	–	
Select		3.5	–	3.5	–	3.5	–	3.5	–	3.5	–	
Hold Time	t_{hold}											ns
Data		1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	
Select		1.0	–	1.0	–	1.0	–	1.0	–	1.0	–	

-55°C and +125°C test values apply to MC105xx devices only.

MC10133/MC10533

QUAD LATCH



The MC10133/MC10533 is a high speed, low power, quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs, allowing direct wiring to a bus. When the clock is high, outputs will follow D inputs. Information is latched on the negative going transition of the clcok.

The outputs are gated when the output enable ($\overline{G}$) is low. All four latches may be clocked at one time with the common clock (C_C), or each half may be clocked separately with its clock enable ($\overline{CE}$).

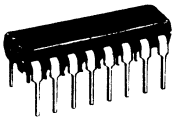
TRUTH TABLE

$\overline{G}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	L	ϕ	Q_n
L	H	L	L
L	H	H	H

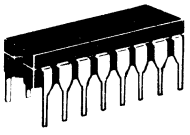
ϕ = Don't Care
C = $C_C + C_E$

V_{CC1} = Pin 1(5)
V_{CC2} = Pin 16(4)
V_{EE} = Pin 8(12)

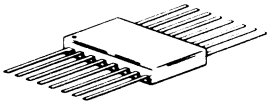
P_D = 310 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ
t_+, t_- = 2.0 ns typ (20% to 80%)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10133 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10533 only

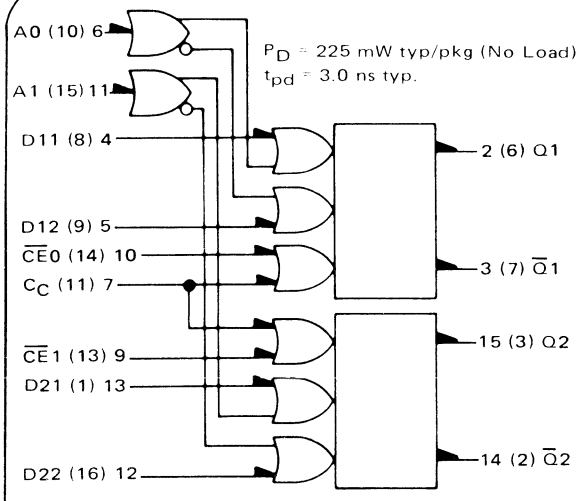
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	83	–	82	–	75	–	82	–	83	mAdc
Input Current	I_{inH}											μAdc
Pins 3,7,9,14		–	415	–	390	–	245	–	245	–	245	
Pins 4,12		–	450	–	425	–	265	–	265	–	265	
Pins 5,10,13		–	595	–	560	–	350	–	350	–	350	
Switching Times												ns
Propagation Delay Data	t_{pd}	1.0	5.8	1.0	5.6	1.0	5.4	1.1	5.9	1.0	6.3	
Clock		1.0	5.8	1.0	5.4	1.0	5.4	1.2	6.0	1.0	6.3	
$\overline{Gate}$		1.0	3.3	1.0	3.2	1.0	3.1	1.0	3.4	1.0	3.6	
Rise Time, Fall Time (20% to 80%)	t_+, t_-	1.0	3.9	1.0	3.6	1.1	3.5	1.1	3.8	1.0	4.1	ns
Setup Time	t_{set}	2.5	–	2.5	–	2.5	–	2.5	–	2.5	–	ns
Hold Time	t_{hold}	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	ns

−55°C and +125°C test values apply to MC105xx devices only.

MC10134/MC10534

DUAL MULTIPLEXER WITH LATCH



P_D = 225 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ.

The MC10134/MC10534 is a dual multiplexer with clocked D type latches. Each latch may be clocked separately by holding the common clock in the low state, and using the clock enable inputs for the clocking function. If the common clock is to be used to clock the latch, the clock enable ($\overline{CE}$) inputs must be in the low state. In this mode, the enable inputs perform the function of controlling the common clock (C_C).

The data select inputs determine which data input is enabled. A high (H) level on the A0 input enables data input D12 and a low (L) level on the A0 input enables data input D11. A high (H) level on the A1 input enables data input D22 and a low (L) level on the A1 input enables data input D21.

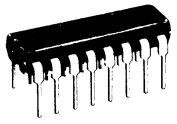
Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

TRUTH TABLE

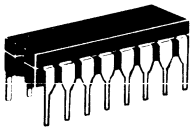
C	A0	D11	D12	Q_{n+1}
L	L	L	Φ	L
L	L	H	Φ	H
L	H	Φ	L	L
L	H	Φ	H	H
H	Φ	Φ	Φ	Q_n

Φ = Don't Care
$C = \overline{CE} + C_C$

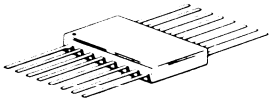
V_{CC1} = Pin 1(5)
V_{CC2} = Pin 16(4)
V_{EE} = Pin 8(12)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10134 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10534 only

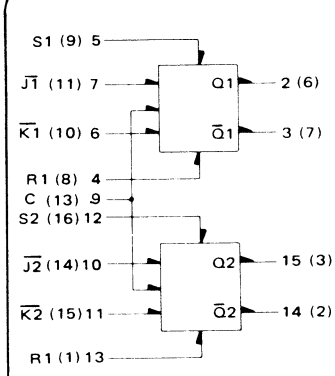
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	61	–	60	–	55	–	60	–	61	mAdc
Input Current	I_{inH}											μAdc
Pins 4,5,7,12,13		–	495	–	460	–	290	–	290	–	290	
Pins 6,9,10,11		–	450	–	425	–	265	–	265	–	265	
Switching Times												ns
Propagation Delay	t_{pd}											
Data		1.0	3.6	1.0	3.5	1.0	3.3	1.0	3.6	1.0	3.9	
Clock		1.0	6.2	1.0	6.0	1.0	5.7	1.0	6.3	1.0	6.7	
Select		1.0	5.0	1.0	4.8	1.0	4.6	1.0	5.0	1.0	5.6	
Rise Time, Fall Time (20% to 80%)	t+,t−	1.5	3.8	1.5	3.7	1.5	3.5	1.5	3.8	1.5	4.1	ns
Setup Time	t_{set}											ns
Data		2.5	–	2.5	–	2.5	–	2.5	–	2.5	–	
Select		3.5	–	3.5	–	3.5	–	3.5	–	3.5	–	
Hold Time	t_{hold}											ns
Data		1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	
Select		1.0	–	1.0	–	1.0	–	1.0	–	1.0	–	

−55°C and +125°C test values apply to MC105xx devices only.

MC10135/MC10535

DUAL J-K MASTER-SLAVE FLIP-FLOP



CLOCK J-K TRUTH TABLE*

J	K	Q_{n+1}
L	L	$\bar{Q}_n$
H	L	L
L	H	H
H	H	Q_n

*Output states change on positive transition of clock for J, K input condition present.

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

N.D. = Not Defined

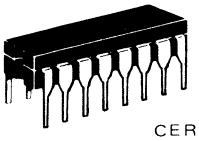
P_D = 280 mW typ/pkg (No Load)
f_{Tog} = 140 MHz typ
t_{pd} = 3.0 ns typ
t+, t− = 2.5 ns typ (20% to 80%)

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

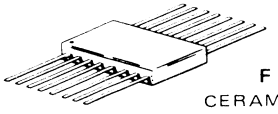
The MC10135/MC10535 is a dual master-slave dc coupled J-K flip-flop. Asynchronous set (S) and reset (R) are provided. The set and reset inputs override the clock.

A common clock is provided with separate $\bar{J}$-$\bar{K}$ inputs. When the clock is static, the $\bar{J}$-$\bar{K}$ inputs do not effect the output.

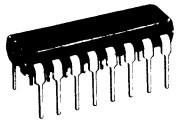
The output states of the flip-flop change on the positive transition of the clock.



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10535 only



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10135 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C Min	−55°C Max	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	I_E	–	75	–	75	–	68	–	75	–	75	mAdc
Input Current	I_{inH}											μAdc
Pins 6,7,9,10,11		–	450	–	425	–	265	–	265	–	265	
Pins 4,5,12,13		–	660	–	620	–	390	–	390	–	390	
Switching Times												ns
Propagation Delay	t_{pd}											
Clock		1.7	4.8	1.8	5.0	1.8	4.5	1.8	4.6	1.8	5.3	
Set, Reset		1.7	5.4	1.8	5.6	1.8	5.0	1.8	5.2	1.8	5.9	
Rise Time, Fall Time (20% to 80%)	t+,t−	1.0	4.8	1.1	4.8	1.1	4.5	1.1	4.7	1.0	5.3	ns
Setup Time	t_{set}	2.5	–	2.5	–	2.5	–	2.5	–	2.5	–	ns
Hold Time	t_{hold}	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	ns
Toggle Frequency	f_{Tog}	125	–	125	–	125	–	125	–	115	–	MHz

−55°C and +125°C test values apply to MC105xx devices only.

MC10136/MC10536

UNIVERSAL HEXADECIMAL COUNTER

SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	L	L	H	H	ϕ	H	L	L	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	L	H	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	H	H	H	L
L	H	ϕ	ϕ	ϕ	ϕ	H	L	H	H	H	H	H
L	H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H
H	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H
L	L	ϕ	ϕ	ϕ	ϕ	ϕ	H	H	H	L	L	L
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	H	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H

ϕ = Don't care.

* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

** A clock H is defined as a clock input transition from a low to a high logic level.

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

P_D = 625 mW typ/pkg (No Load)
f_{count} = 150 MHz typ
t_{pd} = 3.3 ns typ (C - Q)
= 7.0 ns typ (C - $\overline{C}_{out}$)
= 5.0 ns typ ($\overline{C}_{in}$ - $\overline{C}_{out}$)

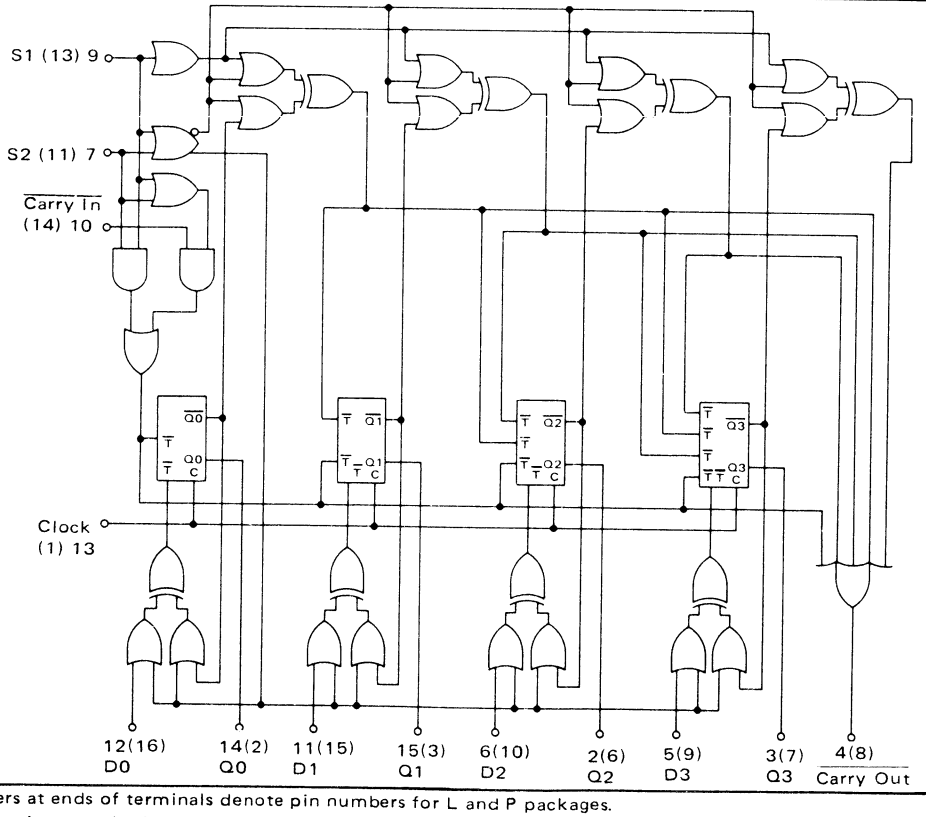
The MC10136/MC10536 is a high speed synchronous counter that can count up, count down, preset, or stop count at frequencies exceeding 100 MHz. The flexibility of this device allows the designer to use one basic counter for most applications, and the synchronous count feature makes the MC10136/MC10536 suitable for either computers or instrumentation.

Three control lines (S1, S2, and $\overline{\text{Carry In}}$) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. $\overline{\text{Carry Out}}$ goes low on the terminal count, or when the counter is being preset.

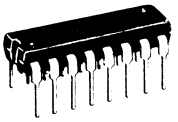
This device is not designed for use with gated clocks. Control is via S1 and S2.

FUNCTION SELECT TABLE

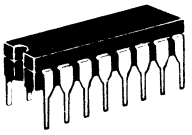
S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)



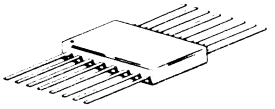
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10136 Only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10536 Only

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	165	–	165	–	150	–	165	–	165	mAdc
Input Current	I_{inH}											μAdc
Pins 5, 6, 11, 12		–	375	–	350	–	220	–	220	–	220	
Pins 9, 10		–	415	–	390	–	245	–	245	–	245	
Pin 7		–	450	–	425	–	265	–	265	–	265	
Pin 13		–	495	–	460	–	290	–	290	–	290	
Switching Times												ns
Propagation Delay	t_{pd}											
Clock to Q		0.8	4.6	0.8	4.8	1.0	4.5	1.4	5.0	1.4	5.2	
Clock to $\overline{\text{Carry Out}}$		2.0	11.0	2.0	10.9	2.5	10.5	2.4	11.5	2.4	12.6	
$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$		1.6	7.1	1.6	7.4	1.6	6.9	1.9	7.5	1.9	7.6	
Rise Time, Fall Time (20% to 80%)	t+, t-	0.9	3.3	0.9	3.3	1.1	3.3	1.1	3.5	1.2	3.7	ns
Setup Time	t_{set}											ns
Data (D0 to C)		3.5	–	3.5	–	3.5	–	3.5	–	3.5	–	
Select (S to C)		7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	
$\overline{\text{Carry In}}$ ($\overline{C_{in}}$ to C)		4.5	–	4.5	–	3.7	–	4.5	–	4.5	–	
(C to $\overline{C_{in}}$)		-1.0	–	-1.0	–	-1.0	–	-1.0	–	-1.0	–	
Hold Time	t_{hold}											ns
Data (C to D0)		0	–	0	–	0	–	0	–	0	–	
Select (C to S)		-2.5	–	-2.5	–	-2.5	–	-2.5	–	-2.5	–	
$\overline{\text{Carry In}}$ (C to $\overline{C_{in}}$)		-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	
($\overline{C_{in}}$ to C)		4.0	–	4.0	–	3.1	–	4.0	–	4.0	–	
Counting Frequency	$f_{countup}$	115	–	125	–	125	–	125	–	115	–	MHz
	$f_{countdown}$	115	–	125	–	125	–	125	–	115	–	

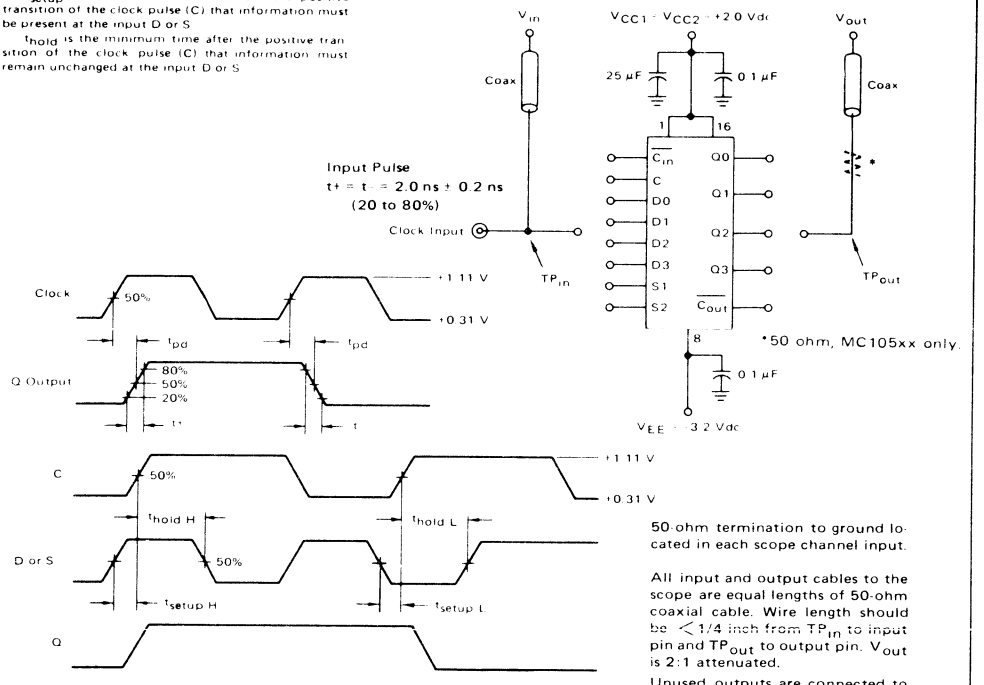
-55°C and +125°C test values apply to MC105xx devices only.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input D or S.

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the input D or S.



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. V_{out} is 2:1 attenuated.

Unused outputs are connected to a 50 ohm resistor to ground (100 ohm for MC105xx).

NOTE: All power supply and logic levels are shown shifted 2 volts positive.

SET UP AND HOLD TIMES

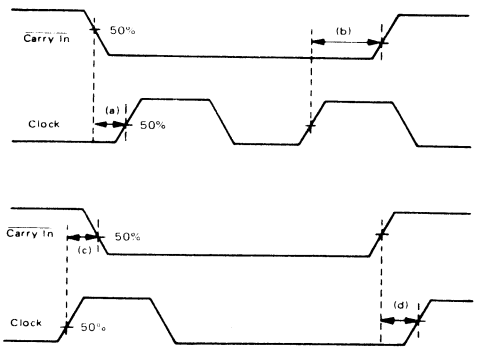
(a) is the minimum time to wait after the counter has been enabled to clock it.

(b) is the minimum time before the counter has been disabled that it may be clocked.

(c) is the minimum time before the counter is enabled that a clock pulse may be applied with no effect on the state of the counter.

(d) is the minimum time to wait after the counter is disabled that a clock pulse may be applied with no effect in the state of the counter.

(b) and (c) may be negative numbers.



APPLICATIONS INFORMATION

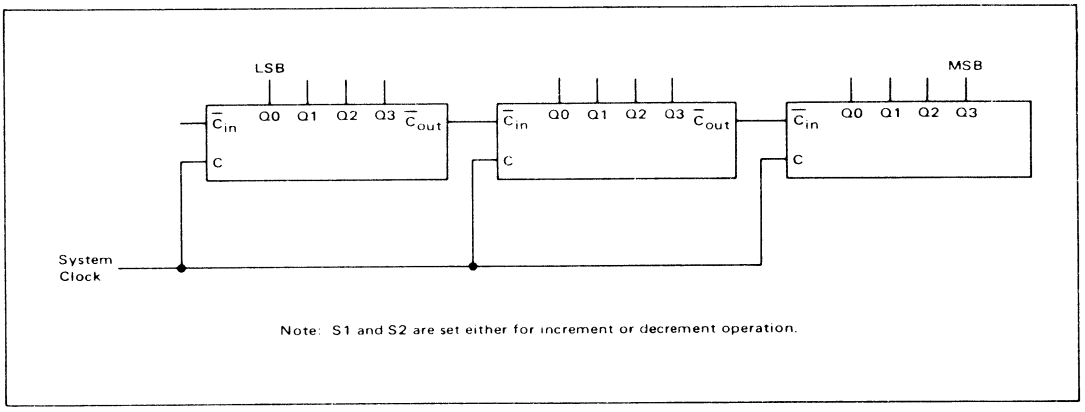
To provide more than four bits of counting capability several MC10136/MC10536 counters may be cascaded. The Carry In input overrides the clock when the counter is either in the increment mode or the decrement mode of operation. This input allows several devices to be cascaded in a fully synchronous multistage counter as illustrated in Figure 1. The carry is advanced between stages as shown with no external gating. The Carry In of the first device may be left open. The system clock is common to all devices.

The various operational modes of the counter make it useful for a wide variety of applications. If used with MECL III devices, prescalers with input toggle frequencies in excess of 300 MHz are possible. Figure 2 shows such a prescaler using the MC10136 and MC1670. Use of the MC10231 in place of the MC1670 permits 200 MHz operation.

The MC10136 may also be used as a programmable counter. The configuration of Figure 3 requires no additional gates, although maximum frequency is limited to about 50 MHz. The divider modulus is equal to the program input plus one (M = N + 1), therefore, the counter will divide by a modulus varying from 1 to 16.

A second programmable configuration is also illustrated in Figure 4. A pulse swallowing technique is used to speed the counter operation up to 110 MHz typically. The divider modulus for this figure is equal to the program input (M = N). The minimum modulus is 2 because of the pulse swallowing technique, and the modulus may vary from 2 to 15. This programmable configuration requires an additional gate, such as ½MC10109 and a flip flop such as ½MC10131.

FIGURE 1 – 12 BIT SYNCHRONOUS COUNTER



Note: S1 and S2 are set either for increment or decrement operation.

FIGURE 2 – 300 MHz PRESCALER

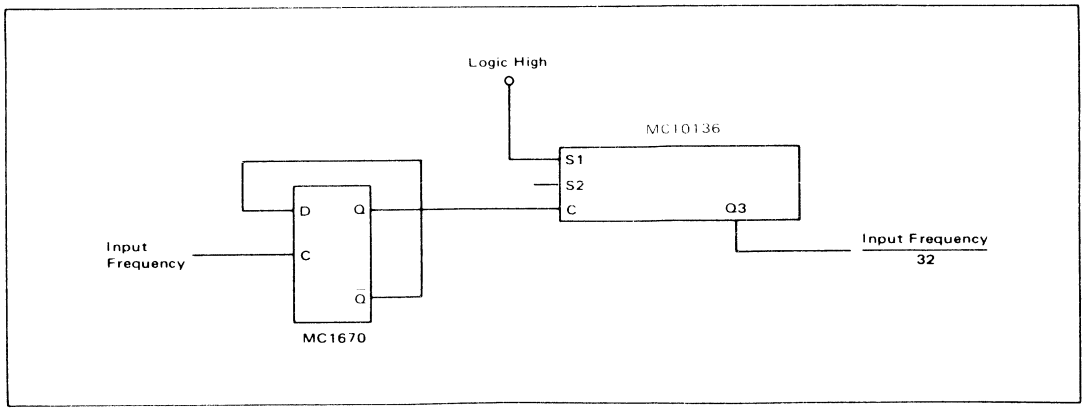
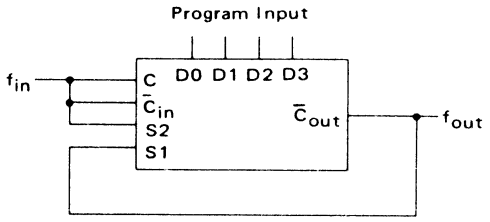


FIGURE 3 – 50 MHz PROGRAMMABLE COUNTER

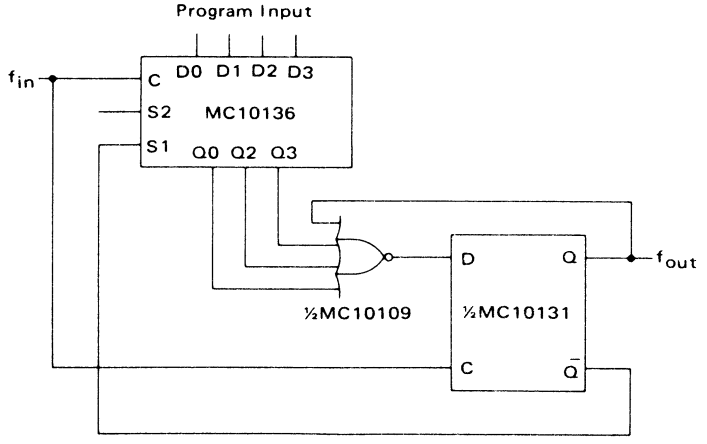


1 $f_{out} = \dfrac{f_{in}}{\text{Program Input} + 1}$

2 $f_{max} \cong 50$ MHz Typ.

3 Divide Ratio is from 1 to 16.

FIGURE 4 – 100 MHz PROGRAMMABLE COUNTER



1 $f_{out} = \dfrac{f_{in}}{\text{Program Input}}$

2 $f_{max} \cong 110$ MHz Typ.

3 Divide Ratio is from 2 to 15.

MC10137/MC10537

UNIVERSAL DECADE COUNTER

SEQUENTIAL TRUTH TABLE*

INPUTS								OUTPUTS				
S1	S2	D0	D1	D2	D3	$\overline{\text{Carry In}}$	Clock **	Q0	Q1	Q2	Q3	$\overline{\text{Carry Out}}$
L	L	H	H	H	L	ϕ	H	H	H	H	L	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	H	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	H	L
L	H	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	L	H
L	H	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
L	H	ϕ	ϕ	ϕ	ϕ	H	H	H	L	L	L	H
L	H	ϕ	ϕ	ϕ	ϕ	H	H	H	L	L	L	H
H	H	ϕ	ϕ	ϕ	ϕ	ϕ	H	H	L	L	L	H
L	L	H	H	L	L	ϕ	H	H	H	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	H	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	H	L	L	L	H
H	L	ϕ	ϕ	ϕ	ϕ	L	H	L	L	L	L	L

ϕ = Don't care.

* Truth table shows logic states assuming inputs vary in sequence shown from top to bottom.

** A clock H is defined as a clock input transition from a low to a high logic level.

FUNCTION SELECT TABLE

S1	S2	Operating Mode
L	L	Preset (Program)
L	H	Increment (Count Up)
H	L	Decrement (Count Down)
H	H	Hold (Stop Count)

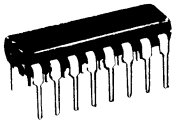
P_D = 625 mW typ/pkg (No Load)

f_{count} = 150 MHz typ

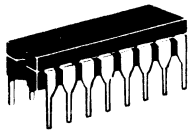
t_{pd} = 3.3 ns typ (C – Q)
= 7.0 ns typ (C – $\overline{C}_{out}$)
= 5.0 ns typ ($\overline{C}_{in}$ – $\overline{C}_{out}$)

The MC10137/MC10537 is a high speed synchronous counter that can count up, down, preset, or stop count at frequencies exceeding 100 MHz. The flexibility of this device allows the designer to use one basic counter for most applications. The snychronous count feature makes the MC10137 suitable for either computers or instrumentation.

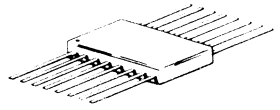
Three control lines (S1, S2, and $\overline{\text{Carry In}}$) determine the operation mode of the counter. Lines S1 and S2 determine one of four operations; preset (program), increment (count up), decrement (count down), or hold (stop count). Note that in the preset mode a clock pulse is necessary to load the counter, and the information present on the data inputs (D0, D1, D2, and D3) will be entered into the counter. $\overline{\text{Carry Out}}$ goes low on the terminal count. The $\overline{\text{Carry Out}}$ on the MC10137 is partially decoded from Q1 and Q2 directly, so in the preset mode the condition of the $\overline{\text{Carry Out}}$ after the Clock's positive excursion will depend on the condition of Q1 and/or Q2. The counter changes state only on the positive going edge of the clock. Any other input may change at any time except during the positive transition of the clock. The sequence for counting out of improper states is as shown in the State Diagrams.



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10137 only



L SUFFIX
CERAMIC PACKAGE
CASE 620

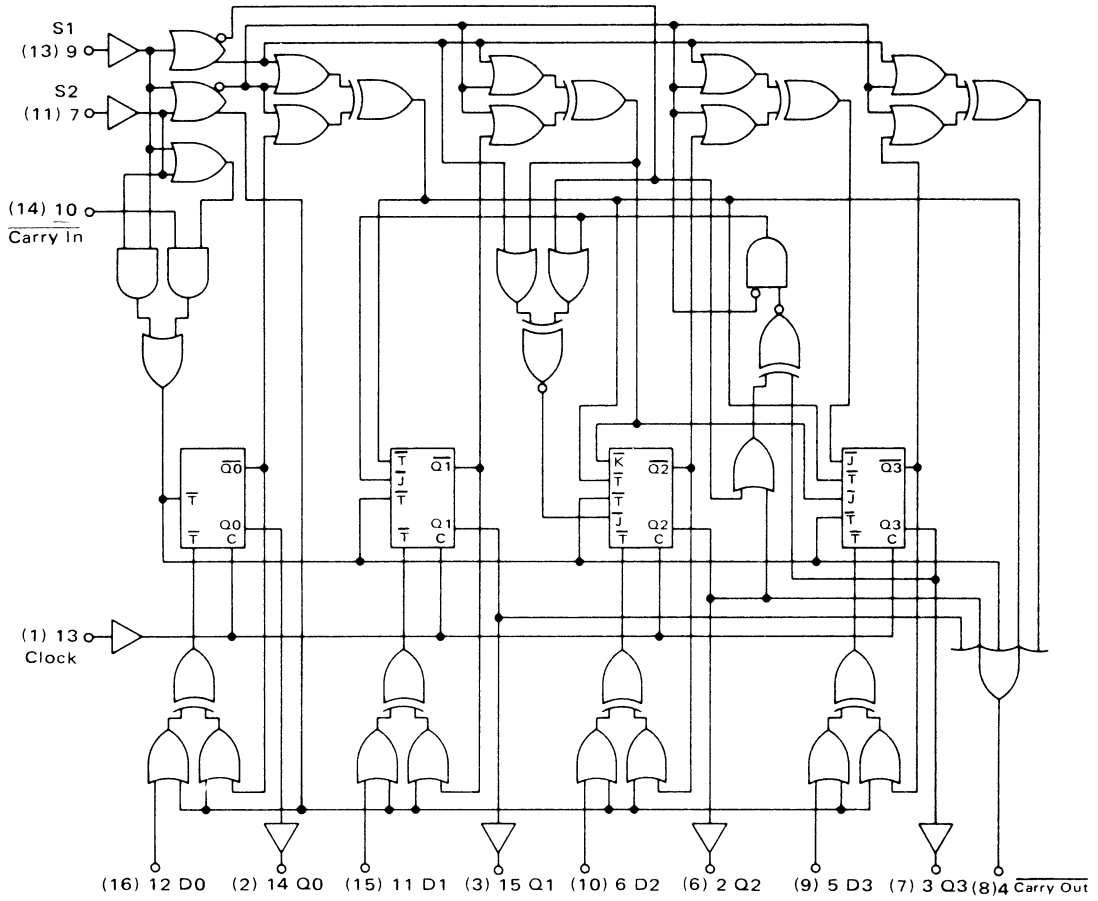


F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10537 only

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	165	–	165	–	150	–	165	–	165	mAdc
Input Current	I_{inH}											μAdc
Pins 5, 6, 11, 12		–	375	–	350	–	220	–	220	–	220	
Pins 9, 10		–	415	–	390	–	245	–	245	–	245	
Pin 7		–	450	–	425	–	265	–	265	–	265	
Pin 13		–	495	–	460	–	290	–	290	–	290	
Switching Times												ns
Propagation Delay	t_{pd}											
Clock to Q		0.8	4.6	0.8	4.8	1.0	4.5	1.4	5.0	1.4	5.2	
Clock to $\overline{\text{Carry Out}}$		2.0	11	2.0	10.9	2.5	10.5	2.4	11.5	2.4	12.6	
$\overline{\text{Carry In}}$ to $\overline{\text{Carry Out}}$		1.6	7.1	1.6	7.4	1.6	6.9	1.9	7.5	1.9	7.6	
Rise Time, Fall Time (20% to 80%)	t^+, t^-	0.9	3.3	0.9	3.3	1.1	3.3	1.1	3.5	1.2	3.7	ns
Setup Time	t_{set}											ns
Data (D0 to C)		3.5	–	3.5	–	3.5	–	3.5	–	3.5	–	
Select (S to C)		7.5	–	7.5	–	7.5	–	7.5	–	7.5	–	
$\overline{\text{Carry In}}$ ($\overline{C_{in}}$ to C)		4.5	–	4.5	–	3.7	–	4.5	–	4.5	–	
(C to $\overline{C_{in}}$)		-1.0	–	-1.0	–	-1.0	–	-1.0	–	-1.0	–	
Hold Time	t_{hold}											ns
Data (C to D0)		0	–	0	–	0	–	0	–	0	–	
Select (C to S)		-2.5	–	-2.5	–	-2.5	–	-2.5	–	-2.5	–	
$\overline{\text{Carry In}}$ (C to $\overline{C_{in}}$)		-1.6	–	-1.6	–	-1.6	–	-1.6	–	-1.6	–	
($\overline{C_{in}}$ to C)		4.0	–	4.0	–	3.1	–	4.0	–	4.0	–	
Counting Frequency	$f_{countup}$	115	–	125	–	125	–	125	–	115	–	MHz
	$f_{countdn}$	115	–	125	–	125	–	125	–	115	–	

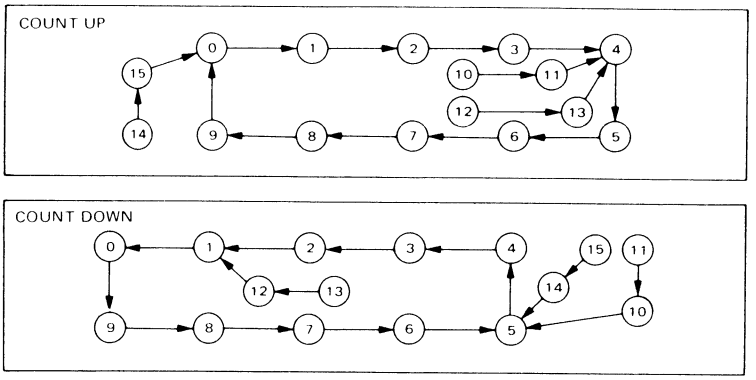
-55°C and +125°C test values apply to MC105xx devices only.



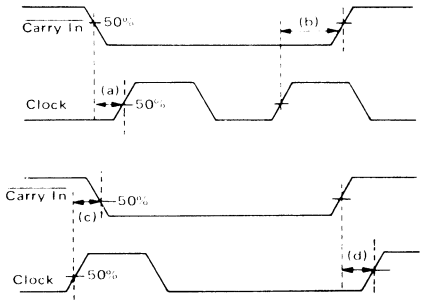
V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

STATE DIAGRAMS



SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



(a) is the minimum time to wait after the counter has been enabled to clock it.

(b) is the minimum time before the counter has been disabled that it may be clocked.

(c) is the minimum time before the counter is enabled that a clock pulse may be applied with no effect on the state of the counter.

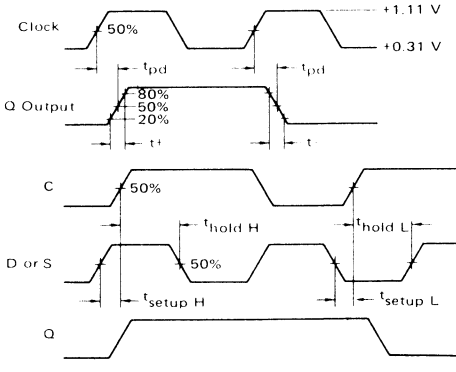
(d) is the minimum time to wait after the counter is disabled that a clock pulse may be applied with no effect in the state of the counter.

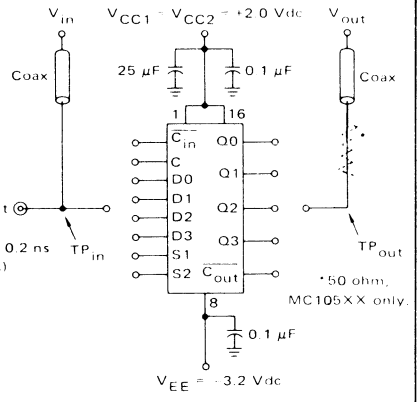
(b) and (c) may be negative numbers.

NOTE:

t_{setup} is the minimum time before the positive transition of the clock pulse (C) that information must be present at the input D or S.

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the input D or S.





50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin. V_{out} is 2:1 attenuated.

Unused outputs are connected to a 50 ohm resistor to ground (100 ohm for MC105XX).

NOTE: All power supply and logic levels are shown shifted 2 volts positive.

COUNTER TRUTH TABLES

BI-QUINARY

(Clock connected to C2 and Q3 connected to C1)

COUNT	Q1	Q2	Q3	Q0
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	L	L	L	H
6	H	L	L	H
7	L	H	L	H
8	H	H	H	H
9	L	L	H	H

BCD

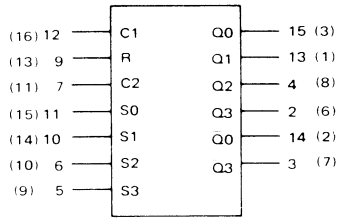
(Clock connected to C1 and Q0 connected to C2)

COUNT	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

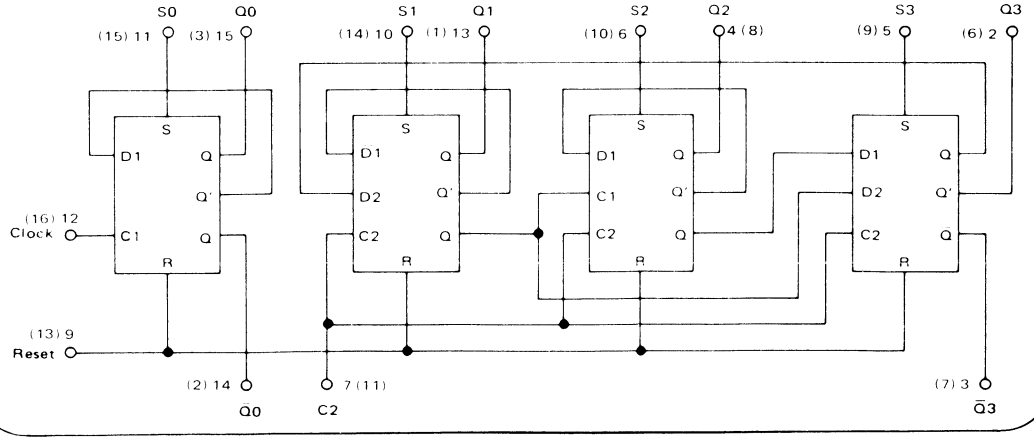
The MC10138/MC10538 is a four bit counter capable of divide by two, five, or ten functions. It is composed of four set-reset master-slave flip-flops. Clock inputs trigger on the positive going edge of the clock pulse.

Set or reset inputs override the clock, allowing asynchronous "set" or "clear". Individual set and common reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

P_D = 370 mW typ/pkg (No Load)
f_{Tog} = 150 MHz typ
t_{pd} = 3.5 ns typ
t_+, t_- = 2.5 ns typ (20% to 80%)



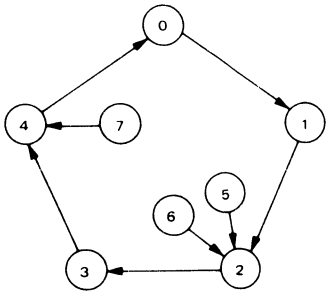
V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)



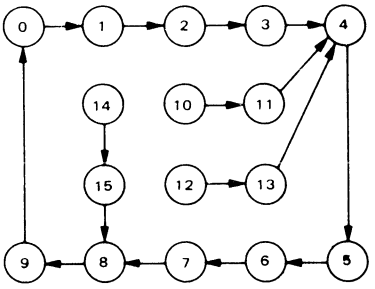
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

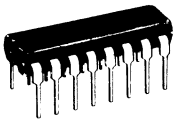
COUNTER STATE DIAGRAM – POSITIVE LOGIC

Clock connected to C2

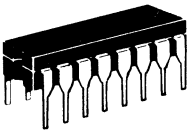


$\overline{Q0}$ connected to C2

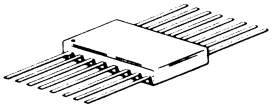




P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10138 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



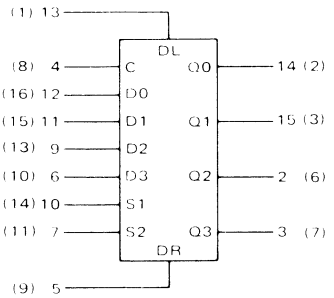
F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10538 only

Characteristic	Symbol	−55°C Min	−55°C Max	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	I_E	–	97	–	97	–	88	–	97	–	97	mAdc
Input Current	I_{inH}											μAdc
Pin 12		–	375	–	350	–	220	–	220	–	220	
Pins 5,6,10,11		–	415	–	390	–	245	–	245	–	245	
Pin 7		–	495	–	460	–	290	–	290	–	290	
Pin 9		–	700	–	650	–	410	–	410	–	410	
Switching Times												ns
Propagation Delay	t_{pd}											
Clock to Q0, $\overline{Q0}$		1.4	5.5	1.4	5.0	1.5	4.8	1.5	5.3	1.5	5.5	
Clock to Q1, Q2, Q3, $\overline{Q3}$		1.4	6.2	1.4	5.2	1.5	5.0	1.5	5.5	1.5	6.2	
Set		1.4	5.2	1.4	5.2	1.5	5.0	1.5	5.5	1.5	6.2	
Reset		1.4	5.5	1.4	5.2	1.5	5.0	1.5	5.5	1.5	6.2	
Rise Time, Fall Time (20% to 80%)	t^+, t^-	1.1	4.7	1.1	4.7	1.1	4.5	1.1	5.0	1.1	5.0	ns
Counting Frequency	f_{count}	125	–	125	–	125	–	125	–	125	–	MHz

−55°C and +125°C test values apply to MC105xx devices only.

MC10141/MC10541

FOUR-BIT UNIVERSAL SHIFT REGISTER



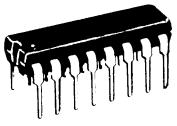
TRUTH TABLE

SELECT			OUTPUTS			
S1	S2	OPERATING MODE	$Q0_{n+1}$	$Q1_{n+1}$	$Q2_{n+1}$	$Q3_{n+1}$
L	L	Parallel Entry	D0	D1	D2	D3
L	H	Shift Right*	$Q1_n$	$Q2_n$	$Q3_n$	DR
H	L	Shift Left*	DL	$Q0_n$	$Q1_n$	$Q2_n$
H	H	Stop Shift	$Q0_n$	$Q1_n$	$Q2_n$	$Q3_n$

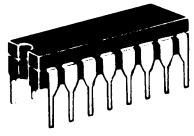
*Outputs as exist after pulse appears at C input with input conditions as shown. †Pulse = Positive transition of clock input.

The MC10141/MC10541 is a four-bit universal shift register which performs shift left, or shift right, serial/parallel in, and serial/parallel out operations with no external gating. Inputs S1 and S2 control the four possible operations of the register without external gating of the clock. The flip-flops shift information on the positive edge of the clock. The four operations are stop shift, shift left, shift right, and parallel entry of data. The other six inputs are all data type inputs, four for parallel entry data, and one for shifting in from the left (DL) and one for shifting in from the right (DR).

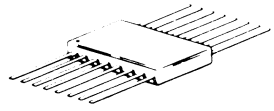
P_D = 425 mW typ/pkg (No Load)
f_{Shift} = 200 MHz typ
V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10141 only

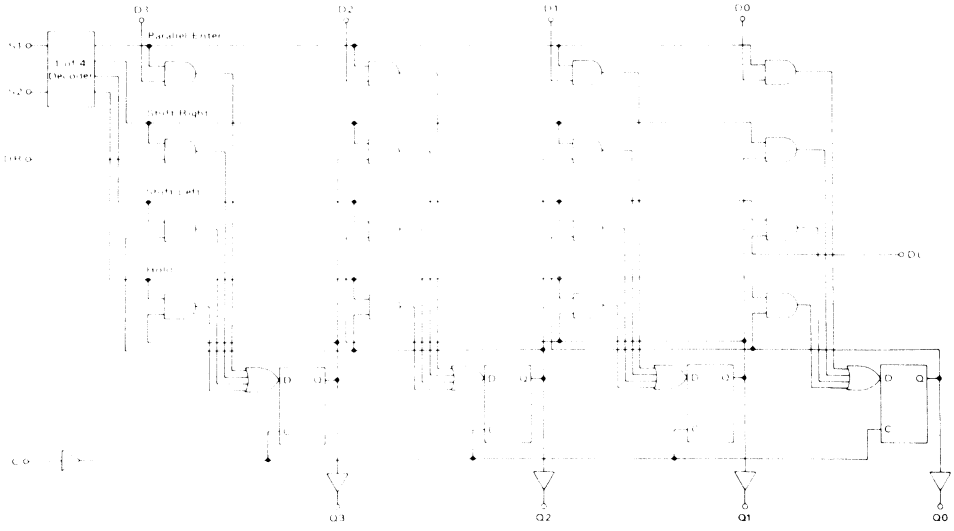


L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10541 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

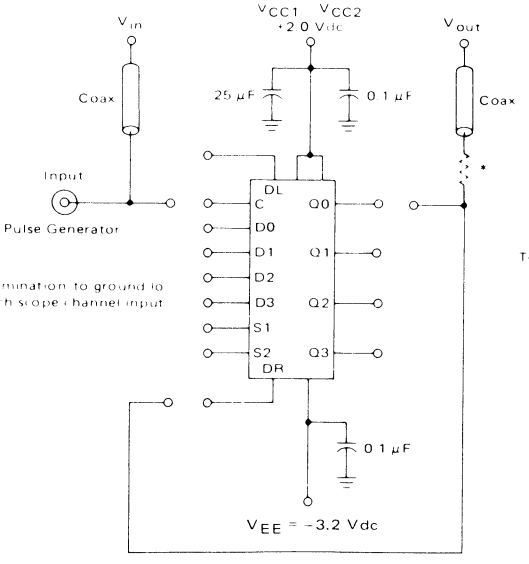


ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	112	–	112	–	102	–	112	–	112	mAdc
Input Current	I_{inH}											μAdc
Pins 5, 6, 9, 11, 12, 13		–	375	–	350	–	220	–	220	–	220	
Pins 7,10		–	415	–	390	–	245	–	245	–	245	
Pin 4		–	450	–	425	–	265	–	265	–	265	
Switching Times												ns
Propagation Delay	t_{pd}	1.7	4.1	1.7	3.9	1.8	3.8	2.0	4.2	2.0	4.5	
Rise Time, Fall Time (20% to 80%)	t+,t−	1.0	3.6	1.0	3.4	1.1	3.3	1.1	3.6	1.0	3.9	ns
Setup Time	t_{set}											ns
Data		3.0	–	2.5	–	2.5	–	2.5	–	3.0	–	
Select		7.0	–	5.5	–	5.0	–	5.5	–	7.0	–	
Hold Time	t_{hold}											ns
Data, Select		1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	
Shift Frequency	f_{Shift}	150	–	150	–	150	–	150	–	150	–	MHz

−55°C and +125°C test values apply to MC105xx devices only.

SHIFT FREQUENCY TEST CIRCUIT



50 ohm termination to ground located in each scope channel input

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Test Procedures

1. Set D1, D2, D3 +0.31 Vdc (Logic L)
   D0 +1.11 Vdc (Logic H)
2. Apply Clock pulse V_{IH} / V_{IL} to set Q0 high
3. Maintain Clock Low
   Set S1 +0.31 Vdc (Logic L)
   S2 +1.11 Vdc (Logic H)
4. Test Shift Frequency

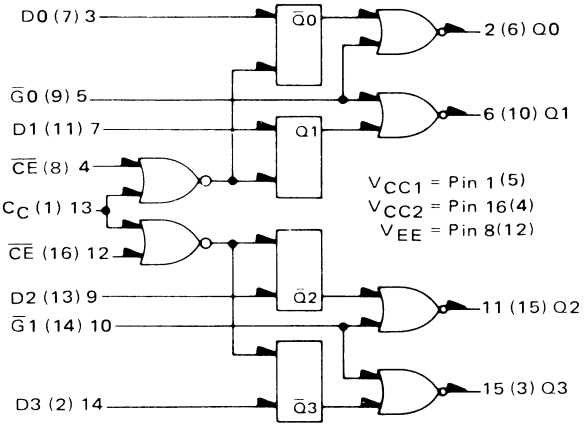
Unused outputs are connected to a 50 ohm resistor to ground (100 ohm for MC105xx).

*50 ohm, MC105xx only

NOTE: All power supply and logic levels are shown shifted 2 volts positive.

MC10153/MC10553

QUAD LATCH



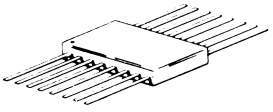
The MC10153/MC10553 is a high speed, low power, quad latch consisting of four bistable latch circuits with D type inputs and gated Q outputs, allowing direct wiring to a bus. When the clock is low, outputs will follow D inputs. Information is latched on the positive going transition of the clock. The MC10153/MC10553 provides the same logic function as the MC10133/MC10533 except for inversion of the clock.

TRUTH TABLE

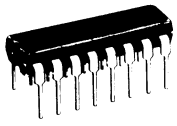
$\overline{G}$	C	D	Q_{n+1}
H	ϕ	ϕ	L
L	H	ϕ	Q_n
L	L	L	L
L	L	H	H

ϕ = Don't Care
$C = C_C + \overline{CE}$

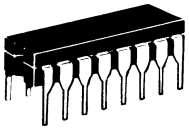
P_D = 310 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ
$t+, t-$ = 2.0 ns typ (20% to 80%)



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10553 only



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10153 only



L SUFFIX
CERAMIC PACKAGE
CASE 620

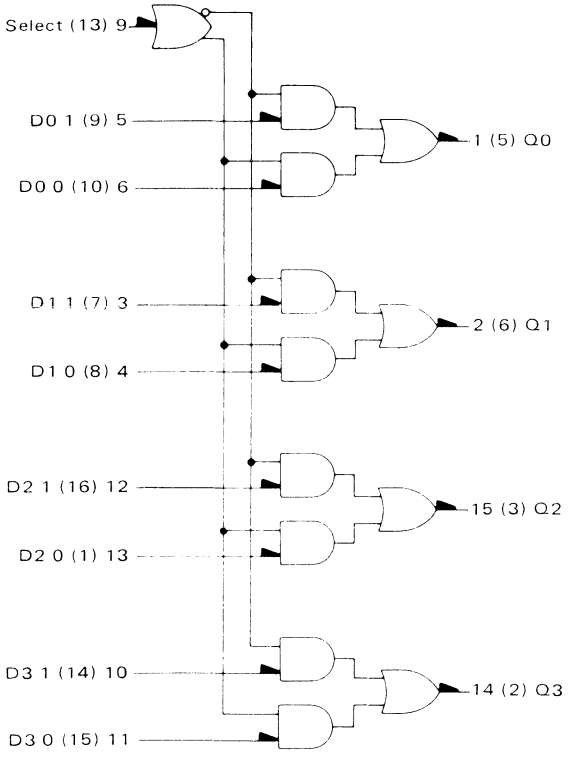
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	83	–	83	–	75	–	83	–	83	mAdc
Input Current	I_{inH}											μAdc
Pins 3,4,7,9,12,14		–	415	–	390	–	245	–	245	–	245	
Pin 13		–	495	–	460	–	290	–	290	–	290	
Pins 5,10		–	595	–	560	–	350	–	350	–	350	
Switching Times												ns
Propagation Delay	t_{pd}											
Data		1.0	5.8	1.0	5.6	1.0	5.4	1.1	5.9	1.0	6.3	
Clock		1.0	6.1	1.0	5.6	1.0	5.6	1.2	6.2	1.0	6.6	
$\overline{Gate}$		1.0	3.4	1.0	3.2	1.0	3.1	1.0	3.4	1.0	3.6	
Rise Time, Fall Time (20% to 80%)	$t+,t-$	1.0	3.9	1.0	3.6	1.1	3.5	1.1	3.8	1.0	4.1	ns
Setup Time	t_{set}	2.5	–	2.5	–	2.5	–	2.5	–	2.5	–	ns
Hold Time	t_{hold}	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	ns

−55°C and +125°C test values apply to MC105xx devices only.

MC10158/MC10558

QUAD 2-INPUT MULTIPLEXER (Non-Inverting)



The MC10158/MC10558 is a quad two channel multiplexer. A common select input determines which data inputs are enabled. A high (H) level enables data inputs D0 0, D1 0, D2 0, and D3 0 and a low (L) level enables data inputs D0 1, D1 1, D2 1, and D3 1.

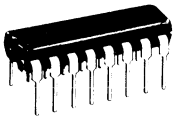
TRUTH TABLE

Select	D0	D1	Q
L	Φ	L	L
L	Φ	H	H
H	L	Φ	L
H	H	Φ	H

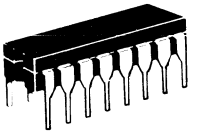
Φ : Don't care

V_{CC} = Pin 16 (4)
V_{EE} = Pin 8 (12)

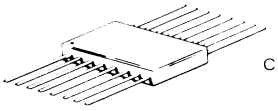
P_D = 197 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ (Data to Q)
3.2 ns typ (Select to Q)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10158 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10558 only

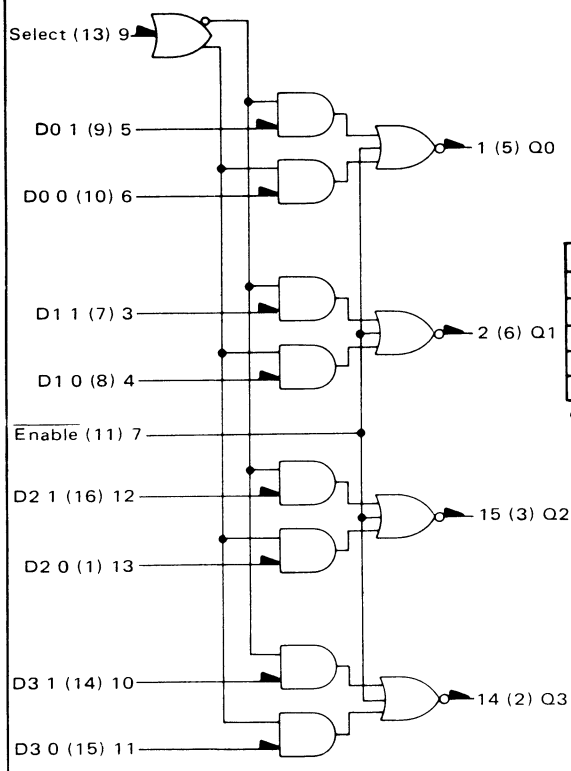
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	53	–	53	–	48	–	53	–	53	mAdc
Input Current	I_{inH}											μAdc
Pin 9		–	380	–	360	–	225	–	225	–	225	
Pins 3,4,5,6,10,11,12,13		–	425	–	400	–	250	–	250	–	250	
Switching Times												ns
Propagation Delay	t_{pd}											
Data		1.5	3.5	1.3	3.1	1.2	3.0	1.3	3.2	1.5	3.5	
Select		2.5	5.0	2.5	4.8	2.4	4.5	2.5	4.8	2.5	5.0	
Rise Time, Fall Time (20% to 80%)	t+, t−	1.6	3.5	1.6	3.4	1.5	3.3	1.6	3.4	1.6	3.5	ns

−55°C and +125°C test values apply to MC105xx devices only.

MC10159/MC10559

QUAD 2-INPUT MULTIPLEXER (Inverting)



The MC10159/MC10559 is a quad two channel multiplexer with enable. It incorporates common enable and common data select inputs. The select input determines which data inputs are enabled. A high (H) level enables data inputs D0 0, D1 0, D2 0, and D3 0. A low (L) level enables data inputs D0 1, D1 1, D2 1, and D3 1. Any change on the data inputs will be reflected at the outputs while the enable is low. Input levels are inverted at the output.

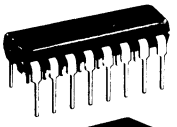
TRUTH TABLE

Enable	Select	D0	D1	Q
L	L	ϕ	L	H
L	L	ϕ	H	L
L	H	L	ϕ	H
L	H	H	ϕ	L
H	ϕ	ϕ	ϕ	L

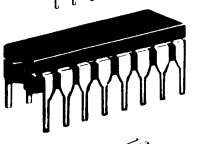
ϕ = Don't Care

V_{CC} Pin 16 (4)
V_{EE} Pin 8 (12)

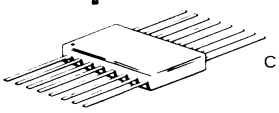
P_D = 218 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ (Data to Q)
3.2 ns typ (Select to Q)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10159 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10559 only

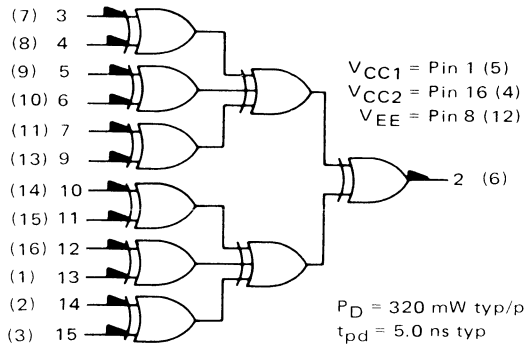
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C Min	−55°C Max	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	I_E	–	58	–	58	–	53	–	58	–	58	mAdc
Input Current	I_{inH}											μAdc
Pin 9		–	380	–	360	–	225	–	225	–	225	
Pins 3,4,5,6,7,10,11,12,13		–	425	–	400	–	250	–	250	–	250	
Switching Times												ns
Propagation Delay	t_{pd}											
Data		1.1	4.0	1.1	3.8	1.2	3.3	1.1	3.8	1.1	4.0	
Select		1.5	5.5	1.5	5.3	1.5	5.0	1.5	5.3	1.5	5.5	
Enable		1.4	5.5	1.4	5.3	1.5	5.0	1.4	5.3	1.4	5.5	
Rise Time, Fall Time (20% to 80%)	t+,t−	1.0	3.8	1.0	3.7	1.1	3.5	1.0	3.7	1.0	3.8	ns

−55°C and +125°C test values apply to MC105xx devices only.

MC10160/MC10560

12-BIT PARITY GENERATOR-CHECKER

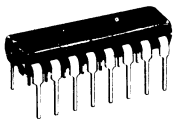


V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

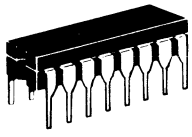
P_D = 320 mW typ/pkg (No Load)
t_{pd} = 5.0 ns typ

The MC10160/MC10560 consists of nine EXCLUSIVE-OR gates in a single package, internally connected to provide odd parity checking or generation. Output goes high when an odd number of inputs are high. Unconnected inputs are pulled to low logic levels allowing parity detection and generation for less than 12 bits.

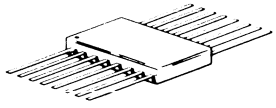
INPUT	OUTPUT
Sum of High Level Inputs	Pin 2
Even	Low
Odd	High



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10160 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10560 only

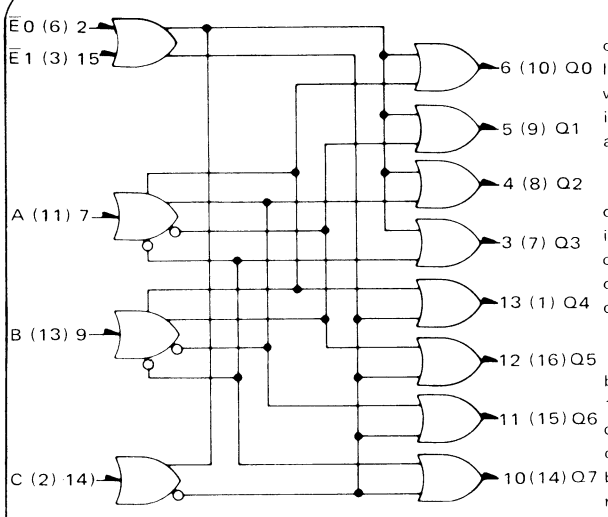
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C Min	−55°C Max	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	I_E	–	86	–	86	–	78	–	86	–	86	mAdc
Input Current	I_{inH}											ns
Pins 3,6,7,11,12,15		–	450	–	425	–	265	–	265	–	265	
Pins 4,5,9,10,13,14		–	375	–	350	–	220	–	220	–	220	
Switching Times												ns
Propagation Delay	t_{pd}	1.6	8.1	1.8	8.1	2.0	7.5	2.0	8.0	1.4	7.9	
Rise Time, Fall Time (20% to 80%)	t+,t−	1.0	3.4	1.1	3.5	1.1	3.3	1.0	3.5	0.9	3.4	ns

−55°C and +125°C test values apply to MC105xx devices only.

MC10161/MC10561

BINARY TO 1-8 DECODER (LOW)



The MC10161/MC10561 is designed to decode a three bit input word to a one of eight line output. The selected output will be low while all other outputs will be high. The enable inputs, when either or both are high, force all outputs high.

The MC10161/MC10561 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders. This design provides the identical 4 ns delay from any address or enable input to any output.

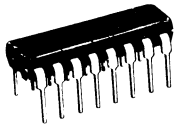
A complete mux/demux operation on 16 bits for data distribution is illustrated in Figure 1. This system, using the MC10136 control counters, has the capability of incrementing, decrementing or holding data channels. When both S0 and S1 are low, the index counters reset, thus initializing both the mux and demux units. The four binary outputs of the counter are buffered by the MC10101s to send twisted-pair select data to the multiplexer/demultiplexer units.

TRUTH TABLE

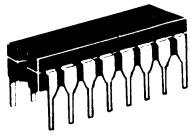
ENABLE INPUTS		INPUTS			OUTPUTS							
$\overline{E}$1	$\overline{E}$0	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	L	H	H	H	H	H	H	H
L	L	L	L	H	H	L	H	H	H	H	H	H
L	L	L	H	L	H	H	L	H	H	H	H	H
L	L	L	H	H	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	L	H	H	H
L	L	H	L	H	H	H	H	H	H	L	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L
H	Φ	Φ	Φ	Φ	H	H	H	H	H	H	H	H
Φ	H	Φ	Φ	Φ	H	H	H	H	H	H	H	H

P_D = 315 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ

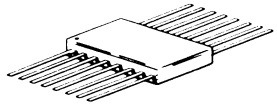
V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10161 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10561 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	84	–	84	–	76	–	84	–	84	mAdc
Input Current	I_{inH}	–	375	–	350	–	220	–	220	–	220	μAdc
Switching Times												ns
Propagation Delay	t_{pd}	1.2	6.5	1.5	6.2	1.5	6.0	1.5	6.4	1.3	7.0	
Rise Time, Fall Time (20% to 80%)	t+, t−	1.0	3.6	1.0	3.3	1.1	3.3	1.1	3.5	1.0	3.9	ns

−55°C and +125°C test values apply to MC105xx devices only.

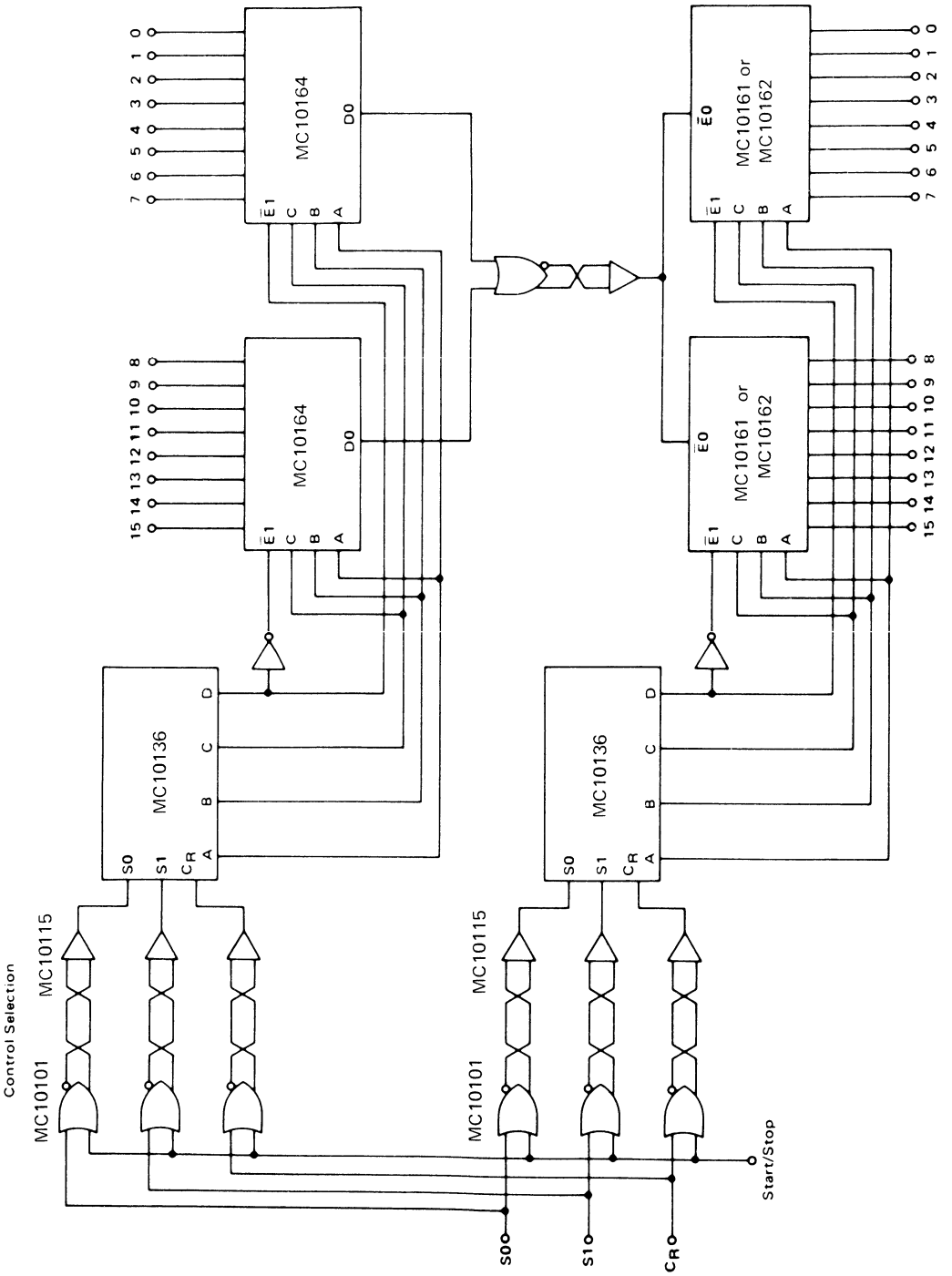
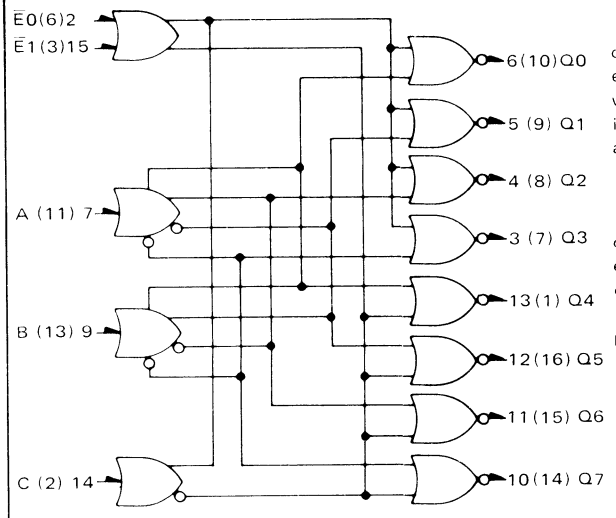


FIGURE 1 – HIGH SPEED 16-BIT MULTIPLEXER/DEMULTIPLEXER

MC10162/MC10562

BINARY TO 1-8 DECODER (HIGH)



The MC10162/MC10562 is designed to convert three lines of input data to a one-of-eight output. The selected output will be high while all other outputs are low. The enable inputs, when either or both are high, force all outputs low.

The MC10162/MC10562 is a true parallel decoder. No series gating is used internally, eliminating unequal delay times found in other decoders.

This device is ideally suited for demultiplexer applications. One of the two enable inputs is used as the data input, while the other is used as a data enable input.

A complete mux/demux operation on 16 bits for data distribution is illustrated in Figure 1 of the MC10161/MC10561 data sheet.

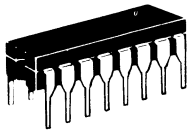
TRUTH TABLE

INPUTS					OUTPUTS							
$\overline{E}$0	$\overline{E}$1	C	B	A	Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
L	L	L	L	L	H	L	L	L	L	L	L	L
L	L	L	L	H	L	H	L	L	L	L	L	L
L	L	L	H	L	L	L	H	L	L	L	L	L
L	L	L	H	H	L	L	L	H	L	L	L	L
L	L	H	L	L	L	L	L	L	H	L	L	L
L	L	H	L	H	L	L	L	L	L	H	L	L
L	L	H	H	L	L	L	L	L	L	L	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H
H	ϕ	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L
ϕ	H	ϕ	ϕ	ϕ	L	L	L	L	L	L	L	L

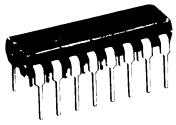
ϕ = Don't Care

P_D = 315 ns typ/pkg (No Load)
t_{pd} = 4.0 ns typ

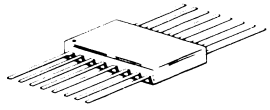
V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10162 only



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10562 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	84	–	84	–	76	–	84	–	84	mAdc
Input Current	I_{inH}	–	375	–	350	–	220	–	220	–	220	μAdc
Switching Times Propagation Delay	t_{pd}	1.2	6.5	1.5	6.2	1.5	6.0	1.5	6.4	1.3	7.0	ns
Rise Time, Fall Time (20% to 80%)	t+,t–	1.0	3.6	1.0	3.3	1.1	3.3	1.1	3.5	1.0	3.9	ns

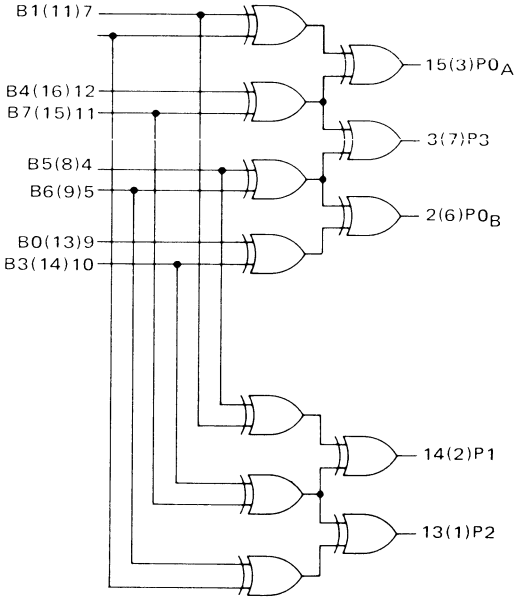
-55°C and +125°C test values apply to MC105xx devices only.

MC10163/MC10563
MC10193/MC10593

ERROR DETECTION - CORRECTION CIRCUITS

The MC10163/MC10563 and the MC10193/MC10593 are error detection and correction circuits. They are building blocks designed for use with memory systems. They offer economy in the design of error detection/correction subsystems for main frame and add-on memory systems. For example, using eight MC10163's together with eight 12-bit parity checkers (MC10160), single-bit error detection/correction and double bit error detection can be done on a word of 64 bit length. Only eight check bits (B0-B7) need be added to the word. A useful feature of this building block is that the MC10193/MC10593 option generates the parity of all inputs to the block. Thus, if the MC10193 is applied in a byte sequence, individual byte parity is automatically available.

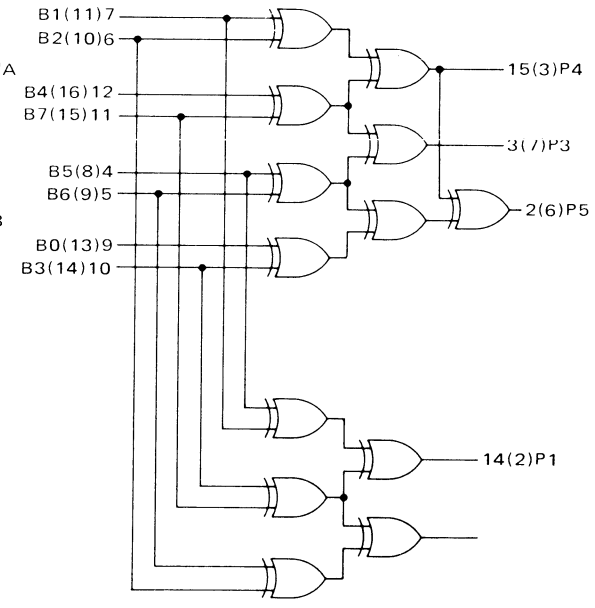
MC10163/MC10563 LOGIC DIAGRAM



IBM CODE

$P0_A$ = B1, B2, B4, B7
$P0_B$ = B0, B3, B5, B6
P1 = B1, B3, B5, B7
P2 = B2, B3, B6, B7
P3 = B4, B5, B6, B7
P_D = 520 mW typ/pkg (No Load)
t_{pd} = 5.0 ns typ

MC10193/MC10593 LOGIC DIAGRAM



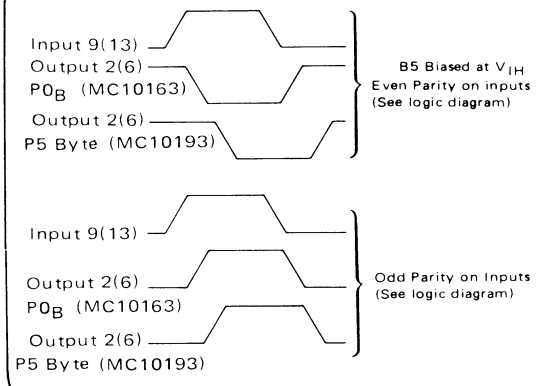
MOTOROLA CODE

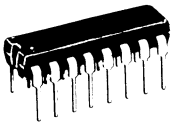
P1 = B1, B3, B5, B7
P2 = B2, B3, B6, B7
P3 = B4, B5, B6, B7
P4 = B1, B2, B4, B7
P5 = Byte (B0, 1, 2, 3, 4, 5, 6, 7)
t_{pd} = 7.5 ns typ (to P5)
= 5.0 ns typ (to P1-P4)

V_{CC1} = Pin 1(5)
V_{CC2} = Pin 16(4)
V_{EE} = Pin 8(12)

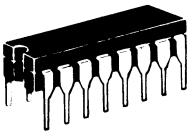
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

SWITCHING TIME WAVEFORMS @ 25°C

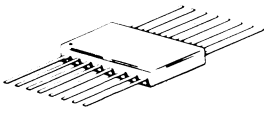




P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10163 and
MC10193 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10563 and
MC10593 only

Characteristic	Symbol	−55°C Min	−55°C Max	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	I_E	–	137	–	137	–	125	–	137	–	137	mAdc
Input Current	I_{inH}											μAdc
Pins 4,6,10		–	375	–	350	–	220	–	220	–	220	
Pins 5,7,9,11,12		–	450	–	425	–	265	–	265	–	265	
Switching Times												ns
Propagation Delay	t_{pd}											
MC10163/MC10563		1.3	7.0	1.3	6.8	1.5	6.5	1.5	7.1	1.5	7.5	
MC10193/MC10593 B to P1–P4		1.3	7.1	1.3	6.8	1.5	6.5	1.5	7.1	1.5	11	
B to P5		1.8	9.1	1.8	8.9	2.0	8.5	2.0	9.2	2.0	10	
Rise Time, Fall Time	t+,t−											ns
(20% to 80%)												
MC10163/MC10563		1.1	4.4	1.1	4.2	1.1	3.9	1.1	4.4	1.1	4.5	
MC10193/MC10593		1.1	4.3	1.1	4.2	1.1	3.9	1.1	4.4	1.1	4.6	

−55°C and +125°C test values apply to MC105xx devices only.

MC10163/MC10563 APPLICATIONS INFORMATION

The MC10163/MC10563 is a building block for generating the modified Hamming single error-correction, double-error-detection (SEC-DED) code used in the IBM370/145 memory. While the MC10163 can also be used for generating other patterns, it is optimized for generating the pattern shown in the H matrix of Figure 1.

When writing into a memory, the MC10163 is used to generate the eight check bits (C0-C32, CT) which are stored with the 64 data bits (B0-B63). These check bits are generated by taking the parity of all data bits marked with an X in the appropriate row of the H matrix. (C0, C1, C32, CT, are even parity; C2, C4, C8, C17, are odd parity.) To generate these check bits with the building blocks, eight MC10163's and eight MC10160 parity checkers are used. One MC10163 is connected to each byte of data and the outputs of these building blocks are connected to the eight MC10160 parity checkers, one for each check bit. Figure 2 shows which connections are required (i.e., C0 is the even parity of output $P0_A$ of the MC10163 on the "zero" byte of data, output $P0_B$ of the "zero" byte, $P0_A$ of the "one" byte, ..., $P0_B$ of the "three byte and data bit 32.)

During the memory read operation, the fetched check bits previously generated (as described) are exclusive-ORed with newly generated C0-C32 to generate syndrome bits S0-S32. Syndrome ST is a special case where ST is the even parity of all eight fetched check bits and all 64 fetched data bits. For determining the type and location of an error:

1. If all syndromes (S0-S32 and ST) are false, there is no error.
2. If ST is true and S0-S32 are false, the CT is in error.
3. If ST is false and one or more of S0-S32 is true, an uncorrectable error has occurred.
4. If ST is true and one or more of S0-S32 is true, simply add the S1-S32 bits to get the binary location of the error (S1 has weight 1, S2 weight 2, S4 weight 4, etc.)

Data bits B0 and B32 are special cases of this location technique: B0 is in error if ST, S0, and S32 are true; B32 is in error if ST, S0, S1, and S32 are true.

FIGURE 1 – 370/145 PATTERN

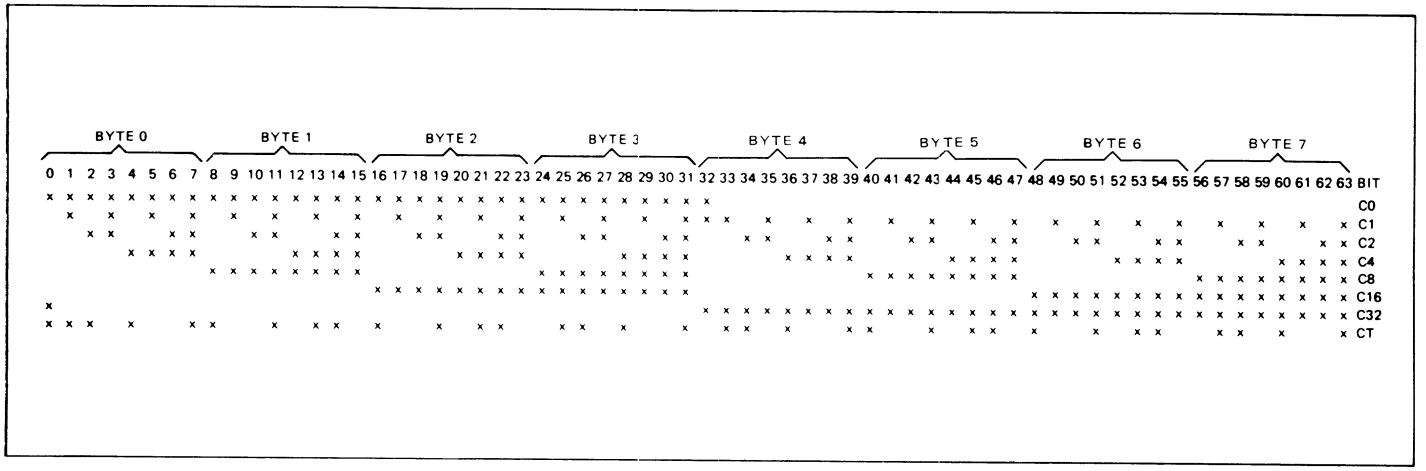


FIGURE 2 – 370/145 PATTERN GENERATION

C0 = $P0_{A0}$	$P0_{B0}$	$P0_{A1}$	$P0_{B1}$	$P0_{A2}$	$P0_{B2}$	$P0_{A3}$	$P0_{B3}$	B(32)
C1 = P10	P11	P12	P13	P14	P15	P16	P17	B(32)
C2 = P20	P21	P22	P23	P24	P25	P26	P27	
C4 = P30	P31	P32	P33	P34	P35	P36	P37	
C8 = $P0_{A1}$	$P0_{B1}$	$P0_{A3}$	$P0_{B3}$	$P0_{A5}$	$P0_{B5}$	$P0_{A7}$	$P0_{B7}$	
C16 = $P0_{A2}$	$P0_{A2}$	$P0_{A3}$	$P0_{B3}$	$P0_{A6}$	$P0_{B6}$	$P0_{A7}$	$P0_{B7}$	
C32 = $P0_{A4}$	$P0_{B4}$	$P0_{A5}$	$P0_{B5}$	$P0_{A6}$	$P0_{B6}$	$P0_{A7}$	$P0_{B7}$	B(0)
CT = $P0_{A0}$	$P0_{B1}$	$P0_{B2}$	$P0_{A3}$	$P0_{A4}$	$P0_{B5}$	$P0_{B6}$	$P0_{A7}$	B(0)

Where for P_{NM}: N = MC10163 Output
M = Byte Number

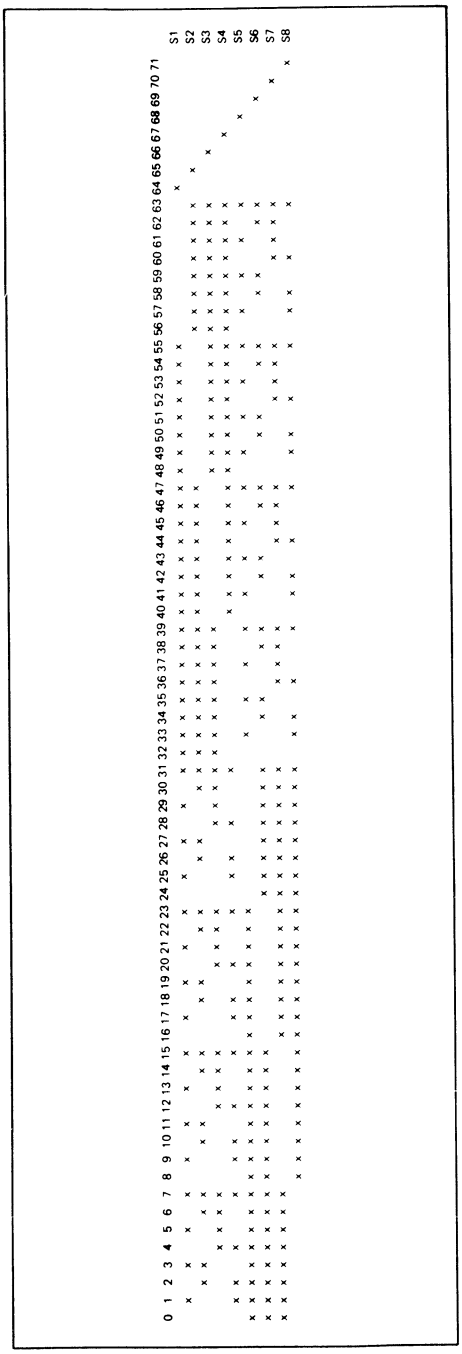


FIGURE 3 – MOTOROLA PATTERN EXAMPLE

The MC10193/MC10593 is a building block for generating modified Hamming SEC-DED codes. It can be used for any length data word and for a variety of codes. The MC10193 is optimized for codes organized on a byte repetitive basis and has the advantage of automatically supplying whole byte parity (P5 output). While it is possible to use a number of criteria for choosing a pattern, the pattern of Figure 3 was chosen on the basis of speed and ease of error location decode. As can be seen in the H matrix of Figure 3, the pattern is repetitive by byte with the various rows generated by only five combinations of bit parities within the bytes. For the 64 bit data word in the example of Figure 3, the eight check bits (B64 to B71) are generated by the odd parity of all data bits indicated by an X in the appropriate row. The syndromes S1 to S8 are generated by including the fetched check bits in the same generator that originally generated the check bits.

The pattern of Figure 3 is easily generated by using eight MC10193 devices, one for each data byte and eight MC10160 parity checkers, one for each syndrome/check bit. The connections of building blocks and parity checkers are shown in tabular form in Figure 4 and in schematic form in Figure 6.

Once the syndrome bits (S1 to S8) have been formed from fetched data (B0 to B63) and fetched check bits (B64 to B71), the determination of type and location of error is simply done:

1. If all syndromes are false, there is no error.
2. If one syndrome is true, the corresponding check bit is in error.
3. If more than one syndrome is true, and the parity of all syndromes is even, a multiple (uncorrectable) error has occurred.
4. If more than one syndrome is true, and the parity of all syndromes is odd, a single error has occurred and is easily located by the circuit of Figure 5.

Figure 5 gives the error location circuit for the example pattern. The outputs EB0 to EB6 are a one-of-eight-high code giving the byte in error. Outputs EC0 to EC3 give the binary location of the bit in error within the located byte. Since this location process can occur simultaneously with the determination of error type described, the entire error correction sequence (using a toggling fetched data latch) takes less than 20 ns. This is because an error occurrence detector is a simple ORing of S1 to S8. The error locator has simultaneously located the error which is then corrected as through the error was a single (and therefore correctable) error. The parity of syndromes then determines if the error was indeed single, and interrupts the CPU if the error was an uncorrectable (multiple) error. Since uncorrec-

table data is unusable without special handling, the CPU would be interrupted anyway; therefore this automatic correction of any error as if it were single does not create any problems. This fast error correction technique allows single erorr correction on a non interrupt basis with only a 20 ns memory system access time penalty.

These techniques can, of course, be extended to large or smaller data words.

FIGURE 4 – M2 PATTERN BUILDING BLOCK

S1 =	P10	P11	P12	P13	P54	P55	P56	B(64)
S2 =	P20	P21	P22	P23	P54	P55	P57	B(65)
S3 =	P30	P31	P32	P33	P54	P56	P57	B(66)
S4 =	P40	P41	P42	P43	P55	P56	P57	B(67)
S5 =	P14	P15	P16	P17	P50	P51	P52	B(68)
S6 =	P24	P25	P26	P27	P50	P51	P53	B(69)
S7 =	P34	P35	P36	P37	P50	P52	P53	B(70)
S8 =	P44	P45	P46	P47	P51	P52	P53	B(71)

Where for P_{NM}: N = MC10193 Output
M = Byte Number

FIGURE 5 – M2 PATTERN CORRECTION MATRIX

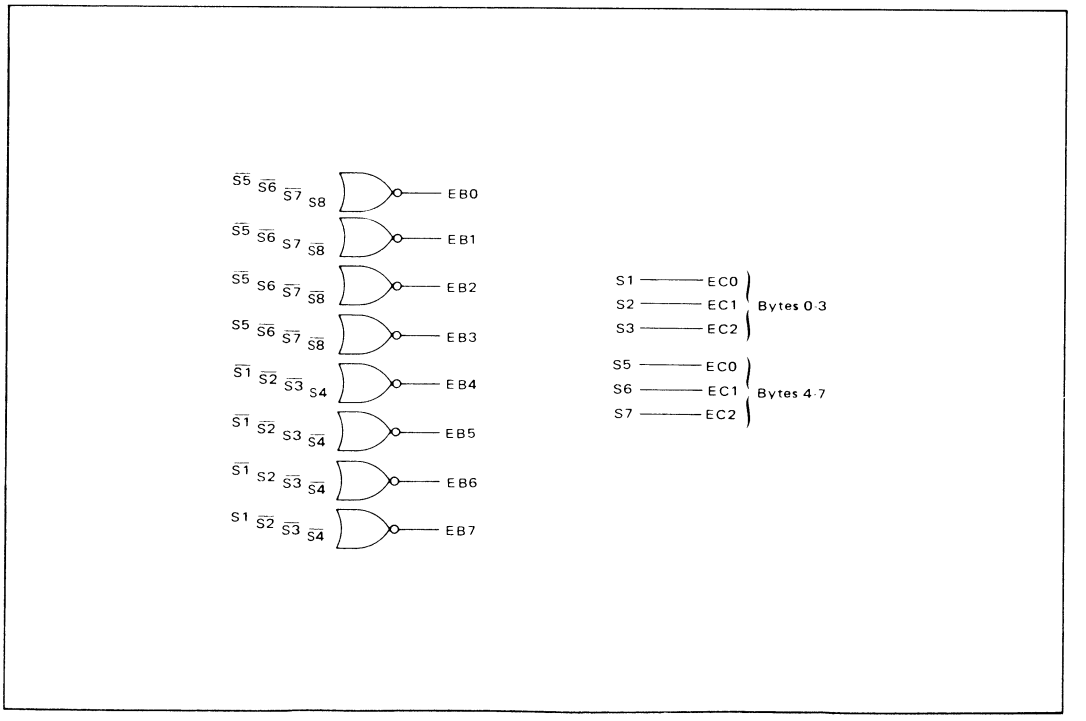
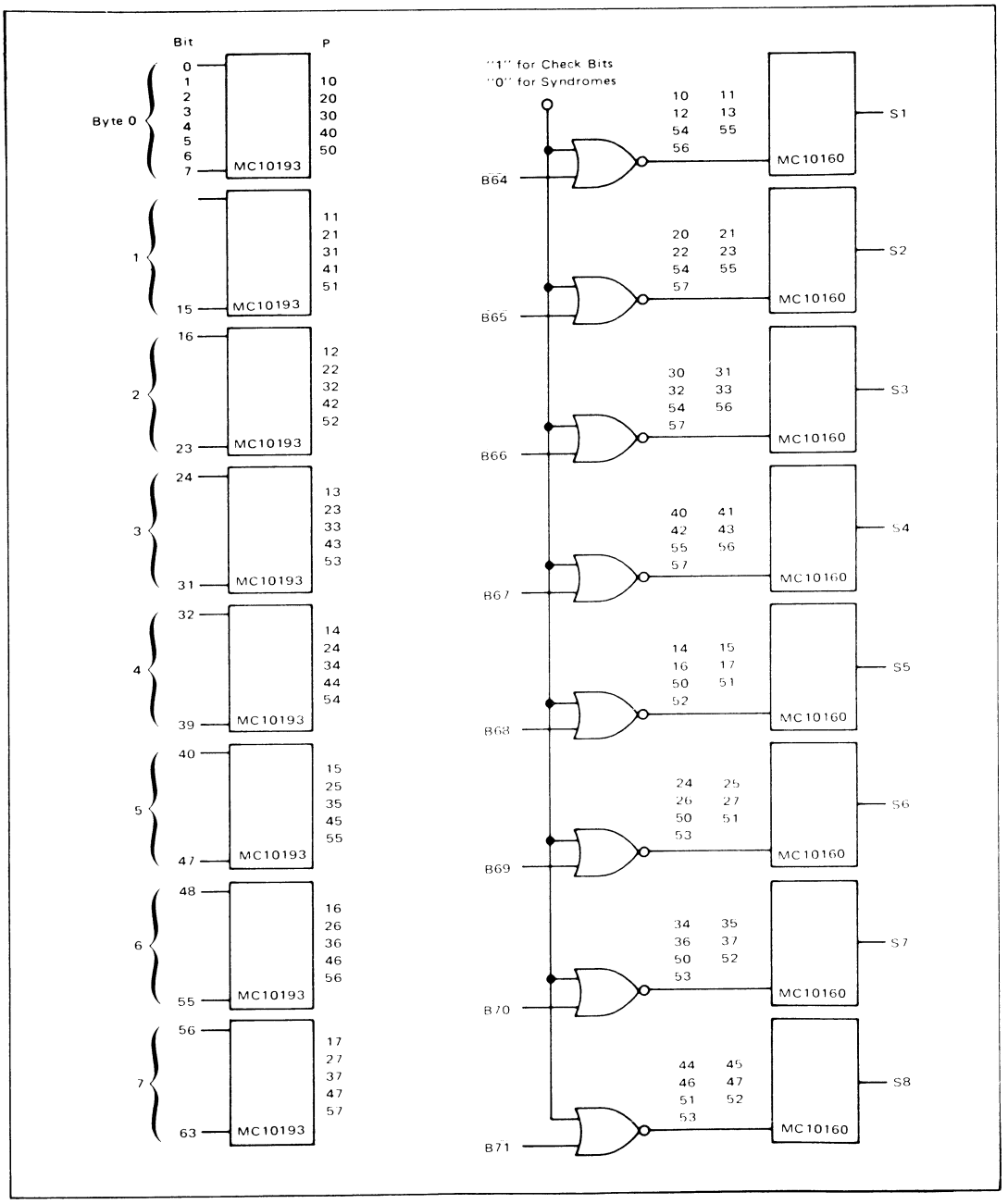
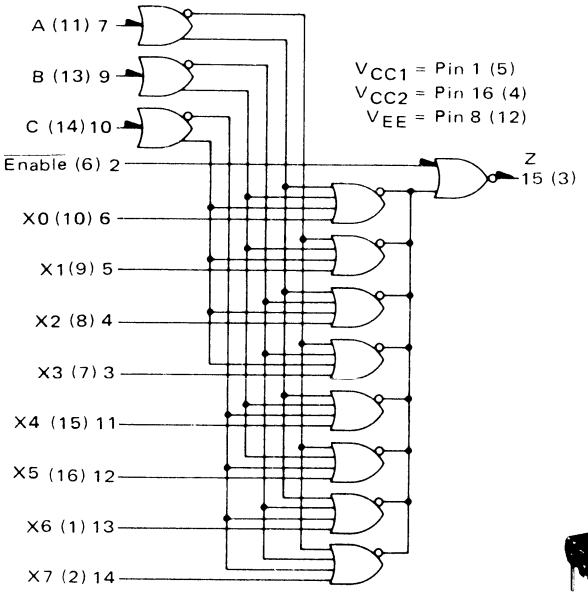


FIGURE 6 – SYNDROME AND CHECK BIT GENERATOR, M2 PATTERN



MC10164/MC10564

8-LINE MULTIPLEXER



The MC10164/MC10564 can be used wherever data multiplexing or parallel to serial conversion is desirable. Full parallel gating permits equal delays through any data path. The output of the MC10164 incorporates a buffer gate with eight data inputs and an enable. A high level on the enable forces the output low. The MC10164 can be connected directly to a data bus, due to its open emitter output and output enable.

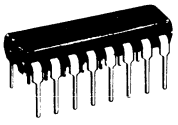
Figure 1 illustrates how a 1-of-64 line multiplexer can be built with eight MC10164's wire ORed at their outputs and one MC10161 to drive the enables on each multiplexer, without speed degradation over a single MC10164 being experienced.

P_D = 310 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ (Data to output)

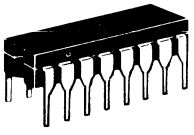
TRUTH TABLE

$\overline{\text{ENABLE}}$	ADDRESS INPUTS C	B	A	Z
L	L	L	L	X0
L	L	L	H	X1
L	L	H	L	X2
L	L	H	H	X3
L	H	L	L	X4
L	H	L	H	X5
L	H	H	L	X6
L	H	H	H	X7
H	φ	φ	φ	L

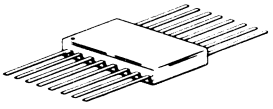
φ = Don't Care



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10164 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



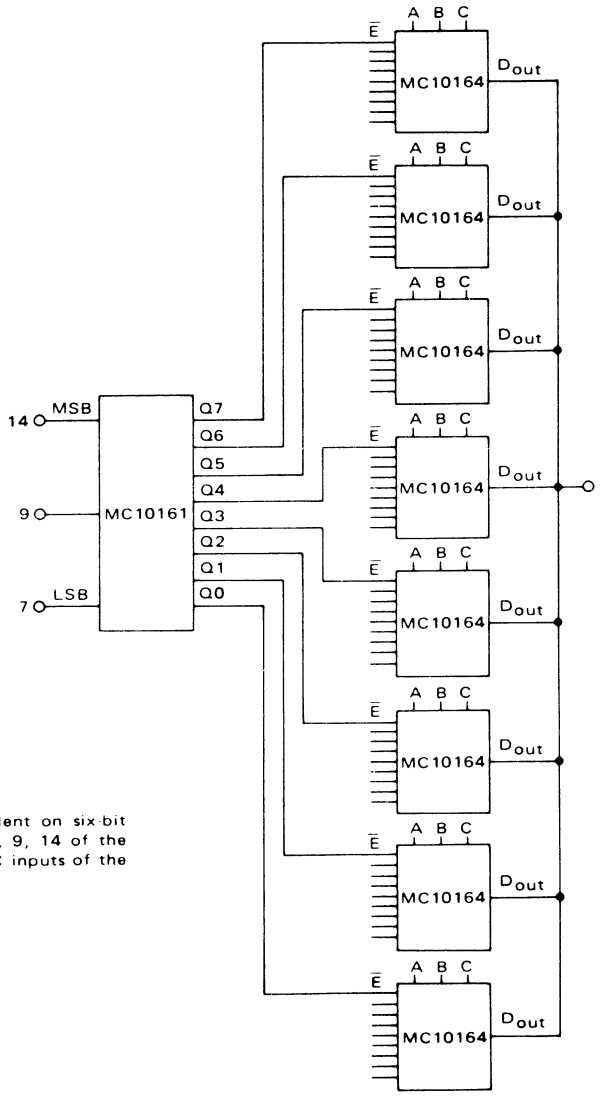
F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10564 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C Min	−55°C Max	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	I_E	–	83	–	83	–	75	–	83	–	83	mAdc
Input Current	I_{inH}	–	450	–	425	–	265	–	265	–	265	μAdc
Switching Times												ns
Propagation Delay	t_{pd}											
X0-X7		1.3	4.6	1.5	4.7	1.5	4.5	1.6	4.8	1.2	4.5	
A, B, C		1.8	6.1	1.9	6.3	2.0	6.0	2.2	6.5	1.9	6.0	
$\overline{\text{Enable}}$		0.9	3.0	0.9	3.3	1.0	2.9	1.0	3.1	0.9	2.9	
Rise Time, Fall Time (20% to 80%)	t+,t−	0.9	3.3	0.9	3.3	1.1	3.3	1.2	3.6	0.9	3.4	ns

-55°C and +125°C test values apply to MC105xx devices only.

FIGURE 1 – 1-OF-64 LINE MULTIPLEXER



The Bit chosen is dependent on six-bit code present on inputs 7, 9, 14 of the MC10161 and the A, B, C inputs of the MC10164.

MC10165/MC10565

8-INPUT PRIORITY ENCODER

TRUTH TABLE

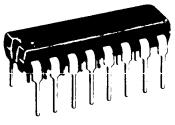
DATA INPUTS								OUTPUTS			
D0	D1	D2	D3	D4	D5	D6	D7	Q3	Q2	Q1	Q0
H	☆	☆	☆	☆	☆	☆	☆	H	L	L	L
L	H	☆	☆	☆	☆	☆	☆	H	L	L	H
L	L	H	☆	☆	☆	☆	☆	H	L	H	L
L	L	L	H	☆	☆	☆	☆	H	L	H	H
L	L	L	L	H	☆	☆	☆	H	H	L	L
L	L	L	L	L	H	☆	☆	H	H	L	H
L	L	L	L	L	L	H	☆	H	H	H	L
L	L	L	L	L	L	L	H	H	H	H	H
L	L	L	L	L	L	L	L	L	L	L	L

☆ Don't Care

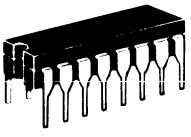
P_D = 545 mW typ/pkg (No Load)
t_{pd} = 7.0 ns typ (Data to Output)

The MC10165/MC10565 is a device designed to encode eight inputs to a binary coded output. The output code is that of the highest order input. Any input of lower priority is ignored. Each output incorporates a latch allowing synchronous operation. When the clock is low the outputs follow the inputs and latch when the clock goes high.

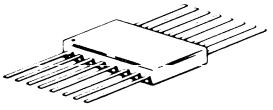
The input is active when high (e.g., the three binary outputs are low when input D0 is high). The Q3 output is high when any input is high. This allows direct extension into another priority encoder when more than eight inputs are necessary.



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10165 only



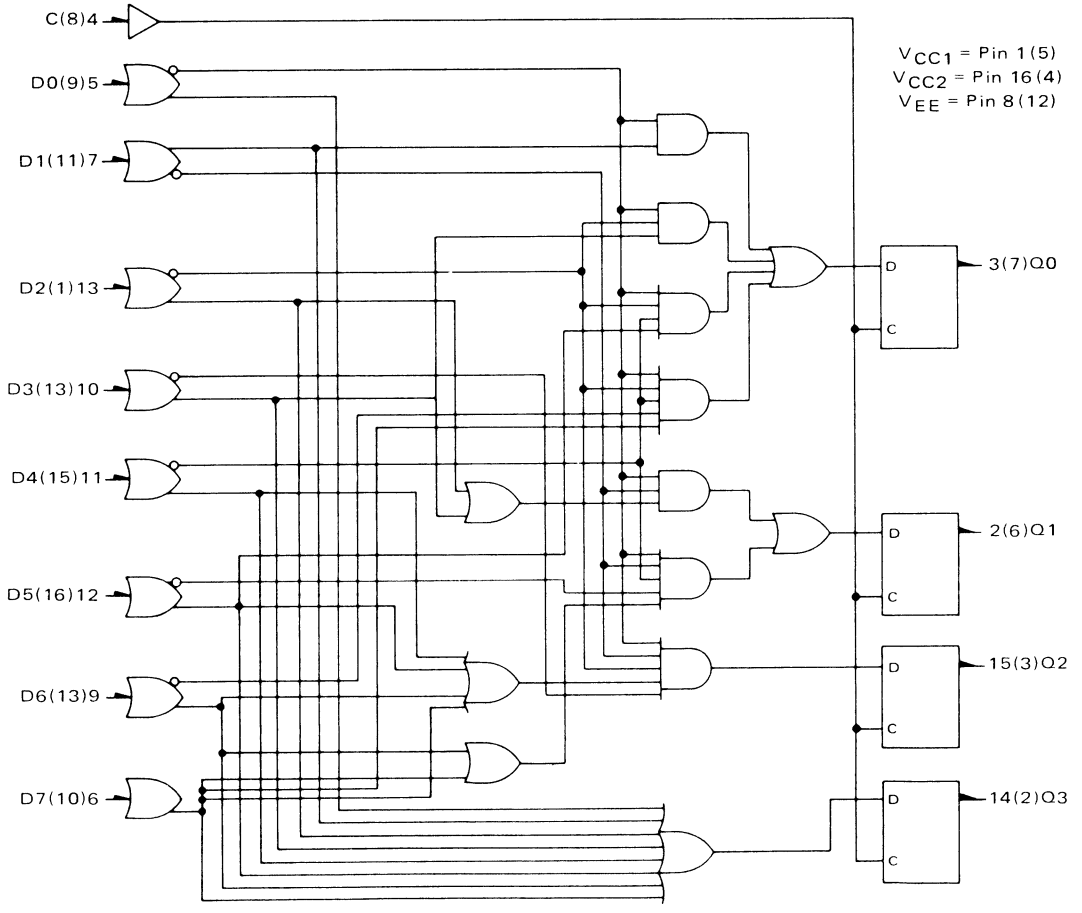
L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10565 only

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	144	–	144	–	131	–	144	–	144	mAdc
Input Current	I_{inH}											μAdc
Pin 4		–	415	–	390	–	245	–	245	–	245	
Pin 5,6,7,9,10,11,12,13		–	375	–	350	–	220	–	220	–	220	
Switching Times												ns
Propagation Delay	t_{pd}											
Data		2.0	7.5	2.0	7.0	2.0	7.0	2.0	8.0	2.0	8.5	
Clock		1.5	5.0	1.5	4.5	1.5	4.0	1.5	4.5	1.5	5.5	
Rise Time, Fall Time (20% to 80%)	t+,t−	1.1	3.8	1.1	3.5	1.1	3.3	1.1	3.5	1.1	4.5	ns
Setup Time	t_{set}	6.0	–	6.0	–	6.0	–	6.0	–	6.0	–	ns
Hold Time	t_{hold}	1.0	–	1.0	–	1.0	–	1.0	–	1.0	–	ns

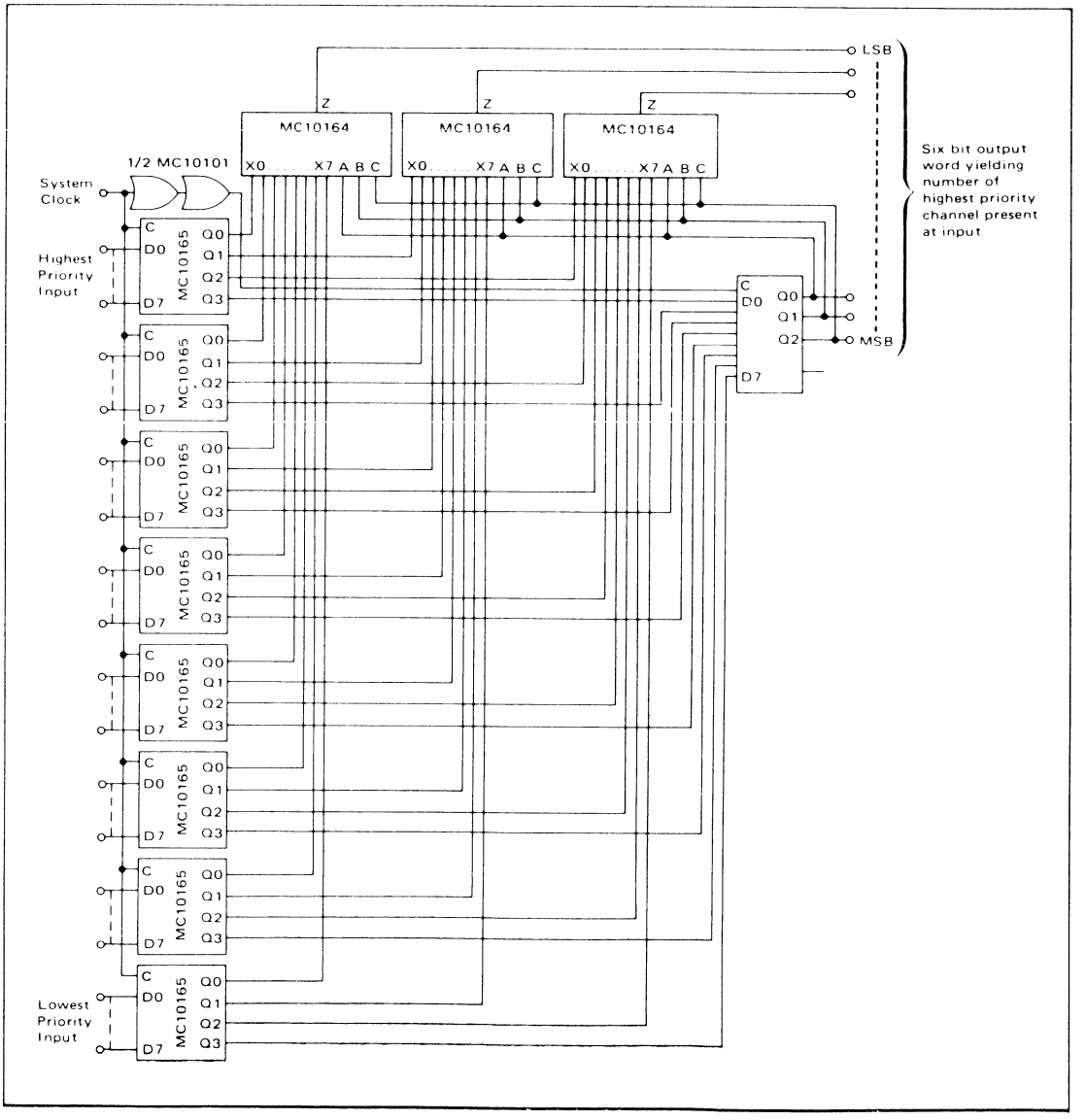
−55°C and +125°C test values apply to MC105xx devices only.



Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

A typical application of the MC10165/MC10565 is the decoding of system status on a priority basis. A 64 line priority encoder is shown in the figure below. System status lines are connected to this encoder such that, when a given condition exists, the respective input will be at a logic high level. This scheme will select the one of 64 different system conditions, as represented at the encoder inputs, which has priority in determining the next system operation to be performed. The binary code showing the address of the highest priority input present will appear at the encoder outputs to control other system logic functions.

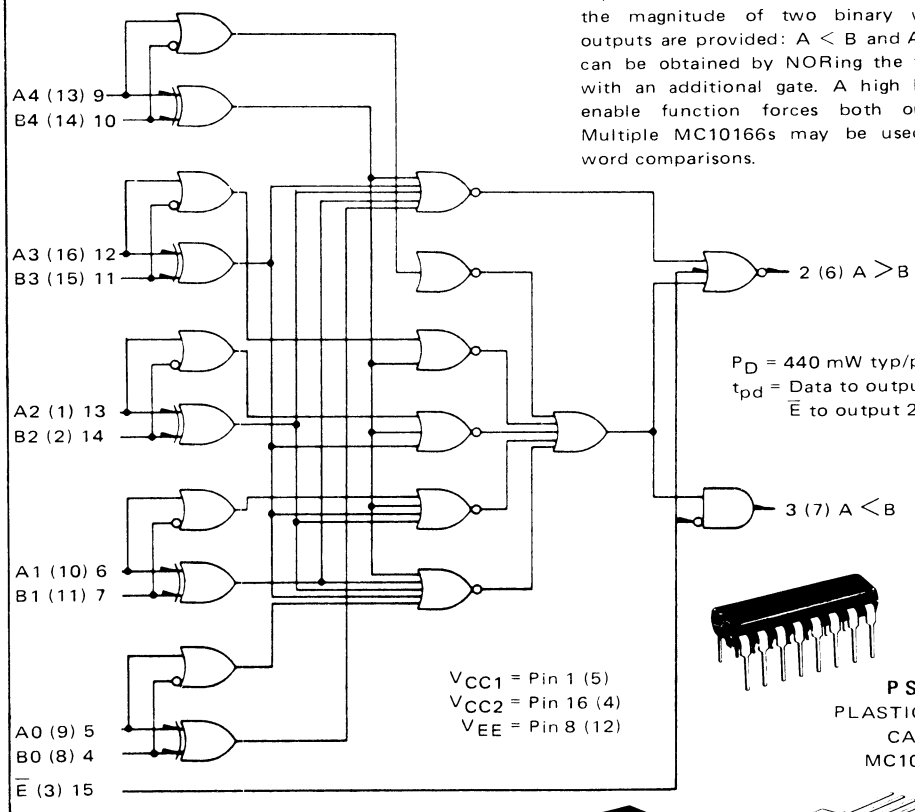
64-LINE PRIORITY ENCODER



MC10166/MC10566

5-BIT MAGNITUDE COMPARATOR

The MC10166/MC10566 is a high speed expandable 5-bit comparator for comparing the magnitude of two binary words. Two outputs are provided: A < B and A > B. A = B can be obtained by NORing the two outputs with an additional gate. A high level on the enable function forces both outputs low. Multiple MC10166s may be used for larger word comparisons.



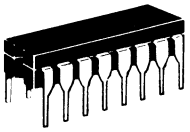
P_D = 440 mW typ/pkg (No Load)
t_{pd} = Data to output 6.0 ns typ
$\overline{E}$ to output 2.5 ns typ

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

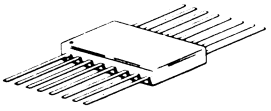
P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10166 only

TRUTH TABLE

Inputs			Outputs	
$\overline{E}$	A	B	A < B	A > B
H	X	X	L	L
L	Word A = Word B		L	L
L	Word A > Word B		L	H
L	Word A < Word B		H	L



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10566 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	117	–	117	–	106	–	117	–	117	mAdc
Input Current	I_{inH}	–	375	–	350	–	220	–	220	–	220	μAdc
Switching Times												ns
Propagation Delay	t_{pd}											
Data		1.0	8.2	1.0	8.0	1.0	7.6	1.0	8.4	1.0	8.9	
Enable		1.0	3.9	1.0	3.8	1.0	3.6	1.0	4.0	1.0	4.2	
Rise Time, Fall Time (20% to 80%)	t+,t−	1.1	3.8	1.0	3.6	1.1	3.5	1.1	3.8	1.1	4.1	ns

−55°C and +125°C test values apply to MC105xx devices only.

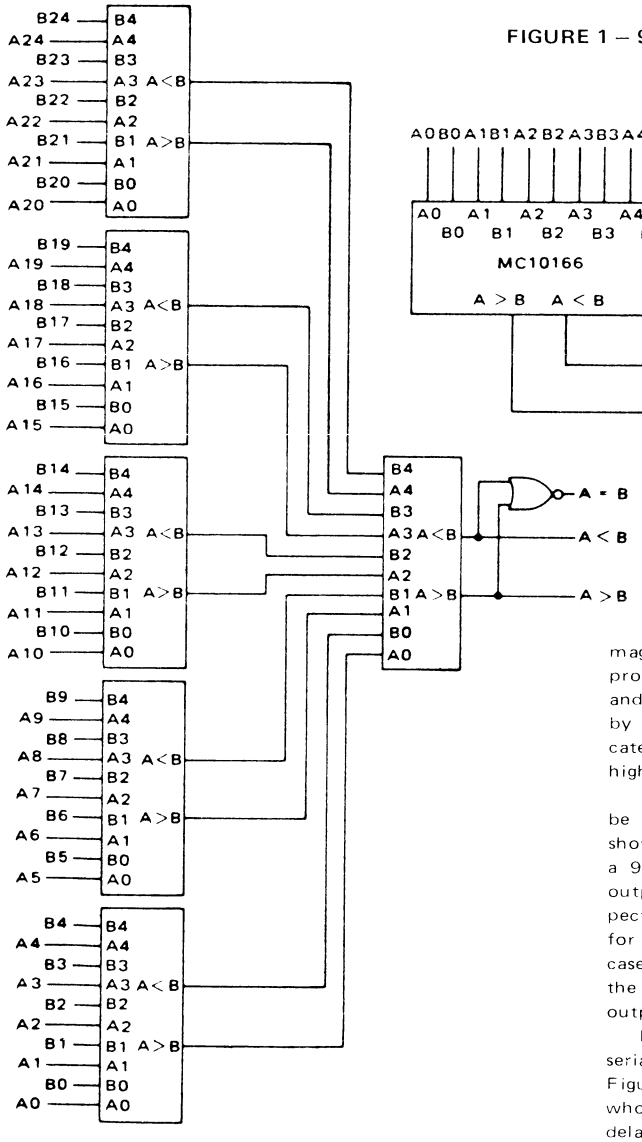
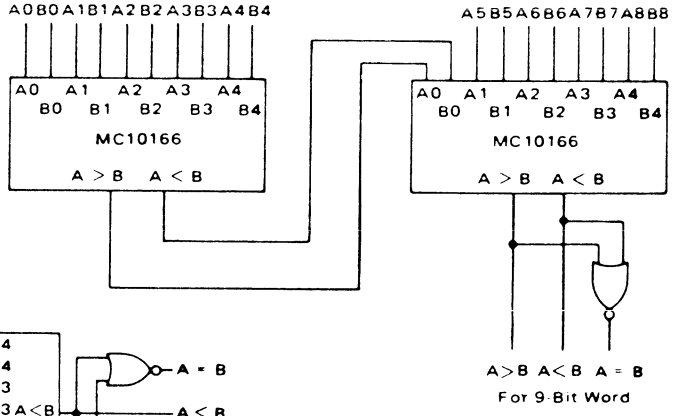


FIGURE 2 – 25-BIT MAGNITUDE COMPARATOR

FIGURE 1 – 9-BIT MAGNITUDE COMPARATOR



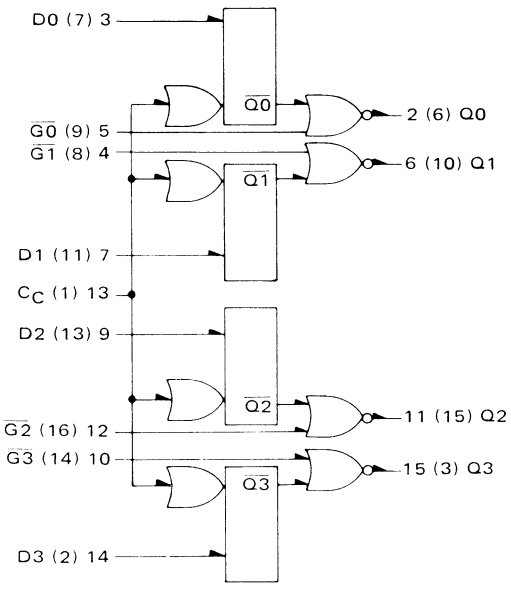
The MC10166/MC10566 compares the magnitude of two 5 bit words. Two outputs are provided which give a high level for A > B and A < B. The A = B function can be obtained by wireORing these outputs (a low level indicates A = B) or by NORing the outputs (a high level indicates A = B).

For longer word lengths, the MC10166 can be serially expanded or cascaded. Figure 1 shows two devices in a serial expansion for a 9-bit word length. The A > B and A < B outputs are fed to the A0 and B0 inputs respectively of the next device. The connection for an A = B output is also shown. The worst case delay time of serial expansion is equal to the number of comparators times the data to output delay.

For shorter delay times than possible with serial expansion, devices can be cascaded. Figure 2 shows a 25 bit cascaded comparator whose worst case delay is two data-to-output delays. The cascaded scheme can be extended to longer word lengths.

MC10168/MC10568

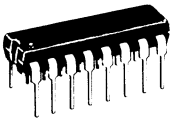
QUAD LATCH



P_D = 310 mW typ/pkg (No Load)
t_{pd}: $\overline{G}$ to Q = 2 ns typ
D to Q = 3 ns typ
C to Q = 4 ns typ

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

The MC10168/MC10568 is a quad latch with common clocking to all four latches. Separate output enabling gates are provided for each latch, allowing direct wiring to a bus. When the clock is high, outputs will follow the D inputs. Information is latched on the negative-going transition of the clock.

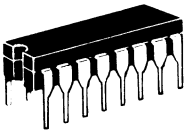


P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10168 only

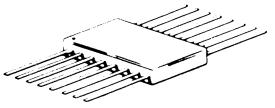
TRUTH TABLE

$\overline{G}$	C	D	Q_n+1
H	Ø	Ø	L
L	L	Ø	Q_n
L	H	L	L
L	H	H	H

Ø = don't care



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10568 only

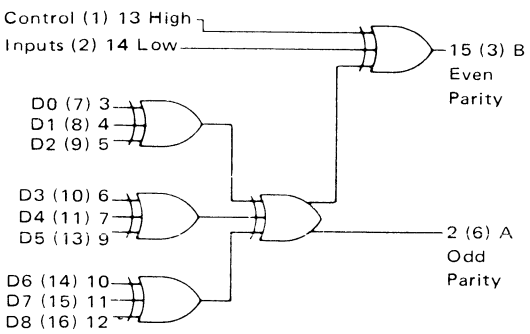
Numbers at ends of terminals denote pin numbers for L and P package
Numbers in parenthesis denote pin numbers for F package

Characteristic	Symbol	−55°C Min	−55°C Max	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	I_E	–	83	–	82	–	75	–	82	–	83	mAdc
Input Current	I_{inH}											μAdc
Pins 3,7,9,14		–	415	–	390	–	245	–	245	–	245	
Pins 4,5,10,12		–	450	–	425	–	265	–	265	–	265	
Pin 13		–	495	–	460	–	290	–	290	–	290	
Switching Times												ns
Propagation Delay	t_{pd}											
Data		1.0	5.8	1.0	5.6	1.0	5.4	1.1	5.9	1.0	6.3	
$\overline{\text{Gate}}$		1.0	3.4	1.0	3.2	1.0	3.1	1.0	3.4	1.0	3.6	
Clock		1.0	6.1	1.0	5.8	1.0	5.6	1.2	6.2	1.0	6.6	
Rise Time, Fall Time (20% to 80%)	t+, t−	1.0	3.9	1.0	3.6	1.1	3.5	1.1	3.8	1.0	4.0	ns
Setup Time	t_{set}	2.5	–	2.5	–	2.5	–	2.5	–	2.5	–	ns
Hold Time	t_{hold}	1.0	–	1.0	–	1.0	–	1.0	–	1.0	–	ns

−55°C and +125°C test values apply to MC105xx devices only.

MC10170/MC10570

9 + 2-BIT PARITY GENERATOR-CHECKER



The MC10170/MC10570 is an 11-bit parity circuit, which is segmented into 9 data bits and 2 control bits.

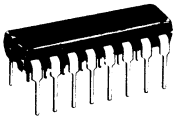
Output A generates odd parity on 9 bits; that is, Output A goes high for an odd number of high logic levels on the bit inputs in only 2 gate delays.

The Control Inputs can be used to expand parity to larger numbers of bits with minimal delay or can be used to generate even parity. To expand parity to larger words, the MC10170 can be used with the MC10160 or other MC10170's.

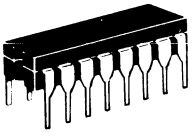
INPUTS	OUTPUTS	
Sums of D Inputs at High Level	Odd Parity	Even Parity
	Output A	Output B
Even	Low	High
Odd	High	Low

V_{CC1} = Pin 1(5)
V_{CC2} = Pin 16(4)
V_{EE} = Pin 8(12)

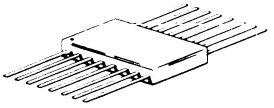
P_D = 300 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ (Control to B)
4.0 ns typ (Data to A)
6.0 ns typ (Data to B)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10170 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10570 only

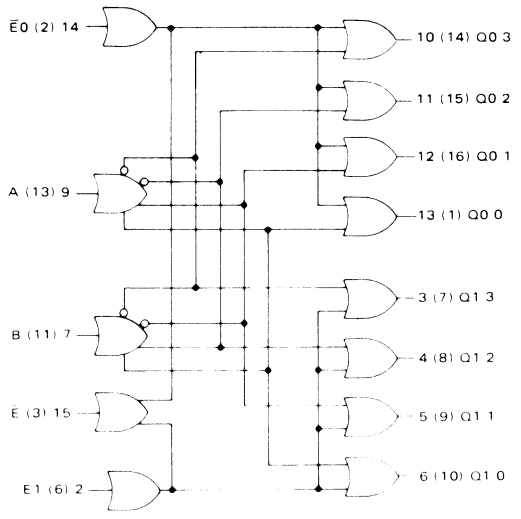
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	78	–	78	–	71	–	78	–	78	mAdc
Input Current	I_{inH}	–	375	–	350	–	220	–	220	–	220	μAdc
Switching Times												ns
Propagation Delay	t_{pd}											
Control		1.5	4.6	1.5	4.2	1.5	4.0	1.5	4.4	1.5	4.8	
Data to A		2.0	7.5	2.0	6.6	2.0	6.0	2.0	6.6	2.0	8.0	
Data to B		4.0	10	4.0	9.5	4.0	8.8	4.0	9.5	4.0	10.5	
Rise Time, Fall Time (20% to 80%)	t+,t−	1.5	4.5	1.5	4.3	1.5	3.9	1.5	4.3	1.5	4.8	ns

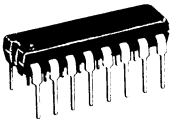
−55°C and +125°C test values apply to MC105xx devices only.

MC10171/MC10571

DUAL BINARY TO 1-4 DECODER (LOW)

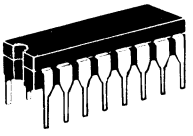


The MC10171/MC10571 is a binary-coded 2 line to dual 4 line decoder with selected outputs low. With either $\overline{E}$0 or $\overline{E}$1 high, the corresponding selected 4 outputs are high. The common enable $\overline{E}$, when high, forces all outputs high.



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10171 only

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)



L SUFFIX
CERAMIC PACKAGE
CASE 620

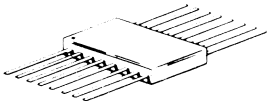
P_D = 325 mW typ/pkg (No Load)

t_{pd} = 4.0 ns typ

TRUTH TABLE

ENABLE INPUTS			INPUTS		OUTPUTS							
E	E0	E1	A	B	Q10	Q11	Q12	Q13	Q00	Q01	Q02	Q03
L	L	L	L	L	L	H	H	H	L	H	H	H
L	L	L	L	H	H	L	H	H	H	L	H	H
L	L	L	H	L	H	H	L	H	H	H	L	H
L	L	L	H	H	H	H	H	L	H	H	H	L
L	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	L	L	L	H	H	H	H	H	H	H
H	ϕ	ϕ	ϕ	ϕ	H	H	H	H	H	H	H	H

ϕ = Don't Care



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10571 only

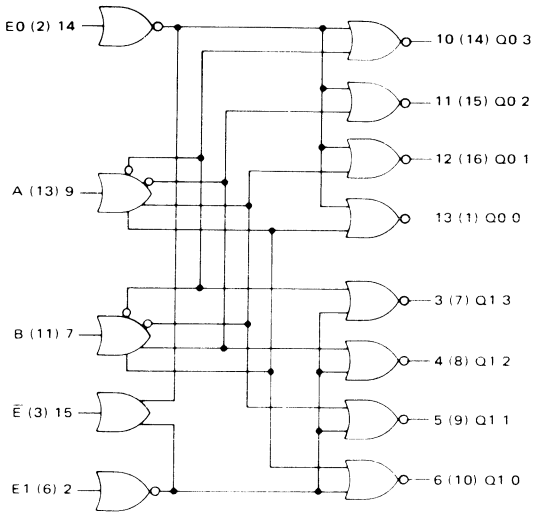
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	85	–	85	–	77	–	85	–	85	mAdc
Input Current	I_{inH}	–	375	–	350	–	220	–	220	–	220	μAdc
Switching Times												ns
Propagation Delay	t_{pd}	1.3	6.5	1.5	6.2	1.5	6.0	1.5	6.4	1.2	7.0	
Rise Time, Fall Time	t+,t−	1.0	3.6	1.0	3.3	1.1	3.3	1.1	3.4	1.0	3.9	ns

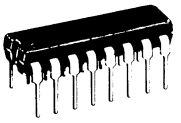
55°C and +125°C test values apply to MC105xx devices only.

MC10172/MC10572

DUAL BINARY TO 1-4 DECODER (HIGH)

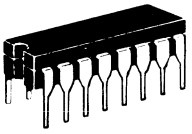


The MC10172/MC10572 is a binary-coded 2 line to dual 4 line decoder with selected outputs high. With either E0 or E1 low, the corresponding selected 4 outputs are low. The common enable E, when high, forces all outputs low.



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10172 only

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)



L SUFFIX
CERAMIC PACKAGE
CASE 620

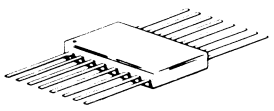
P_D = 325 mW typ/pkg
(No Load)

t_{pd} = 4.0 ns typ

TRUTH TABLE

$\bar{E}$	E1	E0	A	B	Q1 0	Q1 1	Q1 2	Q1 3	Q0 0	Q0 1	Q0 2	Q0 3
L	H	H	L	L	H	L	L	L	H	L	L	L
L	H	H	L	H	L	H	L	L	L	H	L	L
L	H	H	H	L	L	L	H	L	L	L	H	L
L	H	H	H	H	L	L	L	H	L	L	L	H
L	L	H	L	L	L	L	L	L	H	L	L	L
L	H	L	L	L	H	L	L	L	L	L	L	L
H	Ø	Ø	Ø	Ø	L	L	L	L	L	L	L	L

Ø = Don't Care



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10572 only

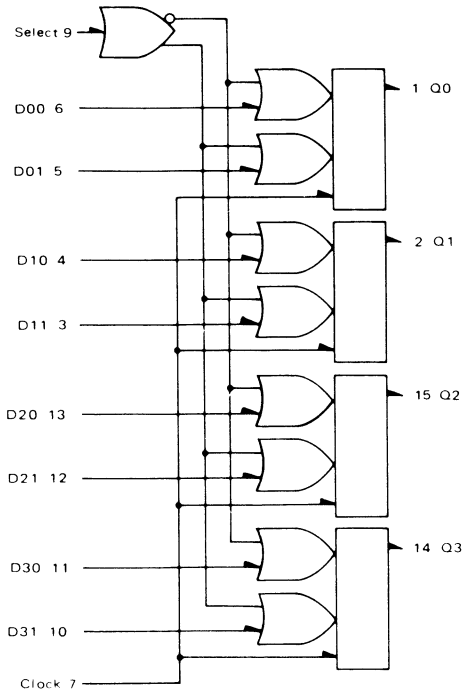
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	85	–	85	–	77	–	85	–	85	mAdc
Input Current	I_{inH}	–	375	–	350	–	220	–	220	–	220	μAdc
Switching Times												ns
Propagation Delay	t_{pd}	1.3	6.5	1.5	6.2	1.5	6.0	1.5	6.4	1.2	7.0	
Rise Time, Fall Time	t+,t−	1.0	3.6	1.0	3.3	1.1	3.3	1.1	3.4	1.0	3.9	ns

−55°C and +125°C test values apply to MC105xx devices only.

MC10173

QUAD 2-INPUT MULTIPLEXER/LATCH



P_D = 275 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ

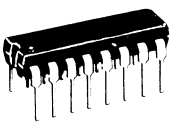
The MC10173 is a quad two channel multiplexer with latch. It incorporates common clock and common data select inputs. The select input determines which data input is enabled. A high (H) level enables data inputs D00, D10, D20, and D30 and a low (L) level enables data inputs D01, D11, D21, D31. Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information.

TRUTH TABLE

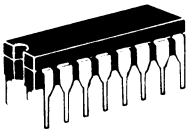
SELECT	CLOCK	$Q0_{n+1}$
H	L	D00
L	L	D01
ϕ	H	$Q0_n$

ϕ = Don't Care

V_{CC} = Pin 16
V_{EE} = Pin 8



P SUFFIX
PLASTIC PACKAGE
CASE 648

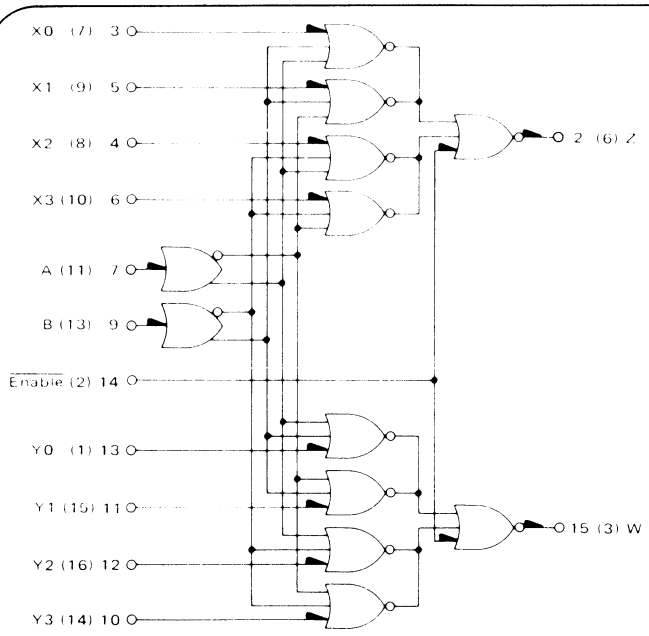


L SUFFIX
CERAMIC PACKAGE
CASE 620

Characteristic	Symbol	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit
Power Supply Drain Current	I_E	–	73	–	66	–	73	mAdc
Input Current	I_{inH}							μAdc
Pins 3,4,5,6,10,11,12,13		–	470	–	295	–	295	
Pins 7,9		–	400	–	250	–	250	
Switching Times								ns
Propagation Delay	t_{pd}							
Data		0.8	3.7	1.0	3.5	1.1	5.3	
Clock		1.6	7.2	1.6	6.8	1.4	6.8	
Select		1.1	6.2	1.3	5.7	1.2	6.7	
Rise Time, Fall Time (20% to 80%)	t+,t−	1.2	4.0	1.5	3.5	1.4	4.0	ns
Setup Time	t_{set}							ns
Data		2.0	–	2.0	–	2.0	–	
Select		3.0	–	3.0	–	3.0	–	
Hold Time	t_{hold}							ns
Data		2.5	–	2.5	–	2.5	–	
Select		1.5	–	1.5	–	1.5	–	

MC10174/MC10574

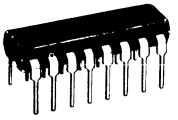
DUAL 4-TO-1 MULTIPLEXER



TRUTH TABLE

ENABLE	ADDRESS INPUTS		OUTPUTS	
$\overline{E}$	B	A	Z	W
H	ϕ	ϕ	L	L
L	L	L	X0	Y0
L	L	H	X1	Y1
L	H	L	X2	Y2
L	H	H	X3	Y3

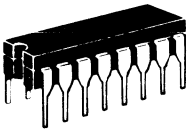
ϕ = Don't Care



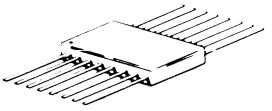
P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10174 only

P_D = 305 mW typ/pkg (No Load)
t_{pd} = 3.5 ns typ (Data to output)

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10574 only

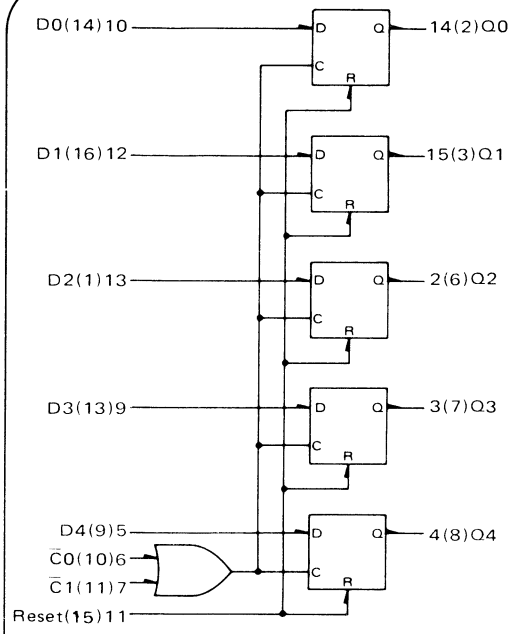
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	80	–	80	–	73	–	80	–	80	mAdc
Input Current	I_{inH}											μAdc
Pins 3,4,5,6,7,9,10,11,12,13		–	375	–	350	–	220	–	220	–	220	
Pin 14		–	565	–	525	–	330	–	330	–	330	
Switching Times												ns
Propagation Delay	t_{pd}											
Data		1.3	4.6	1.4	4.8	1.5	4.5	1.4	4.8	1.2	4.5	
Select (A,B)		1.8	6.1	1.9	6.4	2.0	6.0	2.1	6.4	1.9	6.0	
$\overline{\text{Enable}}$		0.9	3.0	1.0	3.1	1.0	2.9	0.9	3.2	0.9	2.9	
Rise Time, Fall Time (20% to 80%)	t+,t−	0.9	3.3	1.0	3.4	1.1	3.3	1.1	3.6	0.9	3.4	ns

−55°C and +125°C test values apply to MC105xx devices only.

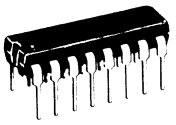
MC10175/MC10575

QUINT LATCH



The MC10175/MC10575 is a high speed, low power quint latch. It features five D type latches with common reset and a common two-input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are "OR"ed together.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. The reset input is enabled only when the clock is in the high state.



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10175

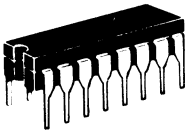
TRUTH TABLE

D	$\overline{C0}$	$\overline{C1}$	Reset	Q_{n+1}
L	L	L	ϕ	L
H	L	L	ϕ	H
ϕ	H	ϕ	L	Q_n
ϕ	ϕ	H	L	Q_n
ϕ	H	ϕ	H	L
ϕ	ϕ	H	H	L

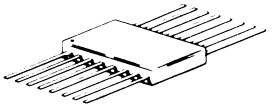
ϕ = don't care

P_D = 400 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ (Data to Output)

V_{CC1} = Pin 1(5)
V_{CC2} = Pin 16(4)
V_{EE} = Pin 8(12)



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10575 only

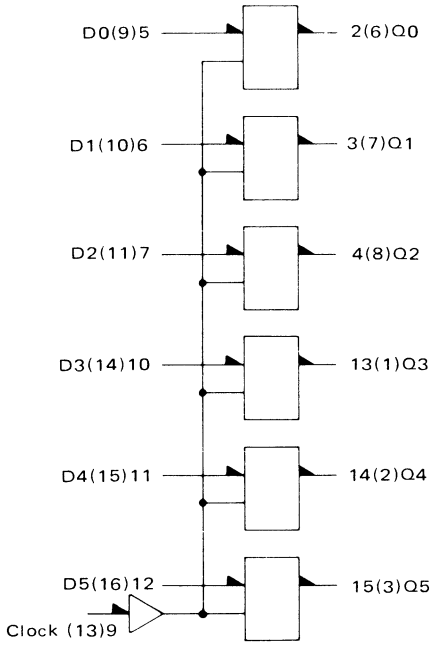
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	107	–	107	–	97	–	107	–	107	mAdc
Input Current	I_{inH}											μAdc
Pins 5,6,7,9,10,12,13		–	495	–	460	–	290	–	290	–	290	
Pin 11		–	1100	–	1000	–	650	–	650	–	650	
Switching Times												ns
Propagation Delay	t_{pd}											
Data		1.0	3.8	1.0	3.6	1.0	3.5	1.0	3.6	1.0	4.1	
Clock		1.0	4.6	1.0	4.7	1.0	4.3	1.0	4.4	1.0	5.0	
Reset		1.0	4.2	1.0	4.0	1.0	3.9	1.0	4.2	1.0	4.6	
Rise Time, Fall Time (20% to 80%)	t+, t–	1.0	3.8	1.0	3.6	1.1	3.5	1.1	3.7	1.0	4.1	ns
Setup Time	t_{set}	2.5	–	2.5	–	2.5	–	2.5	–	2.5	–	ns
Hold Time	t_{hold}	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10176/MC10576

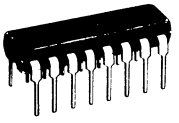
HEX D MASTER-SLAVE FLIP-FLOP



P_D = 460 mW typ/pkg (No Load)
f_{toggle} = 150 MHz (typ)

V_{CC1} = Pin 1(5)
V_{CC2} = Pin 16(4)
V_{EE} = Pin 8(12)

The MC10176/MC10576 contains six high-speed, master slave type "D" flip-flops. Clocking is common to all six flip-flops. Data is entered into the master when the clock is low. Master to slave data transfer takes place on the positive-going Clock transition. Thus, outputs may change only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device.



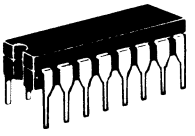
P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10176 only

CLOCKED TRUTH TABLE

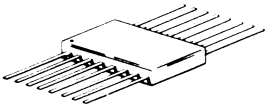
C	D	Q_{n+1}
L	ϕ	Q_n
H*	L	L
H*	H	H

ϕ = Don't Care

*A clock H is a clock transition from a low to a high state.



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10576 only

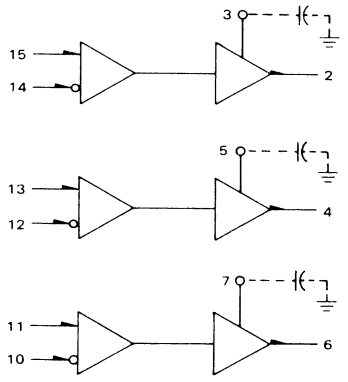
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	121	–	121	–	110	–	121	–	121	mAdc
Input Current	I_{inH}											μAdc
Pins 5,6,7,10,11,12		–	375	–	350	–	220	–	220	–	220	
Pin 9		–	525	–	495	–	310	–	310	–	310	
Switching Times												ns
Propagation Delay	t_{pd}	1.6	4.9	1.6	4.6	1.6	4.5	1.6	5.0	1.6	5.3	
Rise Time, Fall Time (20% to 80%)	t+,t−	1.0	4.3	1.0	4.1	1.1	4.0	1.1	4.4	1.0	4.7	ns
Setup Time	t_{set}	2.5	–	2.5	–	2.5	–	2.5	–	2.5	–	ns
Hold Time	t_{hold}	1.5	–	1.5	–	1.5	–	1.5	–	1.5	–	ns
Toggle Frequency	f_{Tog}	125	–	125	–	125	–	125	–	125	–	MHz

-55°C and +125°C test values apply to MC105xx devices only.

MC10177

TRIPLE MECL-TO-NMOS TRANSLATOR

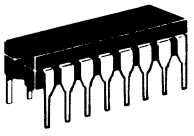


The MC10177 consists of three MECL to MOS translators which convert MECL 10,000 logic levels to NMOS levels. It is designed for use in N-channel memory systems as a Read/Write, Data/Address driver. It may also be used as a high fanout (30) MECL to TTL translator, or in other applications requiring the capability to drive high capacitive loads. A separate lead from each of the three translators is brought out of the package. These leads may be connected to V_{SS}, or to an external capacitor (0.01 to 0.05 μF to ground), for waveform improvement, and short circuit protection. When connection is made to an external capacitor, V_{SS} line fluctuations due to transient currents are also reduced.

V_{CC} = Gnd = Pins 1, 16
V_{EE} = Pin 8 = −5.2 Vdc ± 5%
V_{SS} = Pin 9 (+5.0 Vdc or +6.0 Vdc ± 10%)

Max Load: 350 pF
P_D = 1.0 W typ/pkg @ 5.0 MHz
Operating Rate: 5.0 MHz typ
(all 3 translators in use simultaneously
Input: MECL 10,000 (differential)
Output: NMOS +0.5 V V_{OLmax}
+ 3.0 V V_{OHmin}*

*May be raised by increasing V_{SS}.



L SUFFIX
CERAMIC PACKAGE
CASE 620

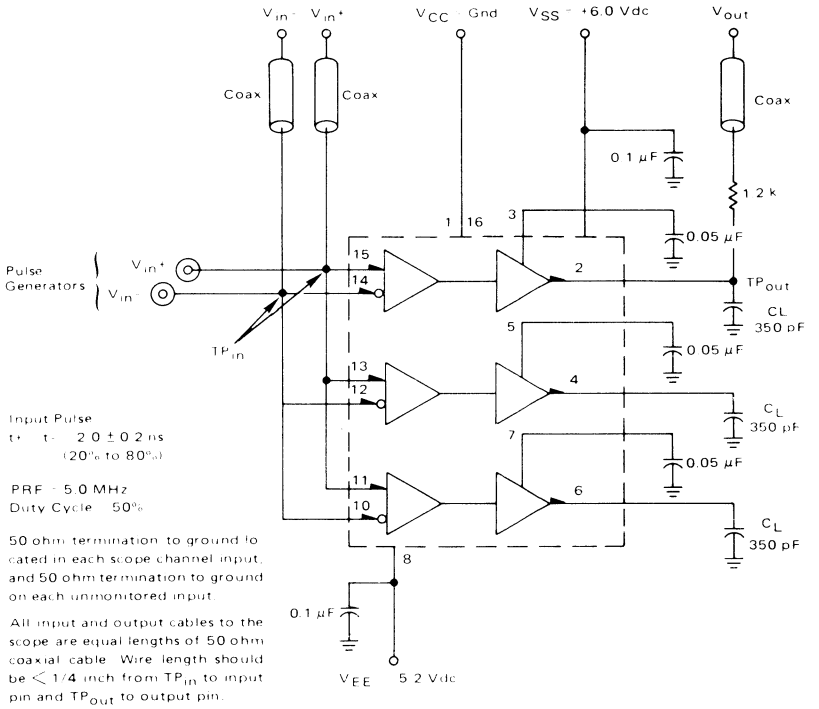
ELECTRICAL CHARACTERISTICS

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES							
	Volts					mAdc ± 1%		
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	I_{OL1}	I_{OL2}	I_{OH}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2	+1.0	+20	−15
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2	+1.0	+20	−15
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2	+1.0	+20	−15

NOTE: V_{SS} (Pin 9) = +5.0 Vdc unless otherwise specified.

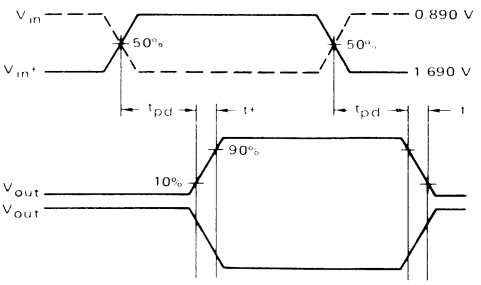
Characteristic	Symbol	−30°C		+25°C		+85°C		Unit	Conditions	
		Min	Max	Min	Max	Min	Max			
Power Supply Drain Current	I_E	–	106	–	96	–	106	mAdc	Pin 9 and all inputs and outputs open.	
Negative	I_{SSO}	–	88	–	88	–	88	mAdc	All inputs and outputs open.	
Positive Output Low	I_{SSL}	–	88	–	88	–	88		$V_{in} = V_{IHmax}$ (Pins 10, 12, 14), V_{ILmin} (Pins 11, 13 15).	
Output High	I_{SSH}	–	44	–	44	–	44		$V_{in} = V_{ILmin}$ (Pins 10, 12, 14), V_{IHmax} (Pins 11, 13, 15).	
Input Current	I_{inH}	–	1.6	–	1.0	–	1.0	mA	$V_{in} = V_{IHmax}$ to P.U.T., V_{ILmin} to the other input of that gate. Test one input at a time.	
Input Leakage Current	I_{CBO}	–	1.5	–	1.0	–	1.0	μAdc	$V_{in} = V_{EE}$ to P.U.T., V_{IHmax} to the other input of that gate. Test one input at a time.	
Logic "1" Output Voltage	V_{OH}	3.0	–	3.0	–	3.0	–	Vdc	V_{SS} = +5.0 Vdc	$V_{in} = V_{IHmax}$ (Pins 11, 13 15), V_{ILmin} (Pins 10, 12, 14). I_{OH} = −15 mAdc.
		4.0	–	4.0	–	4.0	–		V_{SS} = +6.0 Vdc	
Logic "0" Output Voltage	V_{OL}	–	0.5	–	0.5	–	0.5	Vdc	I_{OL1} = +1.0 mAdc	$V_{in} = V_{IHmax}$ (Pins 10, 12 14), V_{ILmin} (Pins 11, 13 15).
		–	0.6	–	0.6	–	0.6		I_{OL2} = +20 mAdc	
Logic "1" Threshold Voltage	V_{OHA}	3.0	–	3.0	–	3.0	–	Vdc	V_{SS} = +5.0 Vdc	$V_{in} = V_{IHAmin}$ (Pins 11, 13, 15, one at a time), V_{ILmin} (Pins 10, 12, 14). I_{OH} = −15 mAdc.
		4.0	–	4.0	–	4.0	–		V_{SS} = +6.0 Vdc	
Logic "0" Threshold Voltage	V_{OLA}	–	0.5	–	0.5	–	0.5	Vdc	I_{OL1} = +1.0 mAdc	$V_{in} = V_{IHmax}$ (Pins 10, 12, 14), V_{ILAmax} (Pins 11, 13, 15, one at a time).
		–	0.6	–	0.6	–	0.6		I_{OL2} = +20 mAdc	
Output Short-Circuit Current	I_{SC}	−50	−90	−50	−90	−50	−90	mAdc	$V_{in} = V_{ILmin}$ (Pins 10, 12, 14), V_{IHmax} (Pins 11, 13 15). Ground outputs, one at a time.	
Switching Times Propagation Delay	t_{pd}	2.0	12.5	2.0	12.5	2.0	12.5	ns	50% in to 10% or 90% out. See switching time test circuit	
Rise Time, Fall Time	t+, t−	3.0	12	3.0	11	3.0	11	ns	10% to 90%	
Supply Source Current	I_{SS}	–	110	–	110	–	110	mA	@ 5.0 MHz, 350 pF load, V_{SS} = +6.0 Vdc	

SWITCHING TIME TEST CIRCUIT



SWITCHING WAVEFORMS @ 25°C

Switching times are measured after the device under test reaches a stabilized temperature (air flow ≥ 500 lfpm)



MC10178/MC10578

BINARY COUNTER

TRUTH TABLE

INPUTS							OUTPUTS			
R	S0	S1	S2	S3	C1	C2	Q0	Q1	Q2	Q3
H	L	L	L	L	ϕ	ϕ	L	L	L	L
L	H	H	H	H	ϕ	ϕ	H	H	H	H
L	L	L	L	L	H	ϕ	No Count			
L	L	L	L	L	ϕ	H	No Count			
L	L	L	L	L	••		L	L	L	L
L	L	L	L	L	••		H	L	L	L
L	L	L	L	L	••		L	H	L	L
L	L	L	L	L	••		H	H	L	L
L	L	L	L	L	••		L	L	H	L
L	L	L	L	L	••		H	L	H	L
L	L	L	L	L	••		L	H	H	L
L	L	L	L	L	••		H	H	H	L
L	L	L	L	L	••		L	L	L	H
L	L	L	L	L	••		H	L	L	H
L	L	L	L	L	••		L	H	L	H
L	L	L	L	L	••		H	H	L	H
L	L	L	L	L	••		L	L	H	H
L	L	L	L	L	••		H	L	H	H
L	L	L	L	L	••		L	H	H	H
L	L	L	L	L	••		H	H	H	H

ϕ = Don't Care

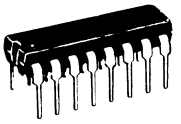
•• V_{IL} ⌐ V_{IH} Clock transition from V_{IL} to V_{IH} may be applied to C1 or C2 or both for same effect

P_D = 370 mW typ/pkg (No Load)
f_{toggle} = 150 MHz (typ)
t_{pd} = 3.5 ns typ (C to Q0)
= 11 ns typ (C to Q3)

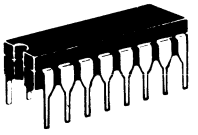
V_{CC1} = Pin 1(5)
V_{CC2} = Pin 16(4)
V_{EE} = Pin 8(12)

The MC10178/MC10578 is a four-bit counter capable of divide-by-two, divide-by-four, divide-by-eight or a divide-by-sixteen function.

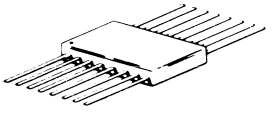
Clock inputs trigger on the positive going edge of the clock pulse. Set and Reset inputs override the clock, allowing asynchronous "set" or "clear". Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.



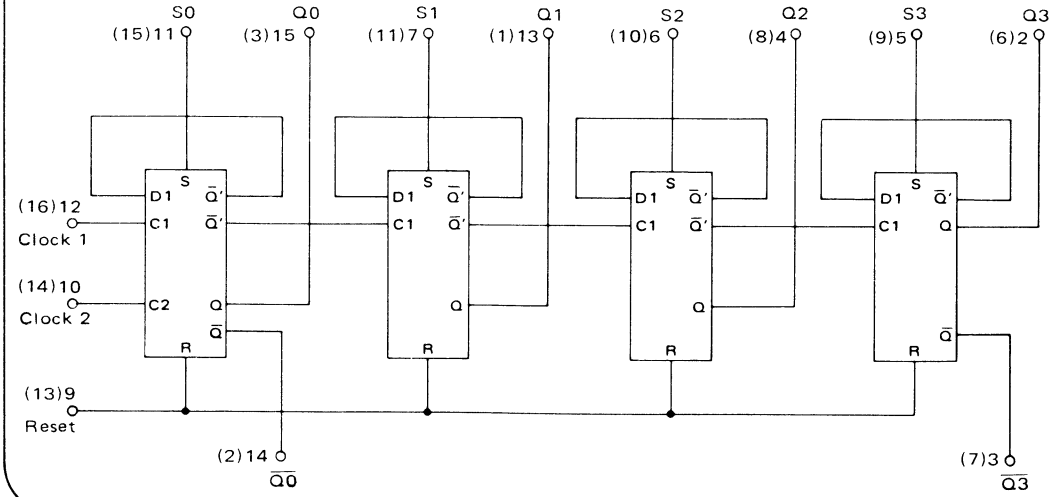
P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10178 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10578 only



Numbers at ends of terminals denote pin numbers for L and P package.
Numbers in parenthesis denote pin numbers for F package.

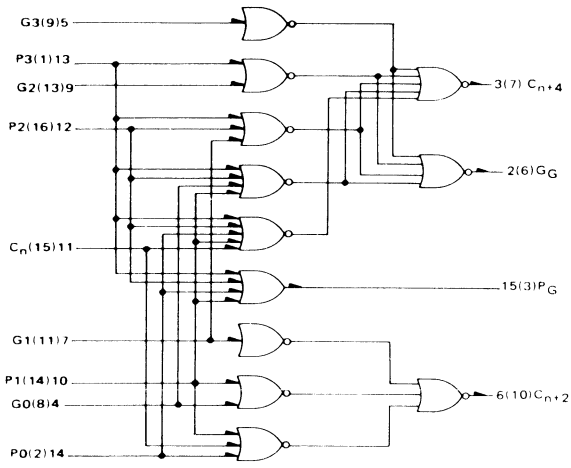
ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	97	–	97	–	88	–	97	–	97	mAdc
Input Current	I_{inH}											μAdc
Pins 10,12		–	415	–	390	–	245	–	245	–	245	
Pins 5,6,7,11		–	375	–	350	–	220	–	220	–	220	
Pin 9		–	700	–	650	–	410	–	410	–	410	
Switching Times												ns
Propagation Delay	t_{pd}											
Clock to Q0		1.4	5.0	1.4	5.0	1.5	4.8	1.5	5.3	1.5	5.6	
Clock to Q1		1.9	9.9	1.9	9.4	2.0	9.2	2.0	9.8	2.0	10.8	
Clock to Q2		2.9	13	2.9	12.3	3.0	12	3.0	12.8	3.0	14	
Clock to Q3		3.9	16	3.9	14.9	4.0	14.5	4.0	15.5	4.0	17	
Set, Reset		1.4	5.6	1.4	5.2	1.5	5.0	1.5	5.5	1.5	6.1	
Rise Time, Fall Time (20% to 80%)	t+,t−	1.1	4.9	1.1	4.7	1.1	4.5	1.1	5.0	1.1	5.3	ns
Counting Frequency	f_{count}	125	–	125	–	125	–	125	–	125	–	MHz

−55°C and +125°C test values apply to MC105xx devices only.

MC10179/MC10579

LOOK-AHEAD CARRY BLOCK



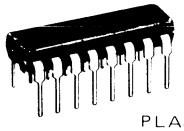
P_D = 300 mW typ/pkg (No Load)
t_{pd} = 3.0 ns typ (Carry, Propagate)
= 4.0 ns typ (Generate)

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

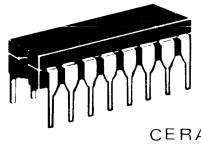
$P_G = P0 + P1 + P2 + P3$
$G_G = (G0 + P1 + P2 + P3)(G1 + P2 + P3)(G2 + P3)\,G3$
$C_{n+2} = (C_n + P0 + P1)(G0 + P1)\,G1$
$C_{n+4} = (C_n + P0 + P1 + P2 + P3)(G0 + P1 + P2 + P3)(G1 + P2 + P3)(G2 + P3)\,G3$

The MC10179/MC10579 is a high speed, low power, standard MECL complex function that is designed to perform the look-ahead carry function. This device can be used with the MC10181/MC10581 4-unit ALU directly, or with the MC10180/MC10580 dual arithmetic unit in any computer, instrumentation or digital communication application requiring high speed arithmetic operation on long words.

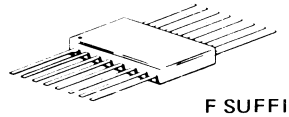
When used with the MC10181/MC10581, the MC10179/MC10579 performs a second order or higher look-ahead. Figure 2 shows a 16-bit look ahead carry arithmetic unit. Second order carry is valuable for longer binary words. As an example, addition of two 32-bit words is improved from 30 nanoseconds with ripple-carry techniques, to 18 nanoseconds with carry look ahead techniques. A block diagram of a 32-bit ALU is shown in Figure 1. The MC10179/MC10579 may also be used in many other applications. It can, for example, reduce system package count when used to generate functions of several variables.



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10179 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10579 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C Min	−55°C Max	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	I_E	–	79	–	79	–	72	–	79	–	79	mAdc
Input Current	I_{inH}											μAdc
Pins 5,9		–	380	–	360	–	225	–	225	–	225	
Pins 4,7,11		–	460	–	430	–	270	–	270	–	270	
Pin 14		–	600	–	565	–	355	–	355	–	355	
Pin 12		–	670	–	630	–	395	–	395	–	395	
Pins 10,13		–	750	–	700	–	440	–	440	–	440	
Switching Times												ns
Propagation Delay	t_{pd}											
G or C_n to Carry; G or P to G_G		1.0	5.9	1.0	5.8	1.0	5.5	1.0	6.1	1.0	6.4	
P to P_G		1.0	3.9	1.0	3.7	1.0	3.5	1.0	3.9	1.0	4.1	
Rise Time, Fall Time (20% to 80%)	t+,t−	1.0	3.9	1.1	3.7	1.1	3.5	1.1	3.9	1.0	4.1	ns

−55°C and +125°C test values apply to MC105xx devices only.

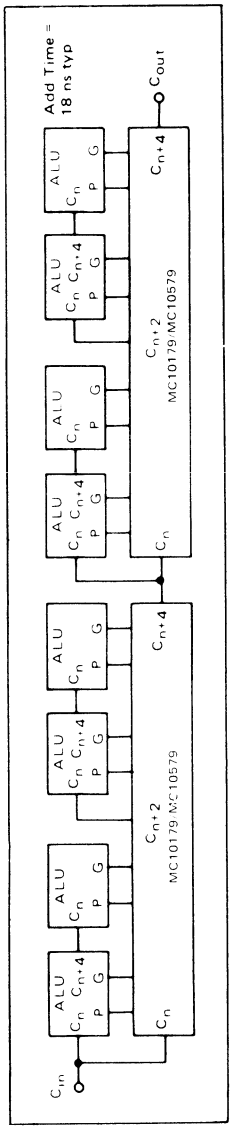


FIGURE 1 – 32-BIT ALU WITH CARRY LOOK-AHEAD

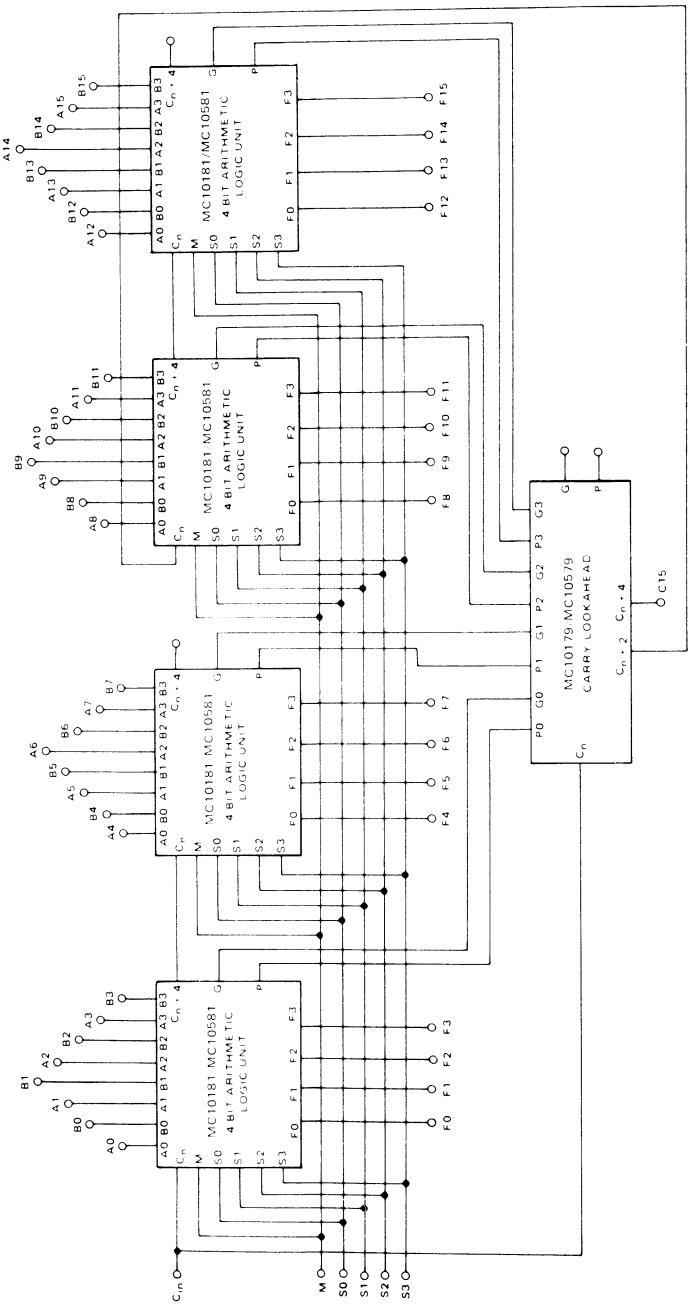
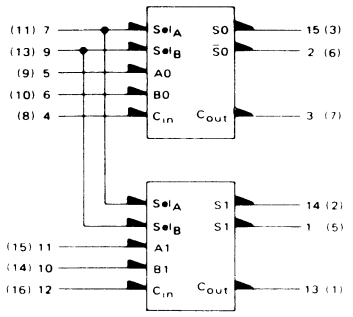


FIGURE 2 – 16-BIT FULL LOOK-AHEAD CARRY ARITHMETIC LOGIC UNIT

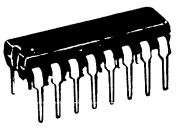
MC10180/MC10580

DUAL 2-BIT ADDER/SUBTRACTOR

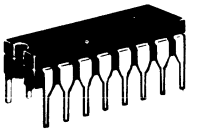


The MC10180/MC10580 is a high speed, low power general-purpose adder/subtracter.

Inputs for each adder are Carry-in, operand A, and operand B; outputs are Sum, $\overline{\text{Sum}}$, and Carry-out; The common Select inputs serve as a control line to invert A for subtract, and a control line to invert B.



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10180 only



L SUFFIX
CERAMIC PACKAGE
CASE 620

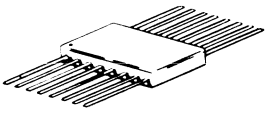
$$A' = \overline{A \oplus Sel_A} = A \odot Sel_A$$

$$B' = \overline{B \oplus Sel_B} = B \odot Sel_B$$

$$S = \overline{C}_{in}(\overline{A}'B' + A'\overline{B}') + C_{in}(A'B' + \overline{A}'\overline{B}')$$

$$C_{out} = C_{in}A' + C_{in}B' + A'B'$$

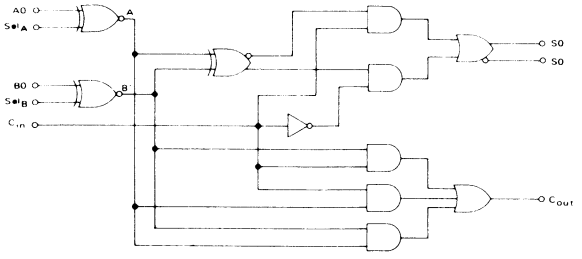
V_{CC} = Pin 16(4)
V_{EE} = Pin 8(12)



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10580 only

P_D = 360 mW typ/pkg (No Load)
t_{pd} = 2.2 ns typ (C_{in} to C_{out})
= 4.5 ns typ (A_0 to S_0 or C_{out})

POSTIVE LOGIC DIAGRAM – 1/2 Of Circuit Shown



FUNCTION SELECT TABLE

Sel_A	Sel_B	Function
H	H	S = A plus B
H	L	S = A minus B
L	H	S = B minus A
L	L	S = 0 minus A minus B

TRUTH TABLE

FUNCTION	INPUTS					OUTPUTS		
	Sel_A	Sel_B	A0	B0	C_{in}	S0	S0	C_{out}
ADD	H	H	L	L	L	L	H	L
	H	H	L	L	H	H	L	L
	H	H	L	H	L	H	L	L
	H	H	L	H	H	L	H	H
	H	H	H	L	L	H	L	L
	H	H	H	L	H	L	H	H
	H	H	H	H	L	L	H	H
	H	H	H	H	H	H	L	H
SUBTRACT	H	L	L	L	L	H	L	L
	H	L	L	L	H	L	H	H
	H	L	L	H	L	H	L	L
	H	L	L	H	H	L	H	H
	H	L	H	L	L	H	L	L
	H	L	H	L	H	L	H	H
	H	L	H	H	L	H	L	L
	H	L	H	H	H	L	H	H
REVERSE SUBTRACT	L	H	L	L	L	H	L	L
	L	H	L	L	H	L	H	H
	L	H	L	H	L	H	L	L
	L	H	L	H	H	L	H	H
	L	H	H	L	L	H	L	L
	L	H	H	L	H	L	H	H
	L	H	H	H	L	L	H	L
	L	H	H	H	H	H	L	H
	L	L	L	L	L	H	L	H
	L	L	L	L	H	H	L	L
	L	L	L	H	L	H	L	H
	L	L	L	H	H	L	H	L
	L	L	H	L	L	H	L	H
	L	L	H	L	H	L	H	L
	L	L	H	H	L	L	H	L
	L	L	H	H	H	H	L	L

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	95	–	95	–	86	–	95	–	95	mAdc
Input Current	I_{inH}											μAdc
Pins 5,6,10,11		–	375	–	350	–	220	–	220	–	220	
Pins 7,9		–	495	–	460	–	290	–	290	–	290	
Pins 4, 12		–	630	–	590	–	370	–	370	–	370	
Switching Times												ns
Propagation Delay	t_{pd}											
Operand, Select		1.0	5.8	1.3	5.8	1.3	5.4	1.1	5.8	1.0	6.3	
Carry-in		1.0	3.6	1.0	3.4	1.0	3.3	0.9	3.6	1.0	3.9	
Rise Time, Fall Time (20% to 80%)	t+,t−	1.0	4.0	1.0	3.8	1.1	3.7	1.1	3.9	1.0	4.3	ns

−55°C and +125°C test values apply to MC105xx devices only.

MC10181/MC10581

4-BIT ARITHMETIC LOGIC UNIT and FUNCTION GENERATOR

POSITIVE LOGIC

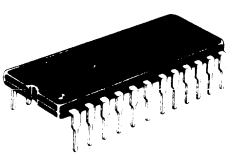
Function Select S3	S2	S1	S0	Logic Functions M is High C = D.C. F	Arithmetic Operation M is Low C_n is low F
L	L	L	L	$F = \overline{A}$	F = A plus 0
L	L	L	H	$F = \overline{A} + \overline{B}$	F = A plus (A • $\overline{B}$)
L	L	H	L	$F = \overline{A} + B$	F = A plus (A • B)
L	L	H	H	F = Logical "1"	F = A times 2
L	H	L	L	$F = \overline{A} \bullet \overline{B}$	F = (A + B) plus 0
L	H	L	H	$F = \overline{B}$	F = (A + B) plus (A • $\overline{B}$)
L	H	H	L	$F = A \oplus B$	F = A plus B
L	H	H	H	$F = A + \overline{B}$	F = A plus (A + B)
H	L	L	L	$F = \overline{A} \bullet B$	F = (A + $\overline{B}$) plus 0
H	L	L	H	$F = A \odot B$	F = A minus B minus 1
H	L	H	L	F = B	F = (A + $\overline{B}$) plus (A • B)
H	L	H	H	F = A + B	F = A plus (A + $\overline{B}$)
H	H	L	L	F = Logical "0"	F = minus 1 (two's complement)
H	H	L	H	F = A • $\overline{B}$	F = (A • $\overline{B}$) minus 1
H	H	H	L	F = A • B	F = (A • B) minus 1
H	H	H	H	F = A	F = A minus 1

The MC10181/MC10581 is a high-speed arithmetic logic unit capable of performing 16 logic operations and 16 arithmetic operations on two four-bit words. Full internal carry is incorporated for ripple through operation.

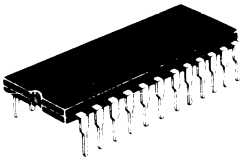
Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S1 through S3) as indicated in the table of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided to allow fast operations on very long words using a second order look ahead. The internal carry is enabled by applying a low level voltage to the mode control input (M).

When used with the MC10179, full-carry look-ahead, as a second order look ahead block, the MC10181 provides high speed arithmetic operations on very long words.

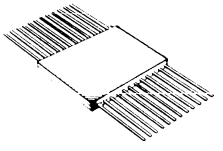
P_D = 600 mW typ/pkg (No Load)
t_{pd} = 6.5 ns typ (A1 to F)
= 3.1 ns typ (C_n to C_{n+4})
= 5.0 ns typ (A1 to P_G or C_{n+4})
= 4.5 ns typ (A1 to G_G)



P SUFFIX
PLASTIC PACKAGE
CASE 649
MC10181 only



L SUFFIX
CERAMIC PACKAGE
CASE 623



F SUFFIX
CERAMIC PACKAGE
CASE 652
MC10581 only

Characteristic	Symbol	−55°C Min	−55°C Max	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	I_E	–	160	–	159	–	145	–	159	–	160	mAdc
Input Current	I_{inH}											μAdc
Pins 9,11,19,20		–	415	–	390	–	245	–	245	–	245	
Pins 10,16,18,21		–	375	–	350	–	220	–	220	–	220	
Pins 13,23		–	340	–	320	–	200	–	200	–	220	
Pins 14,15,17		–	450	–	425	–	265	–	265	–	265	
Pin 22		–	495	–	460	–	290	–	290	–	290	

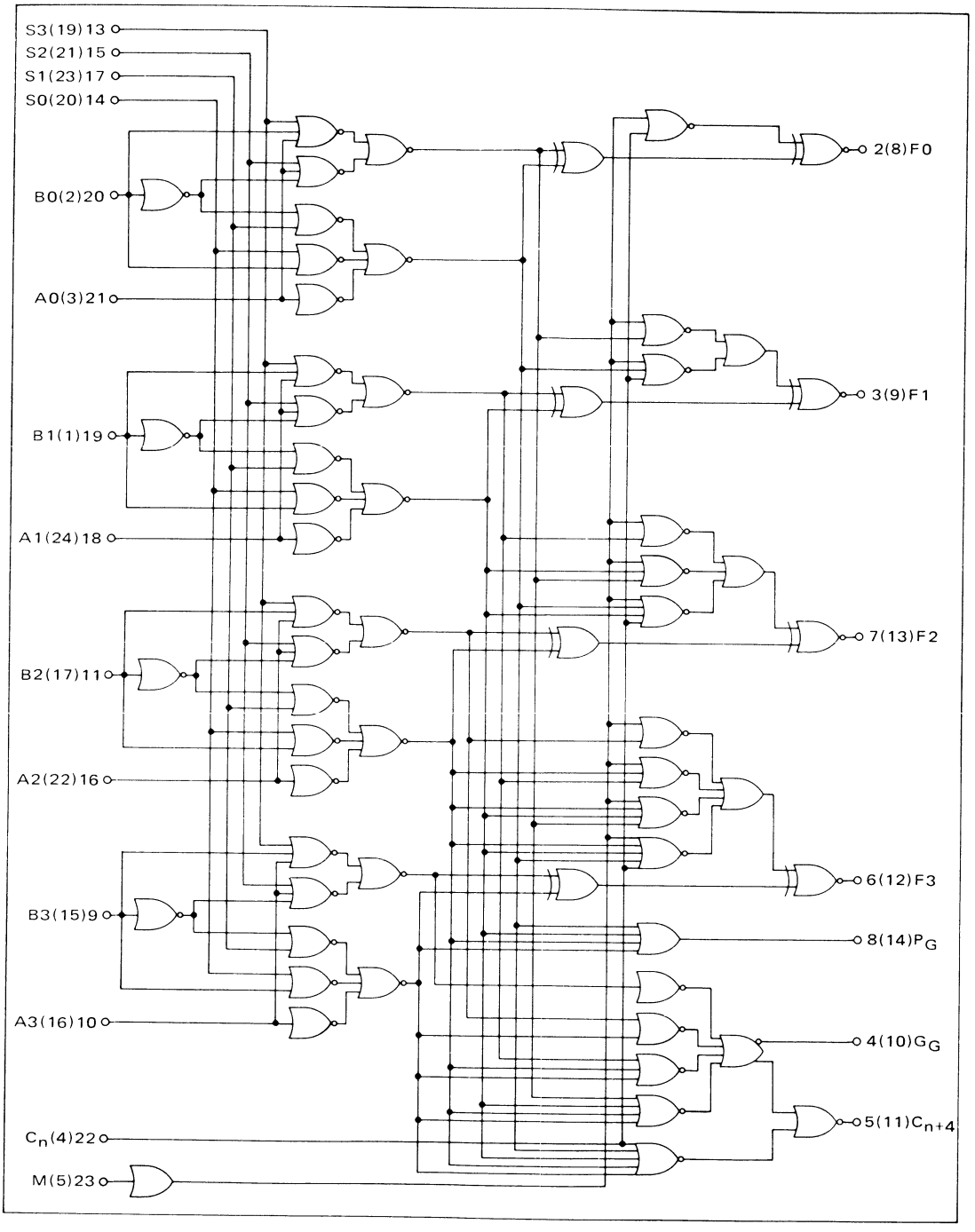
See following page for Switching Times.

-55°C and +125°C test values apply to MC105xx devices only.

SWITCHING TIMES

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Propagation Delay	t_{pd}											ns
C_n to C_{n+4}		1.0	5.1	1.0	5.1	1.1	5.0	1.1	5.4	0.9	5.1	
C_n to F		1.9	7.1	1.7	7.2	2.0	7.0	2.0	7.5	2.0	7.1	
A to F		2.9	10.1	2.6	10.4	3.0	10	3.0	10.8	2.8	10.2	
A to P_G		1.8	6.6	1.6	7.0	2.0	6.5	2.0	7.0	1.8	6.5	
A to G_G		1.9	7.1	1.1	7.4	2.0	7.0	1.3	7.7	2.0	7.1	
A to C_{n+4}		2.0	7.1	1.7	7.3	2.0	7.0	2.0	7.8	1.9	7.1	
B to F		2.9	11.1	2.7	11.3	3.0	11	3.0	11.9	2.7	11.2	
B to P_G		1.8	7.6	1.6	7.7	2.0	7.5	2.0	8.0	1.6	7.6	
B to G_G		1.9	8.1	1.7	8.2	2.0	8.0	2.0	8.6	2.0	8.1	
B to C_{n+4}		1.9	8.1	1.8	8.2	2.0	8.0	2.0	8.7	1.9	8.1	
M to F		2.8	10.3	2.4	10.3	3.0	10	3.0	10.8	2.8	10.2	
S to F		2.7	10.2	2.5	10.7	3.0	10	3.0	10.8	2.6	10.2	
S to P_G		1.9	8.1	1.7	8.3	2.0	8.0	2.0	8.4	1.8	8.1	
S to G_G		1.7	9.2	1.5	9.6	2.0	9.0	1.9	9.7	1.7	9.1	
S to C_{n+4}		1.9	9.1	1.6	9.3	2.0	9.0	2.0	9.9	1.8	9.1	
Rise Time, Fall Time (20% to 80%)	t_+, t_-											ns
C_n to C_{n+4}		0.9	3.1	1.0	3.2	1.0	3.0	1.0	3.2	0.8	3.1	
C_n to F		1.3	5.2	1.3	5.3	1.5	5.0	1.5	5.3	1.3	5.3	
A to F		1.3	5.2	1.3	5.4	1.5	5.0	1.5	5.3	1.3	5.2	
A to P_G		0.9	3.5	0.8	3.7	1.1	3.5	1.1	3.8	1.0	3.6	
A to G_G		1.3	5.2	1.2	5.1	1.5	5.0	1.2	5.3	1.3	5.2	
A to C_{n+4}		0.9	3.0	1.0	3.1	1.0	3.0	1.0	3.2	0.9	3.1	
B to F		1.3	5.2	1.2	5.3	1.5	5.0	1.5	5.3	1.3	5.2	
B to P_G		1.0	3.5	1.0	3.6	1.1	3.5	1.1	3.9	0.9	3.5	
B to G_G		1.3	5.0	1.4	5.2	1.5	5.0	1.2	5.4	1.3	5.0	
B to C_{n+4}		0.9	3.0	0.9	3.1	1.0	3.0	1.0	3.2	0.9	3.0	
M to F		1.3	5.2	1.1	5.1	1.5	5.0	1.5	5.3	1.3	5.2	
S to F		1.3	5.2	1.0	5.4	1.5	5.0	1.5	5.4	1.3	5.2	
S to P_G		1.0	5.1	0.8	5.1	1.1	5.0	1.1	5.2	1.0	5.1	
S to G_G		0.8	6.2	0.8	6.2	0.8	6.0	0.8	6.5	0.8	6.2	
S to C_{n+4}		1.0	5.1	0.9	5.3	1.1	5.0	1.0	5.2	1.0	5.1	

−55°C and +125°C test values apply to MC105xx devices only.



V_{CC1} = Pin 1(7)
V_{CC2} = Pin 24(6)
V_{EE} = Pin 12(18)

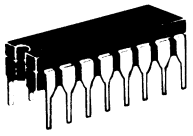
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

MC10182/MC10582

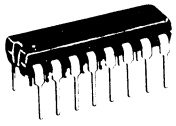
2-BIT ARITHMETIC LOGIC UNIT and FUNCTION GENERATOR

Function Select		POSITIVE LOGIC	
		Logic Function	Arithmetic Operation
		M is High	M is Low
S1	S0	F	F
L	L	F = A ⊙ B	F = A plus B plus Carry
L	H	F = A ⊕ B	F = $\bar{A}$ plus B plus Carry
H	L	F = A • B	F = A plus $\bar{B}$ plus Carry
H	H	F = A + B	F = A times 2

P_D = 575 mW typ/pkg (No Load)
t_{pd} = 7.5 ns typ (A or B to F or C_{n+2})
= 2.7 ns typ (C_n to C_{n+2} or F)
= 6.5 ns typ (A to P_G or G_G)



L SUFFIX
CERAMIC PACKAGE
CASE 620

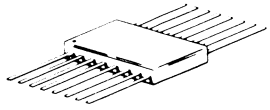


P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10182 only

The MC10182/MC10582 is a high-speed arithmetic logic unit capable of performing 4 logic operations and 4 arithmetic operations on two 2-bit words. Full internal carry is incorporated for arithmetic operation.

Arithmetic logic operations are selected by applying the appropriate binary word to the select inputs (S0 and S1) as indicated in the tables of arithmetic/logic functions. Group carry propagate (P_G) and carry generate (G_G) are provided for a second order look ahead carry using the MC10179. The internal carry is enabled by applying a low level voltage to the mode control input (M).

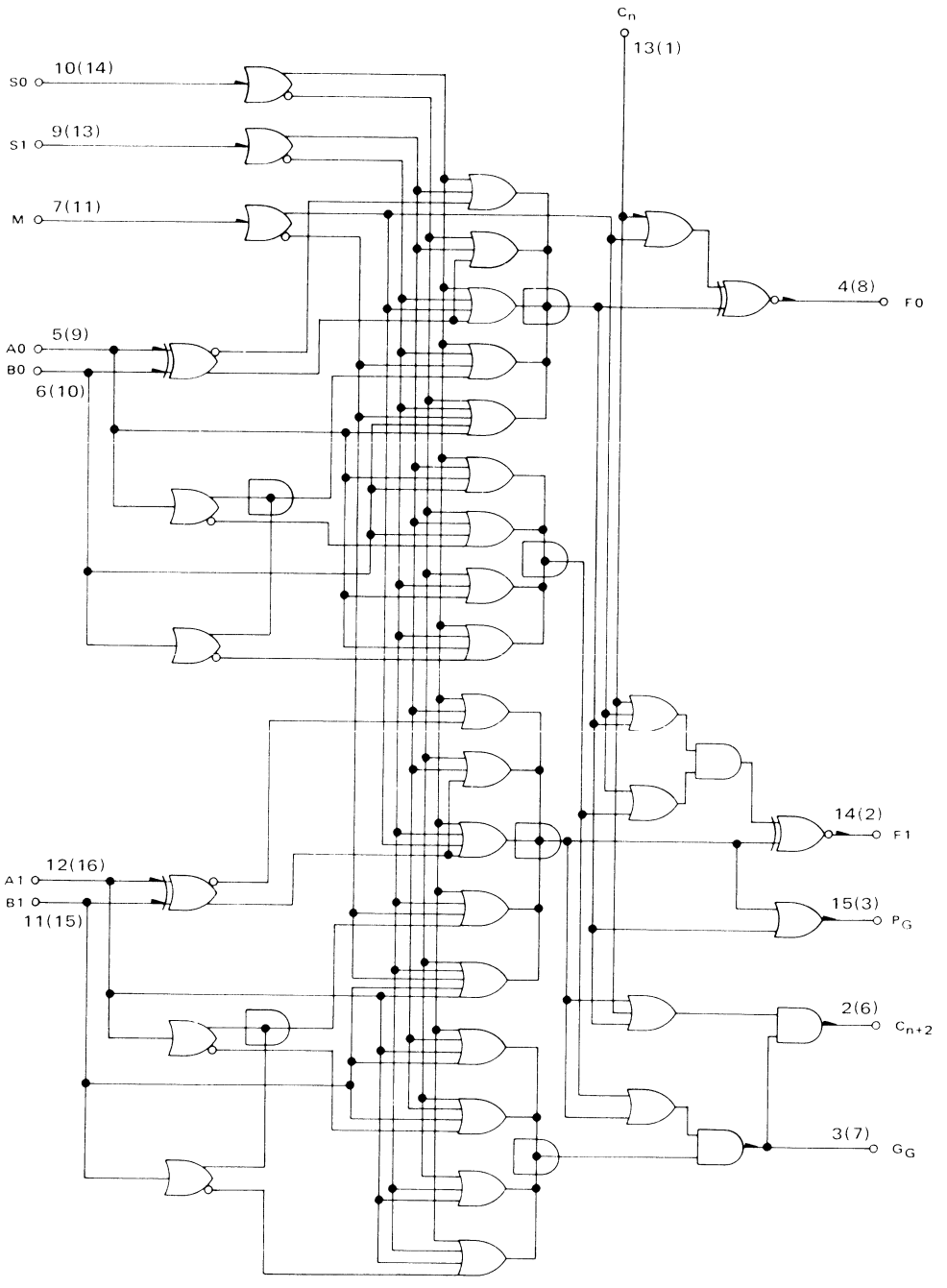
The MC10182 provides an alternate to the MC10181 four-bit ALU for applications not requiring the extended functions of the MC10181 or for applications requiring a 16 pin package. The MC10182 also differs from the MC10181 in that Word A and Word B are treated equally for addition and subtraction (A plus B, A minus B, B minus A).



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10582 only

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	152	–	152	–	138	–	152	–	152	mAdc
Input Current	I_{inH}											μAdc
Pins 7,9,10		–	375	–	350	–	220	–	220	–	220	
Pins 5,12		–	660	–	620	–	390	–	390	–	390	
Pins 6,11		–	495	–	460	–	290	–	290	–	290	
Pin 13		–	595	–	560	–	350	–	350	–	350	
Switching Times												ns
Propagation Delay	t_{pd}											
C_n to C_{n+2} or F		1.5	6.1	1.5	5.9	1.5	5.6	1.6	6.2	1.6	6.6	
M or S to F; A or B to P_G or G_G		2.3	10.8	2.3	10.5	2.3	10	2.4	11	2.4	11.7	
A0 or B0 to F; A1 or B1 to F1		2.3	10.8	2.3	10.5	2.3	10	2.4	11	2.4	11.7	
A0, B0, or A1 to C_{n+2}		2.3	10.8	2.3	10.5	2.3	10	2.4	11	2.4	11.7	
B1 to C_{n+2}		2.8	13	2.8	12.6	2.8	12	2.9	13.2	2.9	14	
Rise Time, Fall Time (20% to 80%)	t+,t−	1.5	4.9	1.5	4.7	1.5	4.5	1.6	5.0	1.6	5.3	ns

−55°C and +125°C test values apply to MC105xx devices only.



V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

TRUTH TABLE

Input					M	L			L			L			H			H			H		
					S1	L			L			H			L			L			H		
					S0	L			H			L			H			L			H		
A1	B1	A0	B0	C_n	F1	F0	P_G	G_G	C_{n+2}	F1	F0	P_G	G_G	C_{n+2}	F1	F0	P_G	G_G	C_{n+2}	F1	F0	P_G	G_G	C_{n+2}
L	L	L	L	L	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
L	L	L	L	H	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
L	L	L	H	L	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
L	L	L	H	H	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
L	L	H	L	L	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
L	L	H	L	H	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
L	L	H	H	L	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
L	L	H	H	H	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
L	H	L	L	L	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
L	H	L	L	H	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
L	H	L	H	L	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
L	H	L	H	H	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
L	H	H	L	L	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
L	H	H	L	H	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
L	H	H	H	L	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
L	H	H	H	H	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
H	L	L	L	L	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
H	L	L	L	H	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
H	L	L	H	L	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
H	L	L	H	H	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
H	L	H	L	L	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
H	L	H	L	H	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
H	L	H	H	L	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
H	L	H	H	H	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
H	H	L	L	L	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
H	H	L	L	H	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
H	H	L	H	L	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
H	H	L	H	H	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
H	H	H	L	L	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
H	H	H	L	H	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
H	H	H	H	L	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L
H	H	H	H	H	L	L	L	H	L	L	L	L	H	L	H	H	L	H	L	L	L	L	H	L

These outputs are not normally used during logic operation.

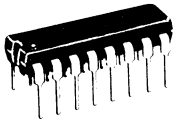
MC10183

4 X 2 MULTIPLIER

TRUTH TABLE

Y 1	Y0	Y1	P	A	B	C	Operation	Complementor
L	L	L	H	L	L	L	Add Zero	Direct
H	L	L	H	H	L	L	Add 1X	Direct
L	H	L	H	H	L	L	Add 1X	Direct
H	H	L	H	L	H	L	Add 2X	Direct
L	L	H	H	L	H	H	Sub 2X	Invert
H	L	H	H	H	L	H	Sub 1X	Invert
L	H	H	H	H	L	H	Sub 1X	Invert
H	H	H	H	L	L	H	Sub Zero	Invert
L	L	L	L	L	L	L	Sub Zero	Direct
H	L	L	L	H	L	H	Sub 1X	Invert
L	H	L	L	H	L	H	Sub 1X	Invert
H	H	L	L	L	H	H	Sub 2X	Invert
L	L	H	L	L	H	L	Add 2X	Direct
H	L	H	L	H	L	L	Add 1X	Direct
L	H	H	L	H	L	L	Add 1X	Direct
H	H	H	L	L	L	H	Add Zero	Invert

X-1, X0, X1, X2, X3	Multiplicand Inputs
Y-1, Y0, Y1	Multiplier Inputs
K0, K1, K2, K3	Constant Inputs
$\overline{C}_n$	Carry Input
$\overline{P}$	Polarity Control
M	Mode Control
S0, S1, S2, S3, S4, S5	Product Output
$\overline{C}_{n+4}$	Carry Output



L SUFFIX
CERAMIC PACKAGE
CASE 623

The MC10183 is a 4 X 2 bit multiplier that can multiply 2's complement numbers producing a 2's complement product without correction. The device can be used as a 4 X 2 bit multiplier cell to build larger iterative arrays.

The part performs the function defined as F = XY + K, where K is an input field used to add partial products in an array or to add a constant to the least significant part of the array product. The algorithm used is a modified Booth's algorithm or multiplier coding technique. The device consists of a shift network and an adder/subtracter in which 0, 1 times X, or 2 times X is either added or subtracted to input constant K. The Y inputs control multiplication as shown in the Truth Table.

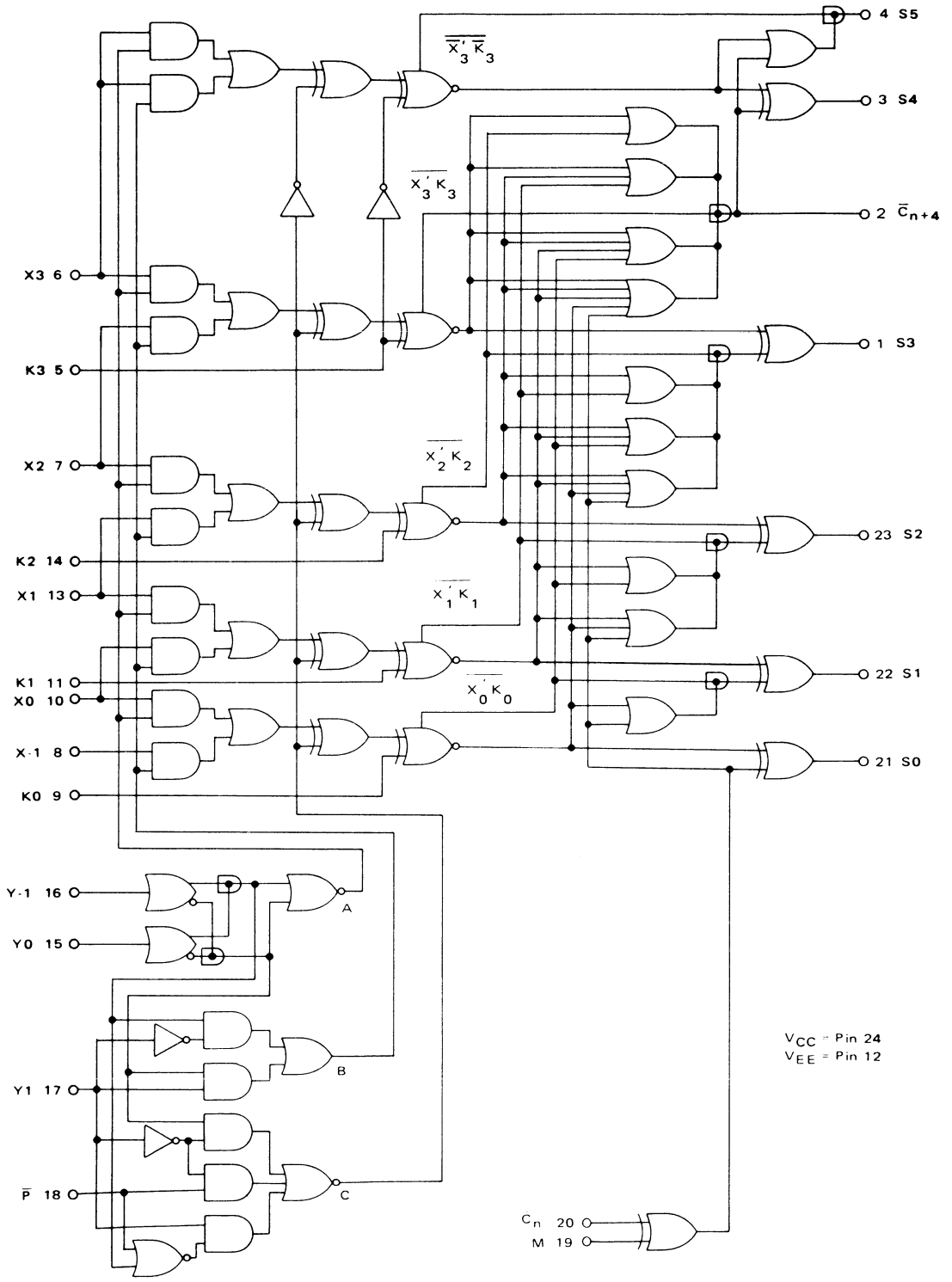
The most significant digit in a word carries a negative weight allowing 2's complement numbers of various lengths to be multiplied. An M-bit by N-bit multiplication produces an M + N bit product.

The $\overline{P}$ polarity input allows multiplication in either positive logic ($\overline{P}$ = high) or negative logic ($\overline{P}$ =low) representation. Also, mode control M inverts $\overline{C}_n$ when high and passes $\overline{C}_n$ directly when left low.

P_D = 760 mW typ/pkg (No Load)
t_{pd} = 50 ns typ (8 X 8 bit product)
t+, t- = 3.5 ns typ (20% - 80%)

Characteristic	Symbol	-30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit
Power Supply Drain Current	I_E	–	201	–	183	–	201	mAdc
Input Current	I_{inH}							μAdc
Pins 8,9,11,14,15,16,20		–	350	–	220	–	220	
Pins 17,18,19		–	320	–	200	–	220	
Pins 5,6,7,10,13		–	390	–	245	–	245	
Switching Times								ns
Propagation Delay	t_{pd}							
$\overline{C}_n$ to $\overline{C}_{n+4}$		1.0	5.3	1.0	5.0	1.0	5.5	
$\overline{C}_n$ to S; X to $\overline{C}_{n+4}$		1.8	8.4	1.8	8.0	1.8	8.8	
K or X to S; $\overline{C}_n$ to S4,S5		2.5	11	2.5	10.5	2.5	11.5	
K to $\overline{C}_{n+4}$		1.6	7.3	1.6	7.0	1.6	7.7	
Y to S or $\overline{C}_{n+4}$		3.2	14.1	3.2	13.5	3.2	14.8	
Rise Time, Fall Time (20% to 80%)	t+,t-	1.0	6.3	1.0	6.0	1.0	6.6	ns

POSITIVE LOGIC DIAGRAM



MC10183 APPLICATIONS INFORMATION

The MC10183 is a 4 X 2 bit multiplier that uses a modified Booth's algorithm or multiplier coding technique. The device generates the function: $S = X \cdot Y + K$

where

X = 4 bit multiplicand
Y = 2-bit multiplier
K = 4-bit constant

The addition of the constant allows the device to be used in an iterative array of parts for larger words. The algorithm for multiplication is:

Y_{i-1}	Y_i	Y_{i+1}	Operation
0	0	0	add zero
1	0	0	add multiplicand
0	1	0	add multiplicand
1	1	0	add 2 times multiplicand
0	0	1	sub 2 times multiplicand
1	0	1	sub multiplicand
0	1	1	sub multiplicand
1	1	1	sub zero

DEVICE OPERATION

The device consists of three main sections; a decoder, a shifter, and a high speed look-ahead carry adder/subtractor.

1. The decoder uses the Y inputs to generate the control signals for the shifter and the adder/subtractor. Also, the polarity control $\overline{P}$ is used to allow operation in either positive or negative logic. Referring to the logic diagram, the control signals are:

$A = Y_{-1} \oplus Y_0$ (1 times multiplicand)

$B = Y_{-1}Y_0\overline{Y}_1 + \overline{Y}_{-1}\overline{Y}_0Y_1$ (2 times multiplicand)

$\overline{C} = \overline{PY}_1 + \overline{Y}_{-1}\overline{Y}_0\overline{Y}_1 + PY_1(\overline{Y}_{-1} + \overline{Y}_0)$ (add/subtract)

The $\overline{P}$ input is tied to a high logic level or ground for positive logic operation.

2. The shift network is a multiplexer that ripples through number X (1 times multiplicand), shifts number X by one bit (2 times multiplicand), or sets the output to zero. The network is controlled by decoder functions A and B which are generated in accordance with the multiply algorithm.

3. The adder/subtractor follows the shift network which performs the actual multiplication. The adder/subtractor produces the sum or difference of the newly formed partial product and the accumulated partial product (constant K). Subtraction is accomplished by inverting the shifted product and doing a two's complement addition. The carry in of the least significant bit must be a logic one during subtraction.

The two most significant bits of the product are used for sign detection and overflow for a two's complement multiply. These outputs are used only as the two most significant bits of the accumulated product at each addition level within a multiplier array.

Overflow can occur either as the result of 2 times the multiplicand, and/or of an addition or subtraction. To show all possible conditions (including overflow), the most significant bit (S5) must carry a negative binary weight. To show this for a 4 X 2 bit multiply plus constant, consider the following addition:

$X'_4 \cdot X'_3\ X'_2\ X'_1\ X'_0$	shifter outputs
+ K3 · K3 K2 K1 K0	constant
S5 S4 · S3 S2 S1 S0	sum

The shift network produces 5 product bits (maximum value of 2 times multiplicand) and a 4-bit constant is added to the least signficant end of the product. The K3 bit is repeated to hold the proper binary weight. Because S5 has a negative weight all possible combinations are represented properly.

If no overflow occurs S4 = S5, and S4 can be used as a sign bit. Under overflow conditions S4 ≠ S5, and overflow can be detected by EXCLUSIVE-ORing S4 and S5.

USAGE RULES

The MC10183 can be used in larger arrays to produce a two's complement product of 2 two's complement numbers. The following rules apply:

1. For an M-bit by N-bit multiplier, an (M+N)-bit product is formed. The number of MC10183's equals (M * N)/8. As an example, an 8 X 8 bit (Figure 1) array requires (8X8)/8 = 8 packages.

2. The MC10183 can be used directly for both positive logic and negative logic representations. The $\overline{P}$ input can be tied to ground or to a high logic level for positive logic operation, or left at a low logic level for negative logic operation.

3. The M mode control input is used to invert $\overline{C}_n$ when placed at a high logic level or ground, or passes $\overline{C}_n$ directly when left as a low logic level. When $\overline{C}_n$ is driven from $\overline{C}_{n+4}$ of a preceding device, M control is left in a low logic state. When $\overline{C}_n$ is the least significant input carry bit for a level of addition within an array, $\overline{C}_n$ is tied to Y_1 of the same device, and the M input is placed at a high logic level. Y_1 controls when subtraction occurs, and carry in must be equal to a logic one during subtraction.

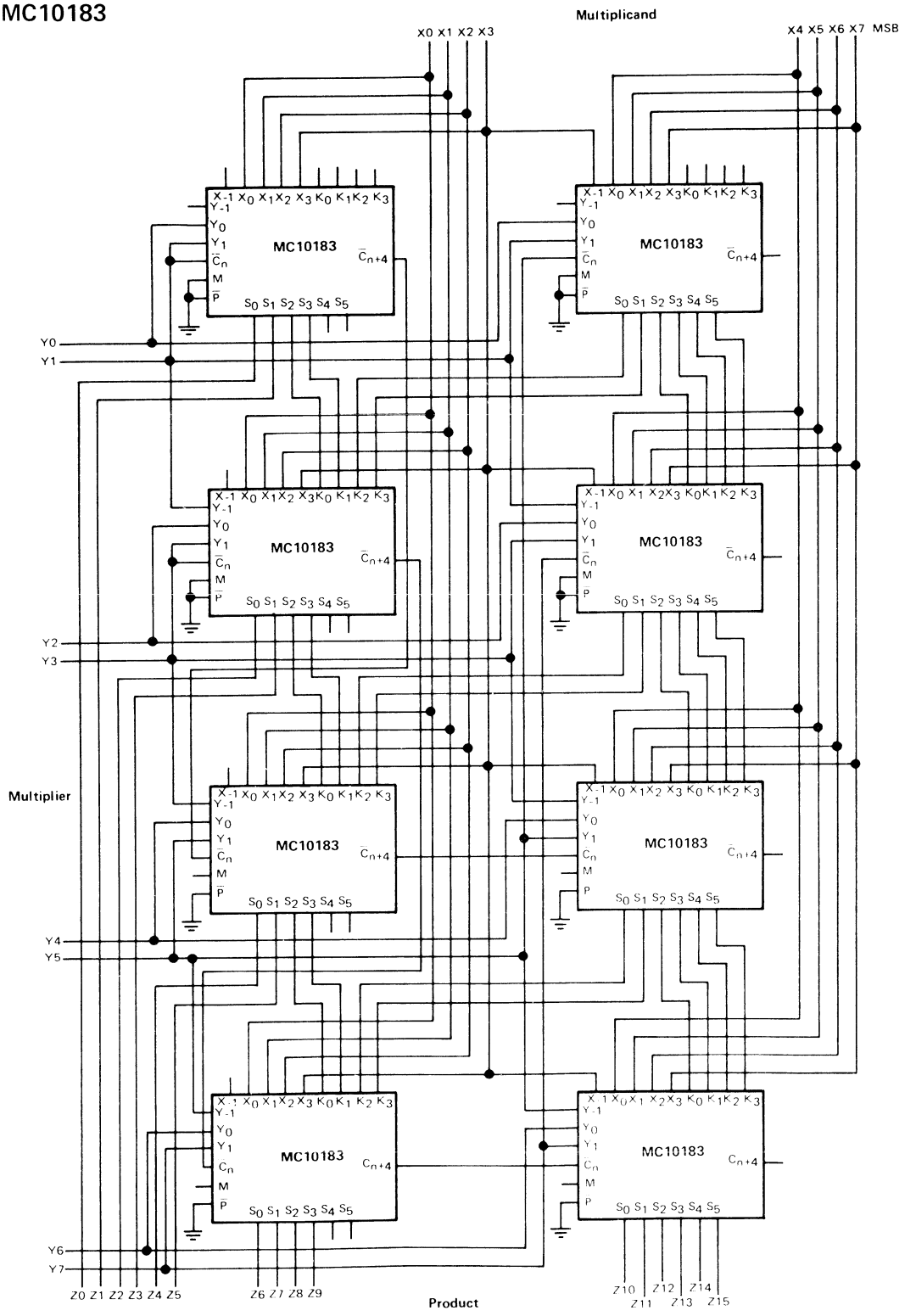


FIGURE 1 – 8-BIT × 8-BIT 2's COMPLEMENT MULTIPLIER

8 × 4 BIT EXAMPLE

Figure 2 shows 4 MC10183's in an 8 × 4 bit array. A 12-bit two's complement product is produced from a 4-bit multiplier and an 8-bit multiplicand. The array is used for positive logic representation, and all $\overline{P}$ inputs are tied to ground. At the first level of multiplication, the X_{-1} and Y_{-1} inputs are left open (logic "0") because the initial condition is treated as an add operation. The K inputs are used to add the accumulated partial product at each level of the array. If the initial partial product is zero, the least significant K inputs are left at a zero logic state (CONSTANT inputs in the figure). However, these inputs can also be used to add a constant to the least significant end of the product.

When the MC10183 is expanded to longer numbers, the carry out ($\overline{C}_{n+4}$) of a device must be rippled to the carry in ($\overline{C}_n$) of the next most significant device at the same level of multiplication. The least significant device must have the carry input equal to zero for an add and equal to one for a subtraction. In observing the multiplication algorithm y_{i+1} is always equal to 1 for a subtraction, and the carry input can be tied to Y_1. However, the M mode input must be tied to ground for this device to invert the carry input ($\overline{C}_n$) because the input requires a complemented signal.

The S4 and S5 outputs are used only at the most significant part of the array. These two sum outputs only have meaning as the two most significant bits of a two's complement number.

OTHER ARRAYS

The normal parallelogram structure consists of several stages, each multiplying two bits of multiplier times the multiplicand and adds the partial product. In larger arrays, faster configurations can be made by moving some multiplier blocks while maintaining the relative weight of each partial product. The typical times possible for various N-bit X N-bit arrays are:

Number of Bits	Total Multiply Time (ns)	Package Count
8	43	8
12	67	18
16	90	32

The times do not include wiring delays.

Because of the versatility of the MC10183, many other types of arrays can also be built. Faster arrays using additional adders, pipeline techniques, one's complement and magnitude multipliers, and truncated product multipliers can all be built.

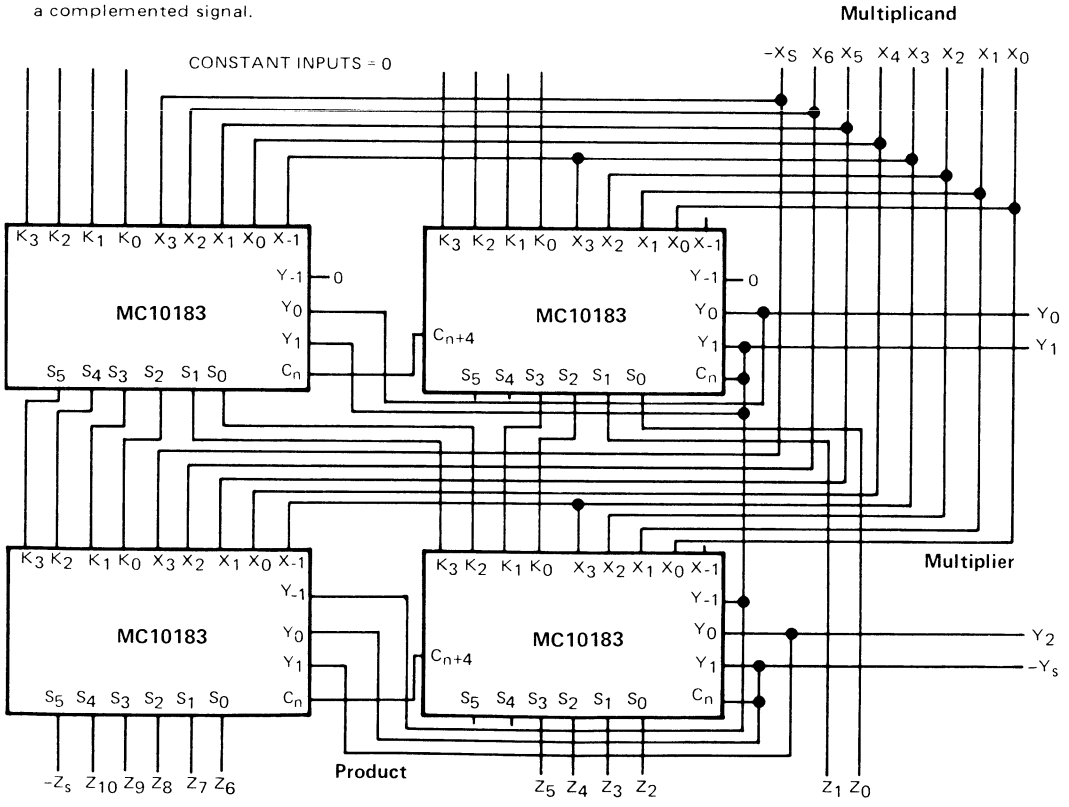
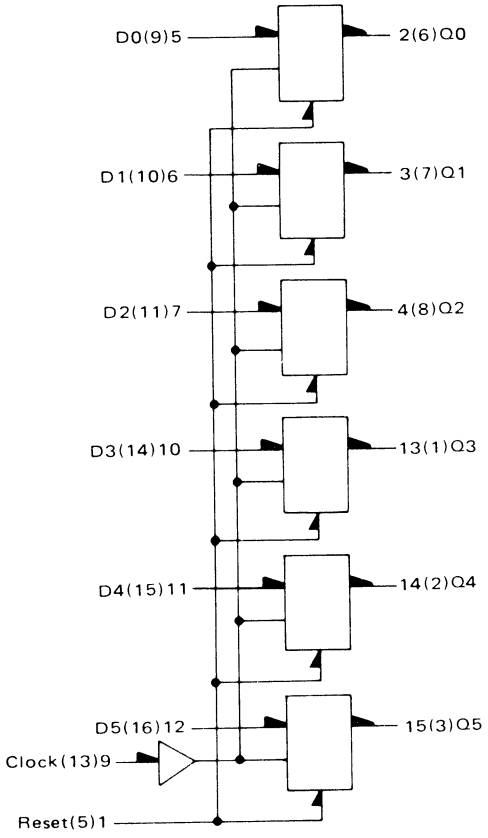


FIGURE 2 – 8-BIT BY 4-BIT 2's COMPLEMENT MULTIPLIER

MC10186/MC10586

HEX D MASTER-SLAVE FLIP-FLOP WITH RESET



The MC10186/MC10586 contains six high-speed, master slave type "D" flip-flops. Clocking is common to all six flip-flops. Data is entered into the master when the clock is low. Master to slave data transfer takes place on the positive-going Clock transition. Thus, outputs may change only on a positive-going Clock transition. A change in the information present at the data (D) input will not affect the output information any other time due to the master-slave construction of this device. A common Reset is included in this circuit. Reset only functions when clock is low.

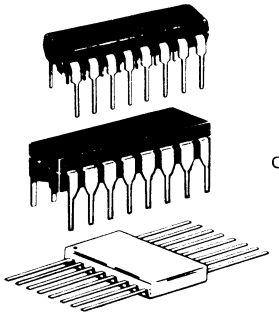
CLOCKED TRUTH TABLE

R	C	Q	Qn+1
L	L	ϕ	Qn
L	H *	L	L
L	H *	H	H
H	L	ϕ	L

ϕ Don't Care

*A clock H is a clock transition from a low to a high state.

V_{CC} = Pin 16 (4)
V_{EE} = Pin 8 (12)
P_D = 460 mW typ/pkg (No Load)
t_{pd} = 3.5 ns typ
f_{Tog} = 150 MHz typ



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10186 only

L SUFFIX
CERAMIC PACKAGE
CASE 620

F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10586 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

ELECTRICAL CHARACTERISTICS

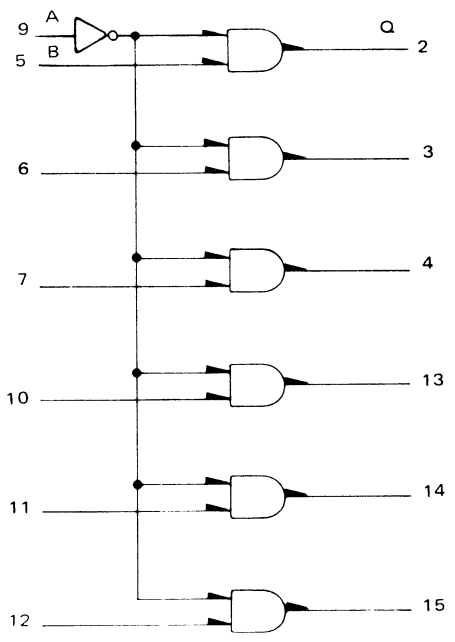
Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	121	—	121	—	110	—	121	—	121	mAdc
Input Current	I_{inH}											μAdc
Pins 5, 6, 7, 10, 11, 12		—	375	—	350	—	220	—	220	—	220	
Pin 9		—	525	—	495	—	310	—	310	—	310	
Pin 1		—	975	—	920	—	575	—	575	—	575	
Switching Times												ns
Propagation Delay	t_{pd}	1.6	4.9	1.6	4.6	1.6	4.5	1.6	5.0	1.6	5.3	
Rise Time, Fall Time (20% to 80%)	t_+, t_-	1.0	4.3	1.0	4.1	1.1	4.0	1.1	4.4	1.0	4.7	ns
Setup Time	t_{set}	2.5	—	2.5	—	2.5	—	2.5	—	2.5	—	ns
Hold Time	t_{hold}	1.5	—	1.5	—	1.5	—	1.5	—	1.5	—	ns
Toggle Frequency	f_{Tog}	125	—	125	—	125	—	125	—	125	—	MHz

−55°C and +125°C test values apply to MC105xx devices only.

MC10188

HEX BUFFER WITH ENABLE

ADVANCE INFORMATION



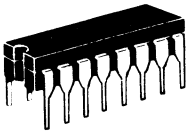
The MC10188 provides a high speed Hex Buffer with a common Enable input. When Enable is in the high state, all outputs are in the low state. When Enable is in the low state, the outputs take the same state as the inputs.

TRUTH TABLE

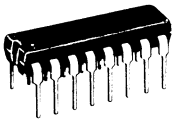
Inputs		Output
A	B	Q
L	L	L
L	H	H
H	L	L
H	H	L

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

P_D = 180 mW typ/pkg (No Load)
t_{pd} = 2.0 ns typ (B – Q)
= 2.5 ns typ (A – Q)



L SUFFIX
CERAMIC PACKAGE
CASE 620



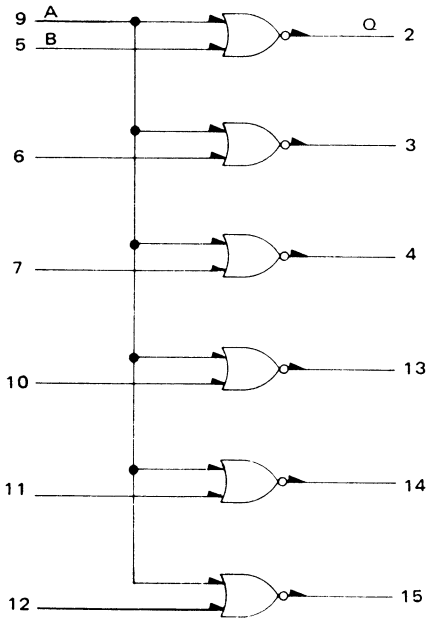
P SUFFIX
PLASTIC PACKAGE
CASE 648

Characteristic	Symbol	-30°C		+25°C			+85°C		Unit
		Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	–	46	–	34	42	–	46	mAdc
Input Current	I_{inH}								μAdc
Pins 5, 6, 7, 10, 11, 12		–	425	–	–	265	–	265	
Pin 9		–	460	–	–	290	–	290	
Switching Times									ns
Propagation Delay	t_{pd}								
Data (B)		–	–	–	2.0	–	–	–	
Enable (A)		–	–	–	2.5	–	–	–	
Rise Time, Fall Time (20% to 80%)	t^+, t^-	–	–	–	2.0	–	–	–	ns

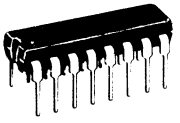
This is advance information and specifications are subject to change without notice.

MC10189

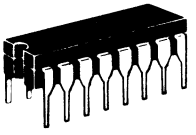
HEX INVERTER WITH ENABLE



The MC10189 provides a high-speed Hex Inverter with a common Enable input. The hex inverting function is provided when Enable is in the low state. When Enable is in the high state all outputs are low. Each input is connected to V_{EE} through a 50 kΩ resistor which eliminates the need to tie unused inputs low. Typical propagation times from inputs to outputs are 2.0 ns and from Enable to outputs are 2.5 ns.



P SUFFIX
PLASTIC PACKAGE
CASE 648



L SUFFIX
CERAMIC PACKAGE
CASE 620

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

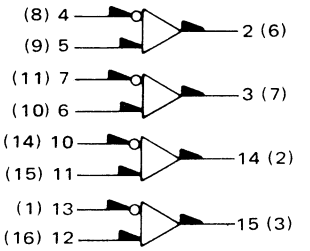
TRUTH TABLE		
Inputs		Output
A	B	Q
L	L	H
L	H	L
H	L	L
H	H	L

P_D = 200 mW typ/pkg (No Load)
t_{pd} = 2.0 ns typ (B – Q)
= 2.5 ns typ (A – Q)

Characteristic	Symbol	-30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit
Power Supply Drain Current	I_E	–	44	–	40	–	44	mAdc
Input Current	I_{inH}							
Pins 5, 6, 7, 10, 11, 12		–	425	–	265	–	265	
Pin 9		–	890	–	555	–	555	
Switching Times								ns
Propagation Delay	t_{pd}							
Data (B)		1.0	3.3	1.0	2.9	1.0	3.3	
Enable (A)		1.1	3.9	1.1	3.5	1.1	3.9	
Rise Time, Fall Time (20% to 80%)	t^+, t^-	1.1	3.7	1.1	3.3	1.1	3.7	ns

MC10190/MC10590

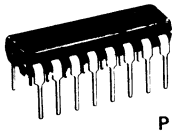
QUAD MST-TO-MECL10,000 TRANSLATOR



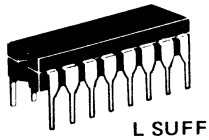
V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)
V_{SS} = Pin 9 (13) Translator
V_{CC} = Pin 9 (13) Receiver

P_D = 215 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ
$t+, t-$ = 2.0 ns typ (20% to 80%)

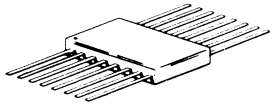
The MC10190/MC10590 is a quad translator for interfacing from IBM MST-type logic signals to standard MECL 10,000 logic levels. This circuit features differential inputs for high noise environments or may be used with single ended lines by tieing one of the inputs to ground (translator), or $V_{BB} \cong 1.29$ V (receiver). Since the device is designed to accept signals centered around ground, it is a useful interface element for many communication systems. When pin 9 is connected to V_{CC} (Gnd) the circuit becomes a line receiver for MECL signals. The outputs go to a low level whenever the inputs are left floating.



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10190 only



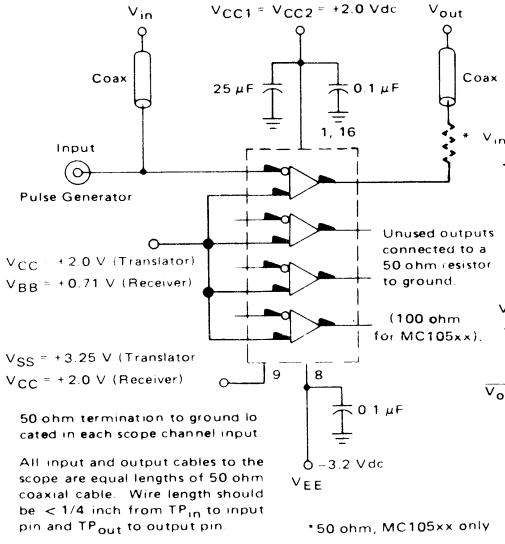
L SUFFIX
CERAMIC PACKAGE
CASE 620

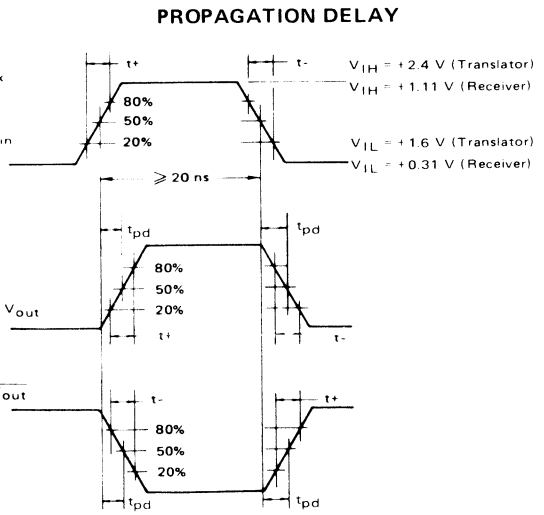


F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10590 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C





NOTE: All power supply and logic levels are shown shifted 2 volts positive.

ELECTRICAL CHARACTERISTICS

@ Test Temperature	TEST VOLTAGE VALUES (Volts)											
	V_{IH}max	V_{IL}min	V_{IHA}min	V_{ILA}max	V_{IHM}*	V_{ILM}*	V_{IHH}*	V_{ILH}*	V_{IHL}*	V_{ILL}*	V_{SS}*	V_{EE}
MC10190												
−30°C	−0.890	−1.890	−1.205	−1.500	+0.374	−0.523	+0.186	−0.850	−1.486	−2.53	+1.25	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	+0.440	−0.490	+0.186	−0.850	−1.486	−2.53	+1.25	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	+0.548	−0.454	+0.186	−0.850	−1.486	−2.53	+1.25	−5.2
MC10590												
−55°C	−0.880	−1.920	−1.255	−1.510	+0.344	−0.538	+0.186	−0.850	−1.486	−2.53	+1.25	−5.2
+25°C	−0.780	−1.850	−1.105	−1.475	+0.440	−0.490	+0.186	−0.850	−1.486	−2.53	+1.25	−5.2
+125°C	−0.630	−1.820	−1.000	−1.400	+0.620	−0.430	+0.186	−0.850	−1.486	−2.53	+1.25	−52.

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Power Supply Drain Current	I_E	–	57	–	57	–	52	–	57	–	57	mAdc	V_{in} = V_{IH} max (Pins 4, 6, 10, 12), V_{IL} min (Pins 5, 7, 11, 13).
	I_{CC}	–	27	–	27	–	27	–	27	–	27	mAdc	
Input Current	I_{inH}	–	80	–	70	–	45	–	45	–	45	μAdc	V_{in} = V_{IH} max to P.U.T., V_{IL} min to the other input of that gate. Test one input at a time.
Reverse Leakage Current	I_{CBO}	–	1.5	–	1.5	–	1.0	–	1.0	–	1.0	μAdc	V_{in} = V_{EE} to P.U.T., one input at a time.
Output Logic Levels (Translator) Common Mode Rejection Test (Receiver) MC10190 MC10590	V_{OH}	–	–	−1.060	−0.890	−0.960	−0.810	−0.890	−0.700	–	–	Vdc	Translator (Pin 9 = V_{SS} = +1.25 Vdc): V_{in} = V_{ILM} to one input of the gate under test and V_{IHM} to the other input of that gate. Receiver (Pin 9 = V_{CC} = Ground): V_{in} = V_{IHH} or V_{IHL} to one input of each gate under test and V_{ILH} or V_{ILL}, respectively, to the other input of that gate.
		−1.080	−0.880	–	–	−0.930	−0.780	–	–	−0.825	−0.630		
MC10190 MC10590	V_{OL}	–	–	−1.890	−1.675	−1.850	−1.650	−1.825	−1.615	–	–	Vdc	
		−1.920	−1.655	–	–	−1.850	−1.620	–	–	−1.820	−1.545		
Switching Times Propagation Delay	t_{pd}	1.0	4.0	1.0	3.9	1.0	3.7	1.0	4.1	1.0	4.3	ns	See switching times test circuit and waveforms.
Rise Time, Fall Time	t+, t−	1.1	4.6	1.1	4.5	1.5	4.3	1.1	4.7	1.1	5.0	ns	20% to 80%

*V_{SS} = IBM Supply Voltage. Unless otherwise specified, Pin 9 = V_{SS} = +1.25 Vdc.

V_{IHM} = Input logic "1" for IBM levels.

V_{ILM} = Input logic "0" for IBM levels.

V_{IHH} = Input logic "1" level shifted positive for common mode rejection tests.

V_{ILH} = Input logic "0" level shifted positive for common mode rejection tests.

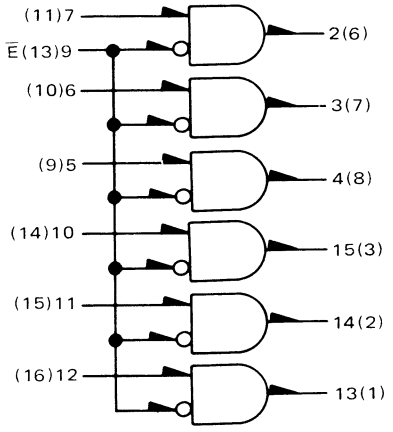
V_{IHL} = Input logic "1" level shifted negative for common mode rejection tests.

V_{ILL} = Input logic "0" level shifted negative for common mode rejection tests.

−55°C and +125°C test values apply to MC105xx devices only.

MC10191/MC10591

HEX MECL 10,000 TO MST TRANSLATOR



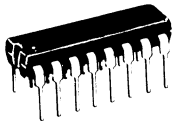
The MC10191/MC10591 is a hex MECL 10,000 to IBM MST type logic translator. A common enable (active low) is provided for gating. Open emitter outputs are provided to permit direct transmission line driving.

The MC10191/MC10591 is useful for interfacing to both MST-II and MST-IV systems.

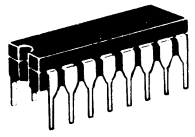
Data	Enable	Output
L	L	L
L	H	L
H	L	H
H	H	L

V_{CC1} = Pin 1(5) = +1.25 Vdc
V_{CC2} = Pin 16(4) = Gnd
V_{EE} = Pin 8(12) = −5.2 Vdc

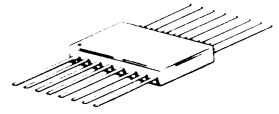
P_D = 145 mW typ/pkg (No Load)
t_{pd} = 2.2 ns typ (Data to Output)
· = 3.3 ns typ (Enable to Output)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10191 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



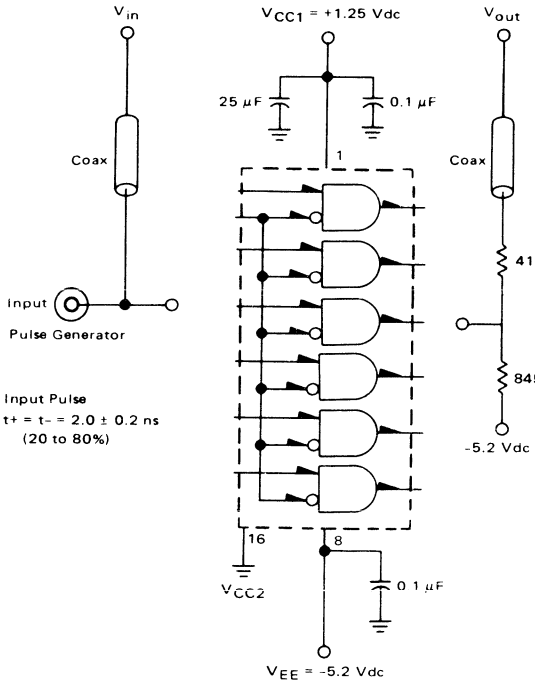
F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10591 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E		39		39	–	35	–	39	–	39	mAdc
	I_{CC}		23		23	–	23	–	23	–	23	mAdc
Input Current	I_{inH}											µAdc
Pins 5,6,7,10,11,12		–	415	–	390		245	–	245	–	245	
Pin 9			450		425		265		265		265	
	I_{inL}	0.5		0.5		0.5	–	0.3	–	0.3	–	µAdc
Logic "1" Output Voltage	V_{OH}	+0.111	+0.344	+0.156	+0.374	+0.255	+0.440	+0.327	+0.548	+0.375	+0.620	Vdc
Logic "0" Output Voltage	V_{OL}	−0.538	−0.333	−0.523	−0.323	−0.490	−0.290	−0.454	−0.254	−0.430	−0.230	Vdc
Logic "1" Threshold Voltage	V_{OHA}	+0.091	–	+0.136	–	+0.235	–	+0.307	–	+0.355	–	Vdc
Logic "0" Threshold Voltage	V_{OLA}		−0.318	–	−0.303	–	−0.270	–	−0.234	–	−0.210	Vdc
Switching Times												ns
Propagation Delay	t_{pd}											
Data		1.0	3.7	1.0	3.6	1.0	3.4	1.0	3.7	1.0	4.0	
Enable		1.0	4.9	1.0	4.7	1.0	4.5	1.0	5.0	1.0	5.3	
Rise Time, Fall Time (20% to 80%)	t_+, t_-	1.1	4.6	1.1	4.5	1.1	4.3	1.1	4.7	1.1	5.0	ns

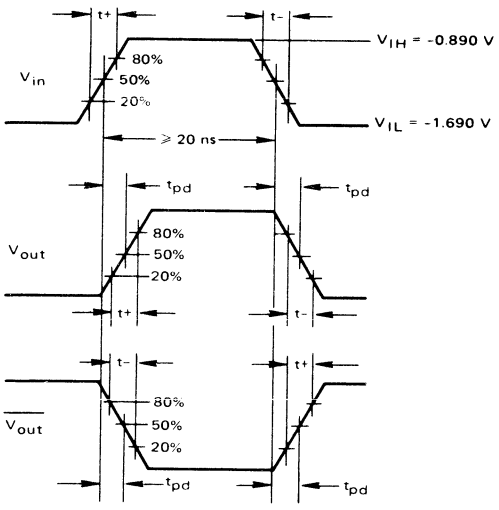
−55°C and +125°C test values apply to MC105xx devices only.

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

PROPAGATION DELAY

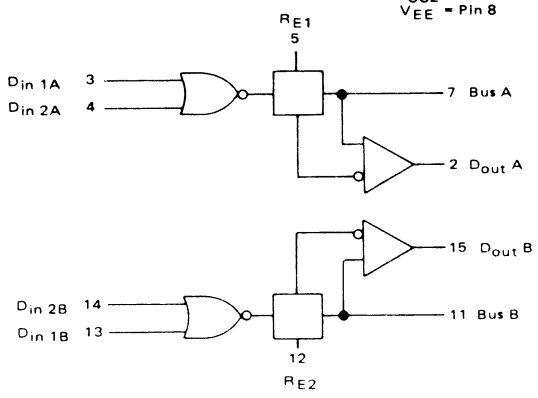


MC10194/MC10594

DUAL SIMULTANEOUS BUS TRANSCEIVER

P_D = 405 mW typ/pkg (No Load)
t_{pd} = 2.5 ns typ

V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8



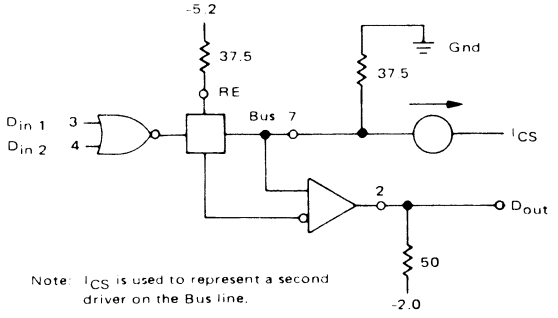
The MC10194/MC10594 is a dual line driver/receiver which is capable of transmitting and receiving full duplex digital signals on a high speed bus line. Because of the current source line driver, two independent messages may be transmitted on one line at the same time.

The MC10194/MC10594 is designed to work with a wide range of line impedances by connecting a resistor equal to one half the line impedance between the R_{E1} and R_{E2} inputs and V_{EE}. Each driver in the circuit will drive lines down to 75 ohms or the two drivers may be operated in parallel for lines down to 37 ohms. The data inputs and data outputs are standard MECL 10,000 logic levels.

TRUTH TABLE

Inputs		Outputs	
D_{in} 1	D_{in} 2	Bus	D_{out}
L	L	V_{BusO}	H
H	L	V_{BusH}	H
L	H	V_{BusH}	H
H	H	V_{BusH}	H
L	L	V_{BusH}	L
H	L	V_{BusL}	L
L	H	V_{BusL}	L
H	H	V_{BusL}	L

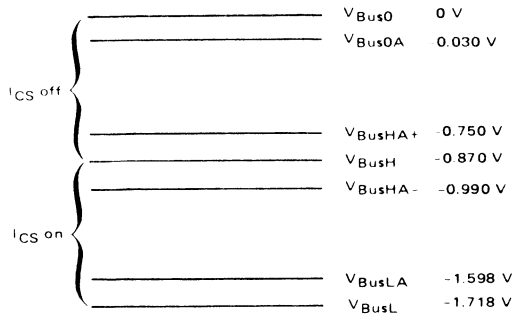
DC TEST CONFIGURATION

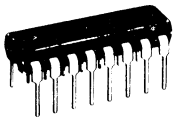


Note: I_{CS} is used to represent a second driver on the Bus line.

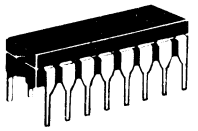
DC LOGIC LEVEL DESCRIPTION

The bus terminal (pin 7 or 11) can be at any one of three possible levels V_{BusO}, V_{BusH}, or V_{BusL} depending upon the combination of inputs applied. The MECL inputs (pins 3 and 4 or 13 and 14) cause the bus terminal to switch between two levels, V_{BusO} and V_{BusH} when the external current source (I_{CS}) is off, and V_{BusH} and V_{BusL} when the external current source is on. The bus output threshold voltage levels caused by applying an input threshold voltage V_{ILA} or V_{IHA} at a data input are also translated depending upon the state of I_{CS}. These threshold levels are V_{BusOA} and V_{BusHA+} respectively when I_{CS} is off, and V_{BusHA-} and V_{BusLA} respectively when I_{CS} is on. These relative voltage levels are shown in the figure on the right.

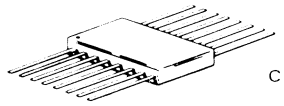




P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10194 Only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10594 Only

TEST VOLTAGE/CURRENT VALUES

	@ Test Temperature	(mAdc) I_{CS1}	(mAdc) I_{CS0A}	(mAdc) I_{CS1A}	(Volts) V_{CL}	(Volts) V_{CH}
MC10194	-30°C	-21.1	6.35	14.50	-1.508	0
	+25°C	-22.6	6.80	15.27	-1.618	0
	+85°C	-24.2	7.27	16.35	-1.738	0
MC10594	-55	-21.1	6.35	14.50	-1.458	0
	±25	-22.6	6.80	15.27	-1.618	0
	+125	-24.2	7.27	16.35	-1.818	0

ELECTRICAL CHARACTERISTICS

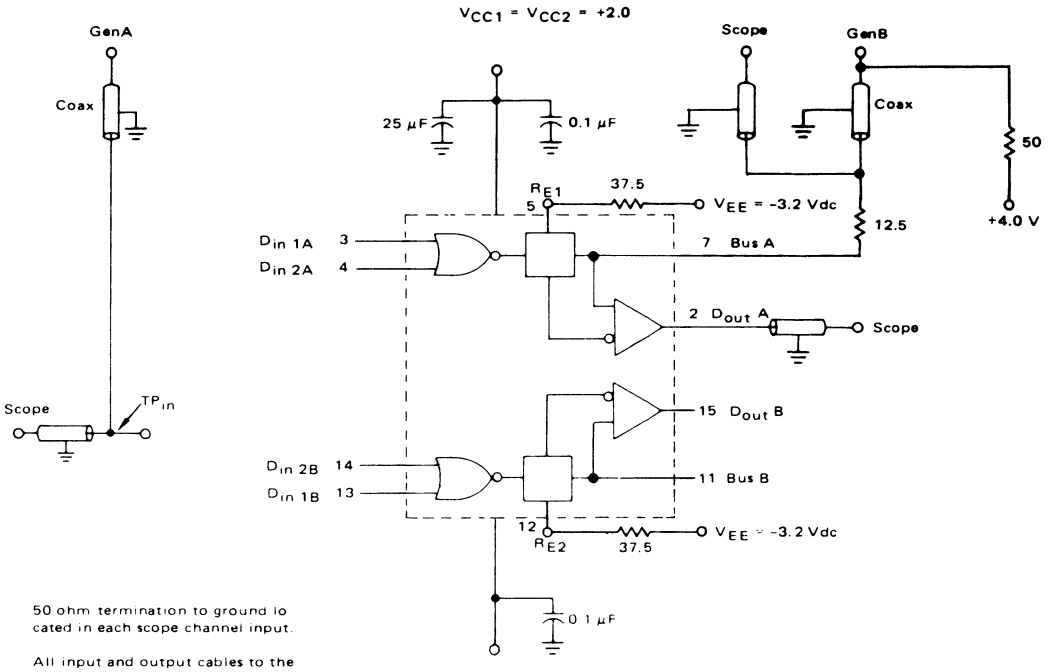
Characteristic	Symbol	-55°C Min	-55°C Max	-30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	+125°C Min	+125°C Max	Unit	Conditions
Power Supply Drain Current	I_E		107		107		97		107		107	mAdc	Inputs open. See DC Test Configuration and Logic Level Description
Input Current Data Inputs Bus Terminals	I_{inH}		 565 45		 525 40		 330 25		 330 25		 330 25	µAdc	 V_{IHMAX} to Data Inputs V_{CH} to Bus terminals, Data inputs open
Input Leakage Current Bus Terminals	I_{inL}		 35		 32		 20		 20		 20	µAdc	 V_{CL} to Bus terminals, Data inputs open
Bus Driver Zero Voltage Level	V_{BusO}	10	+10	10	+10	10	+10	10	+10	10	+10	mVdc	I_{CS} off. Data inputs open or V_{IL}
Bus Driver High Voltage Level	V_{BusH}	0.890	0.690	0.915	0.715	0.970	0.770	1.030	0.830	1.070	0.870	Vdc	I_{CS} off, V_{IHMAX} to Data Inputs. Or ICS on, Data inputs open or V_{IL}
Bus Driver Low Voltage Level	V_{BusL}	1.658	1.458	1.708	1.508	1.818	1.618	1.938	1.738	2.018	1.818	Vdc	I_{CS} on, V_{IHMAX} to Data Inputs
Bus Driver Zero Threshold Voltage Level	V_{BusOA}	30		30		30		30		30		mVdc	I_{CS} off, V_{ILAMAX} to Data inputs (one at a time)
Bus Driver High Threshold Voltage Level	V_{BusHA} ①	-0.910	-0.670	-0.935	-0.695	-0.990	-0.750	1.050	-0.810	1.090	-0.850	Vdc	I_{CS} off, V_{IHAMIN} to Data inputs (one at a time)
	V_{BusHA} ②	-0.910	-0.670	-0.935	-0.695	-0.990	-0.750	1.050	-0.810	1.090	-0.850	Vdc	I_{CS} on, V_{ILAMAX} to Data inputs (one at a time)
Bus Driver Low Threshold Voltage Level	V_{BusLA}		-1.438		-1.488		-1.598		-1.718		-1.798	Vdc	I_{CS} on, V_{IHAMIN} to Data inputs (one at a time)
Switching Times Propagation Delay Data to Bus Bus to Data Out	t_{pd}	 1.0 1.0	 3.2 4.6	 1.0 1.0	 3.1 4.5	 1.0 1.0	 2.9 4.3	 1.0 1.0	 3.2 4.7	 1.0 1.0	 3.4 5.0	ns	 50% to 50%. See Switching Time Test Circuit and Waveforms
Rise Time, Fall Time Data Outputs Bus Outputs	t_r, t_f	 1.0 1.0	 4.5 3.6	 1.1 1.1	 4.4 3.5	 1.1 1.1	 4.2 3.3	 1.1 1.1	 4.6 3.6	 1.0 1.0	 4.9 3.9	ns	20% to 80%

① V_{BusHA+} denotes the upper output threshold level with V_{IHAmin} applied and the external current source, I_{CS} off.
② V_{BusHA-} denotes the lower output threshold level with V_{ILAmax} applied and the external current source, I_{CS} on.

Definitions

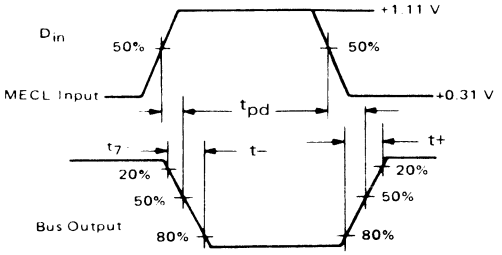
V_{CL} Low bias voltage for testing bus driver input loading
V_{CH} High bias voltage for testing bus driver input loading
I_{CS1} External current source input to the bus driver
I_{CS1A} Upper threshold level of external current source input to the bus driver
I_{CS0A} Lower threshold level of external current source input to the bus driver

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C

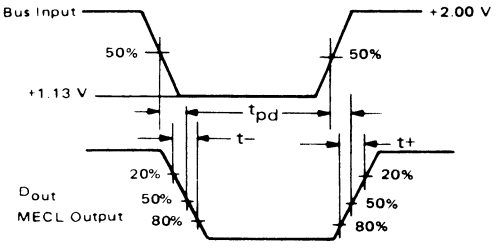


50 ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.



Data to Bus



Bus to Data

NOTE: All power supply and logic levels are shown shifted 2 volts positive.

APPLICATION INFORMATION

The MC10194/MC10594 Dual Simultaneous Bus Driver/Receiver is designed for high speed data transfer over multi-port bus lines. Full duplex data transmission can improve system performance by increasing message density and overcoming the requirement to wait two line propagation delay times between messages.

Figure 1 illustrates two types of system operation. One mode of operation is with two drivers on the bus line at locations X and Z. Any input to D_{in} X is seen at D_{out} Z one line propagation delay later. Similarly, any input to D_{in} Z is transmitted to D_{out} X. Each driver inhibits the data being sent on the bus from appearing at its receiver output, so full duplex signal transmission is possible. In addition, current source drivers allow two messages to pass on the same line so there are no timing restrictions between sending messages.

A second type of system operation is with a multi-terminal bus as illustrated in Figure 1 by points X, Y, and Z. In this mode, any one terminal can transmit data and all other points will receive the message. Alternately, any two terminals can simultaneously exchange data, but the other receivers will not see valid data.

The MC10194 uses current source line driving and is designed to operate with a load to V_{CC} (normally ground). This load is usually the line termination resistors at each end of the line as shown in Figure 2. In addition, to match the driver to a given impedance line, an external resistor equal to one-half the line termination resistor value is connected between the R_E output and V_{EE}. When the circuit is used with a multi-terminal bus, each driver must have the resistor between R_E and V_{EE}, but the termination resistors are required only at each end of the bus line.

Each MC10194 driver in a package is capable of driving 75-ohm lines. Higher impedance lines may be used with no loss of performance if the line is properly matched with R_E. If it is desirable to drive 50-ohm lines, both drivers in a package should be operated in parallel with each having 50-ohm resistors at R_E and the driver outputs both connected to the 50-ohm bus line.

To allow very high data rates, the rise and fall times on the bus line are quite fast (typically 1.0 ns). With full duplex operation, it is possible to get a crosstalk pulse of several hundred mV at a receiver output. A 10-20 pF capacitor connected between each driver output and V_{EE} will slow down the rise and fall times, greatly reduce any crosswalk pulse, and still give good system performance.

The adjustable current source drive feature of the MC10194 makes this circuit a useful output driver for many applications. For example, it is possible to drive the 50-ohm to ground load required by many interface systems. This driver will sink the 14 to 18 mA required to meet the AEC Committee specification for Nuclear Instrument Modules. The MC10114 MECL Line Receiver makes a good interface receiver for the MC10194 driver in these applications.

FIGURE 1 – MC10194/MC10594 SYSTEM OPERATION

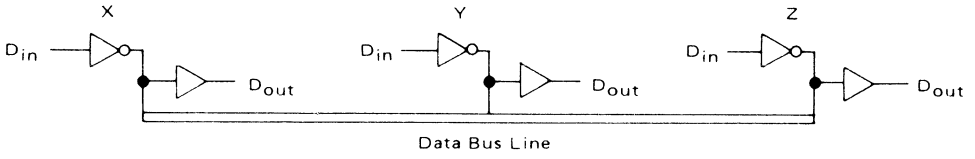
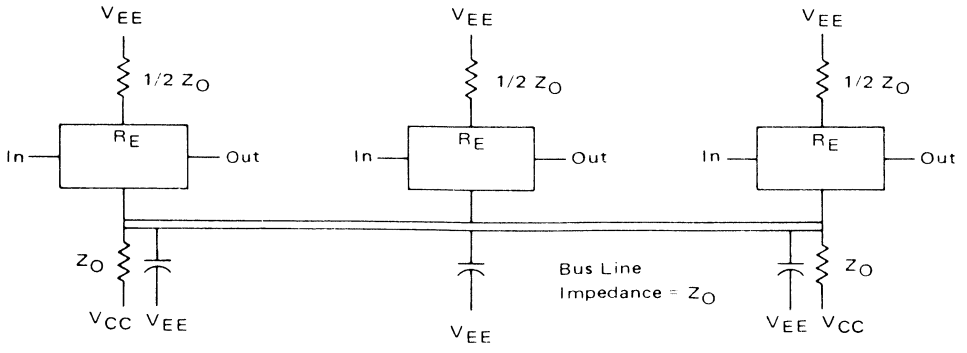
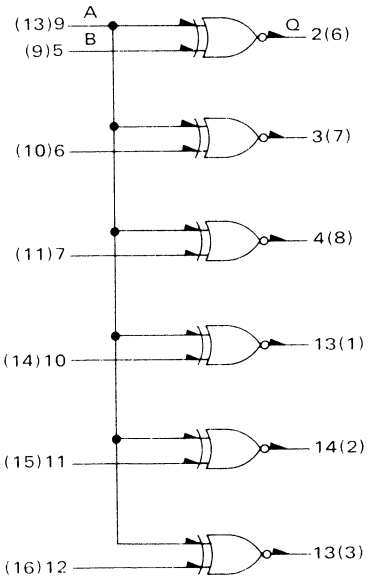


FIGURE 2 – BUS LINE INTERFACE



MC10195/MC10595

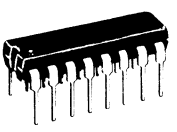
HEX INVERTER/BUFFER



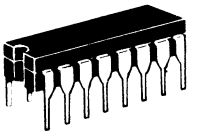
TRUTH TABLE

Inputs		Output
A	B	Q
L	L	H
L	H	L
H	L	L
H	H	H

The MC10195/MC10595 has an enable input which when placed low or left open allows use as inverters. With the enable at a high logic level the MC10195/MC10595 is a hex buffer, useful for high fanout clock driving and reducing stub lengths on long bus lines.

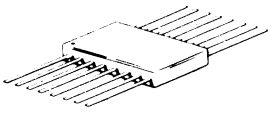


P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10195 Only



L SUFFIX
CERAMIC PACKAGE
CASE 620

V_{CC1} = Pin 1(5)
V_{CC2} = Pin 16(4)
V_{EE} = Pin 8(12)



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10595 only

P_D = 200 mW typ/pkg (No Load)
t_{pd} = 2.8 ns typ (B - Q)
= 3.8 ns typ (A - Q)

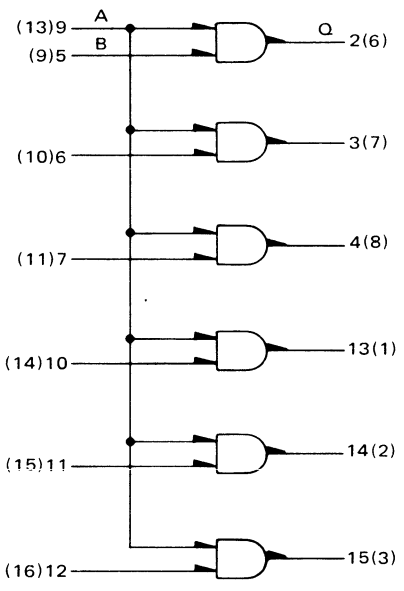
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	54	–	54	–	49	–	54	–	54	mAdc
Input Current	I_{inH}											μAdc
Pins 5,6,7,10,11,12		–	450	–	425	–	265	–	265	–	265	
Pin 9			495		460	–	290	–	290	–	290	
Switching Times												ns
Propagation Delay	t_{pd}											
Data (B)		1.0	4.3	1.1	4.2	1.1	4.0	1.1	4.4	1.0	4.7	
Enable (A)		1.0	5.4	1.1	5.2	1.1	5.0	1.1	5.4	1.0	5.9	
Rise Time, Fall Time (20% to 80%)	t+,t−	1.0	4.9	1.1	4.7	1.1	4.5	1.1	5.0	1.0	5.3	ns

-55°C and +125°C test values apply to MC105xx devices only.

MC10197/MC10597

HEX AND GATE

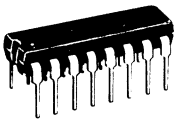


V_{CC1} = Pin 1(5)
V_{CC2} = Pin 16(4)
V_{EE} = Pin 8(12)

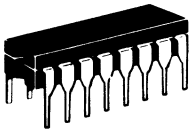
P_D = 200 mW typ/pkg (No Load)
t_{pd} = 2.8 ns typ (B–Q)
= 3.8 ns typ (A–Q)

TRUTH TABLE

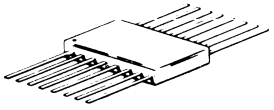
Inputs		Output
A	B	Q
L	L	L
L	H	L
H	L	L
H	H	H



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10197 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10597 only

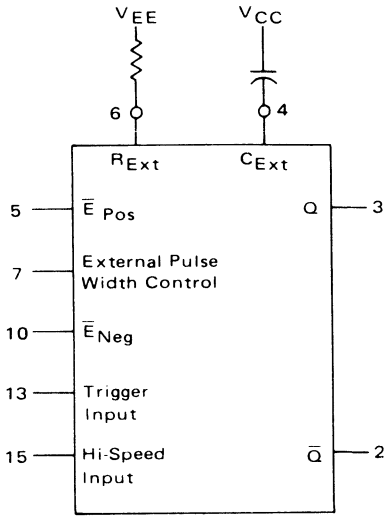
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C Min	−55°C Max	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	I_E	–	54	–	54	–	49	–	54	–	54	mAdc
Input Current	I_{inH}											μAdc
Pins 5,6,7,10,11,12		–	450	–	425	–	265	–	265	–	265	
Pin 9		–	495	–	460	–	290	–	290	–	290	
Switching Times												ns
Propagation Delay	t_{pd}											
Data (B)		1.0	4.3	1.1	4.2	1.1	4.0	1.1	4.4	1.0	4.7	
Enable (A)		1.0	5.4	1.1	5.3	1.1	5.0	1.1	5.5	1.0	5.9	
Rise Time, Fall Time (20% to 80%)	t+,t−	1.0	4.9	1.1	4.7	1.1	4.5	1.1	5.0	1.0	5.3	ns

−55°C and +125°C test values apply to MC105xx devices only.

MC10198

MONOSTABLE MULTIVIBRATOR



V_{CC1} = Pin 1
V_{CC2} = Pin 16
V_{EE} = Pin 8

The MC10198 is a retriggerable monostable multivibrator. Two enable inputs permit triggering on any combination of positive or negative edges as shown in the accompanying table. The trigger input is buffered by Schmitt triggers making it insensitive to input rise and fall times.

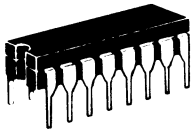
The pulse width is controlled by an external capacitor and resistor. The resistor sets a current which is the linear discharge rate of the capacitor. Also, the pulse width can be controlled by an external current source or voltage (see applications information).

For high-speed response with minimum delay, a hi-speed input is also provided. This input bypasses the internal Schmitt triggers and the output responds within 2 nanoseconds typically.

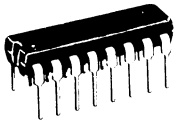
Output logic and threshold levels are standard MECL 10,000. Test conditions are per Table 2. Each "Precondition" referred to in Table 2 is per the sequence of Table 1.

TRUTH TABLE

INPUT		OUTPUT
$\bar{E}_{Pos}$	$\bar{E}_{Neg}$	
L	L	Triggers on both positive & negative input slopes
L	H	Triggers on positive input slope
H	L	Triggers on negative input slope
H	H	Trigger is disabled



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

P_D = 415 mW typ/pkg (No Load)
t_{pd} = 4.0 ns typ Trigger Input to Q
2.0 ns typ Hi-Speed Input to Q

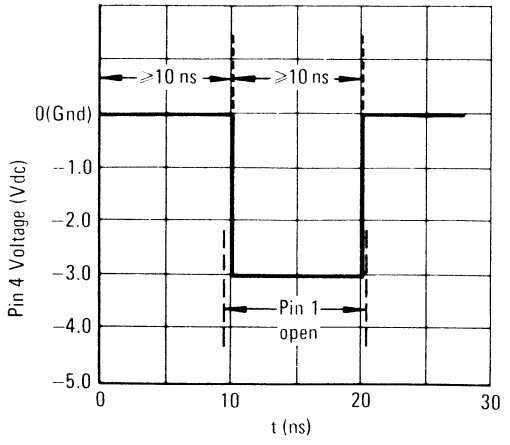
Min Timing Pulse Width	PW_{Qmin}	10 ns typ (1)
Max Timing Pulse Width	PW_{Qmax}	>10 ns typ (2)
Min Trigger Pulse Width	PW_T	2.0 ns typ
Min Hi Speed Trigger Pulse Width	PW_{HS}	3.0 ns typ
Enable Setup Time	t_{set}	1.0 ns typ
Enable Hold Time	t_{hold}	1.0 ns typ

(1) C_{Ext} = 0 (Pin 4 open), R_{Ext} = 0 (Pin 6 to V_{EE})
(2) C_{Ext} = 10 μF, R_{Ext} = 2.7 kΩ

ELECTRICAL CHARACTERISTICS

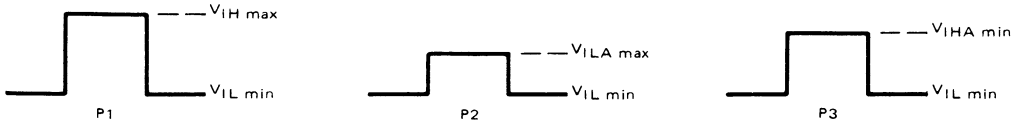
Characteristic	Symbol	−30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	110	–	100	–	110	mAdc
Input Current	I_{inH}							μAdc
Pin 5, 10		–	415	–	260	–	260	
Pin 13		–	350	–	220	–	220	
Pin 15		–	560	–	350	–	350	
Switching Times								ns
Propagation Delay	t_{pd}							
Trigger		2.5	6.5	2.5	5.5	2.5	6.5	
Hi-Speed		1.5	3.2	1.5	2.8	1.5	3.2	
Rise Time, Fall Time (20% to 80%)	t+,t−	1.5	4.0	1.5	3.5	1.5	4.0	ns

TABLE 1 – PRECONDITION SEQUENCE



1. At t = 0 a.) Apply V_{IHmax} to Pin 5 and 10.
   b.) Apply V_{ILmin} to Pin 15.
   c.) Ground Pin 4.
2. At t ≥ 10 ns a.) Open Pin 1.
   b.) Apply −3.0 Vdc to Pin 4. Hold these conditions for ≥ 10 ns.
3. Return Pin 4 to Ground and perform test as indicated in Table 2.

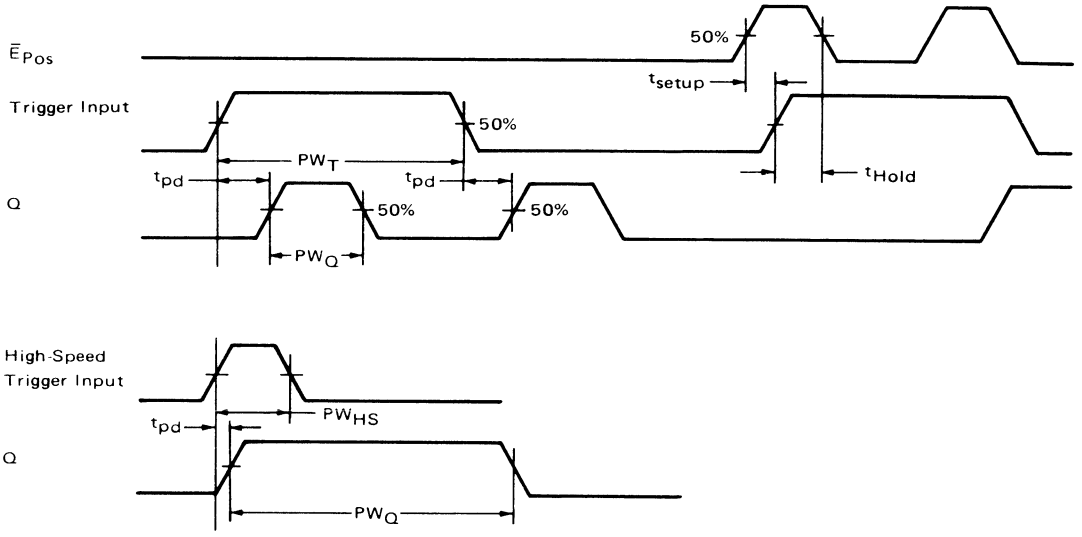
TABLE 2 – CONDITIONS FOR TESTING OUTPUT LEVELS
(See Table 1 for Precondition Sequence)



Pins 1, 16 = V_{CC} = Ground
Pins 6, 8 = V_{EE} = -5.2 Vdc
Outputs loaded 50 Ω to -2.0 Vdc

		Pin Conditions			
Test	P.U.T.	5	10	13	15
Precondition					
V_{OH}	2			V_{IL} min	
V_{OH}	3			P1	
Precondition					
V_{OL}	3			V_{IL} min	
V_{OL}	2			P1	
Precondition					
V_{OHA}	2				V_{ILA} max
V_{OHA}	3				V_{IHA} min
Precondition					
V_{OHA}	2			V_{IL} min	
V_{OHA}	3			P3	
Precondition					
V_{OHA}	2			P2	
V_{OHA}	3			P3	
Precondition					
V_{OHA}	2		V_{IH} max	P2	
V_{OHA}	3		V_{IH} max	P3	
Precondition					
V_{OHA}	2		V_{IH} max	P1	
V_{OHA}	3		V_{IH} max	P1	
Precondition					
V_{OHA}	2		V_{IHA} min	P1	
V_{OHA}	3		V_{ILA} max	P1	
Precondition					
V_{OLA}	3				V_{ILA} max
V_{OLA}	2				V_{IHA} min
Precondition					
V_{OLA}	2			V_{IL} min	
V_{OLA}	3			V_{IL} min	
Precondition					
V_{OLA}	3			P2	
V_{OLA}	2			P3	
Precondition					
V_{OLA}	3		V_{IH} max	P2	
V_{OLA}	2		V_{IH} max	P3	
Precondition					
V_{OLA}	3	V_{IHA} min	V_{IH} max	P1	
V_{OLA}	2	V_{ILA} max	V_{IH} max	P1	
Precondition					
V_{OLA}	3	V_{IH} max	V_{IHA} min	P1	
V_{OLA}	2	V_{IH} max	V_{ILA} max	P1	

SWITCHING TIME WAVEFORMS



CIRCUIT OPERATION

1. PULSE WIDTH TIMING—The pulse width is determined by the external resistor and capacitor. The MC10198 also has an internal resistor (nominally 284 ohms) that can be used in series with R_{Ext}. Pin 7, the external pulse width control, is a constant voltage node (-3.60 V nominally). A resistance connected in series from this node to V_{EE} sets a constant timing current I_T. This current determines the discharge rate of the capacitor:

$$I_T = C_{Ext} \frac{\Delta V}{\Delta T}$$

where

ΔT = pulse width

ΔV = 1.9 V change in capacitor voltage

Then:

$$\Delta T = C_{Ext} \frac{1.9\ V}{I_T}$$

If R_{Ext} + R_{Int} are in series to V_{EE}:

$$I_T = [(-3.60\ V) - (-5.2\ V)] \div [R_{Ext} + 284\ \Omega]$$

$$I_T = 1.6\ V/(R_{Ext} + 284)$$

The timing equation becomes:

$$\Delta T = [(C_{Ext})(1.9\ V)] \div [1.6\ V/(R_{Ext} + 284)]$$

$$\Delta T = C_{Ext}(R_{Ext} + 284)\ 1.19$$

where ΔT = Sec

R_{Ext} = Ohms

C_{Ext} = Farads

Figure 2 shows typical curves for pulse width versus C_{Ext} and R_{Ext} (total resistance includes R_{Int}). Any low leakage capacitor can be used and R_{Ext} can vary from 0 to 16 k ohms. Note that for capacitance less than 20 to 30 pF, actual pulse width tends to be longer than values calculated by the timing equation.

2. TRIGGERING—The $\bar{E}_{Pos}$ and $\bar{E}_{Neg}$ inputs control the trigger input. The MC10198 can be programmed to trigger on the positive edge, negative edge, or both. Also, the trigger input can be totally disabled. The truth table is shown on the first page of the data sheet.

The device is totally retriggerable. However, as duty cycle approaches 100%, pulse width jitter can occur due to the recovery time of the circuit. Recovery time is basically dependent on capacitance C_{Ext}. Figure 3 shows typical recovery time versus capacitance at I_T = 5 mA.

FIGURE 1 –

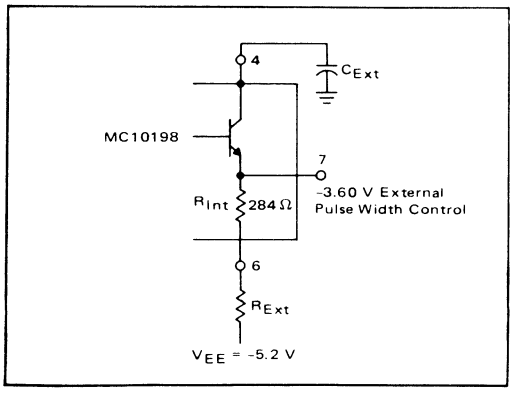


FIGURE 2 – TIMING PULSE WIDTH versus C_{Ext} and R_{Ext}

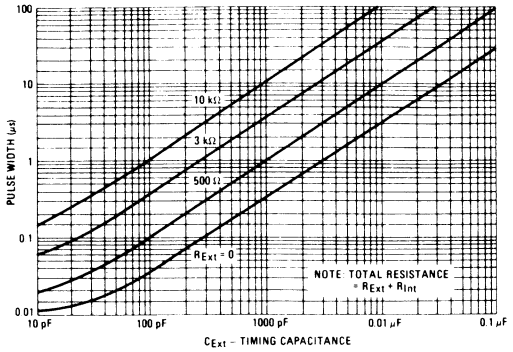
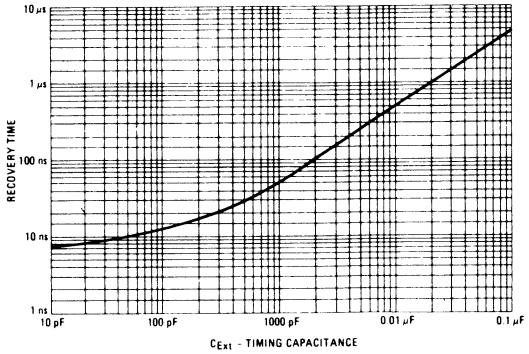


FIGURE 3 – RECOVERY TIME versus C_{Ext} @ I_T = 5 mA



3. HI-SPEED INPUT – This input is used for stretching very narrow pulses with minimum delay between the output pulse and the trigger pulse. The trigger input should be disabled when using the high-speed input. The MC10198 triggers on the rising edge using this input, and input pulse width should be narrow, typically less than 10 nanoseconds.

USAGE RULES

1. Capacitor lead lengths should be kept very short to minimize ringing due to fast recovery rise times.

2. The $\overline{E}$ inputs should *not* be tied to ground to establish a high logic level. A resistor divider or diode can be used to establish a −0.7 to −0.9 voltage level.

3. For optimum pulse width stability versus temperature and power supply variation, a nominal timing current of approximately 0.5 mA is used. Figures 4 and 5 show typical voltage change at Pin 7 for power supply and temperature variation. Figure 6 shows typical pulse width versus temperature and power supply variation.

4. Pulse Width modulation can be attained with the EXTERNAL PULSE WIDTH CONTROL. The timing current can be altered to vary the pulse width. Two schemes are:

(a) The internal resistor is not used. A dependent current source is used to set the timing current as shown in Figure 7. A graph of pulse width versus timing current (C_{Ext} = 13 pF) is shown in Figure 8.

(b) A control voltage can also be used to vary the pulse width using an additional resistor (Figure 9). The current (I_T + I_C) is set by the voltage drop across R_{Int} + R_{Ext}. The control current I_C modifies I_T and alters the pulse width. Current I_C should never force I_T to zero. R_C typically 1 kΩ.

5. The MC10198 can be made non-retriggerable. The Q output is fed back to disable the trigger input during the triggered state (Figure 10). The example shows a positive triggered configuration, a similar configuration can be made for negative triggering.

FIGURE 4 – TYPICAL VOLTAGE AT PIN 7 (EXTERNAL PULSE WIDTH CONTROL) versus SUPPLY VOLTAGE V_{EE} @ I_T = 0.5 mA, TEMPERATURE = 25°C

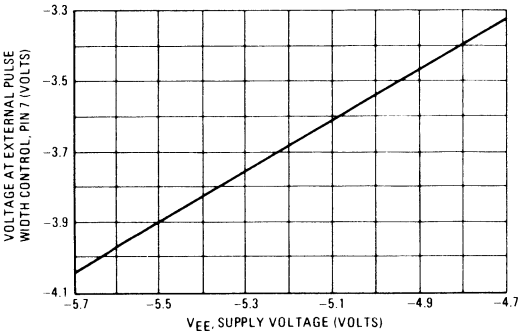


FIGURE 5 – TYPICAL VOLTAGE AT PIN 7 (EXTERNAL PULSE WIDTH CONTROL) versus TEMPERATURE @ I_T = 0.5 mA, V_{EE} = −5.20 VOLTS

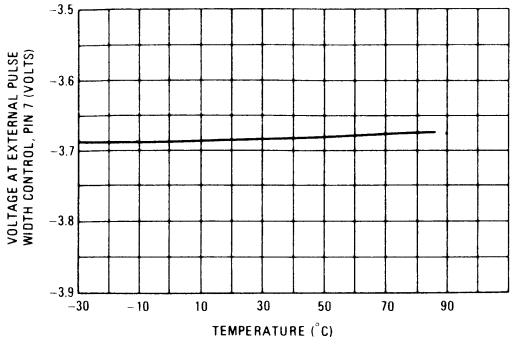


FIGURE 6 – PULSE WIDTH versus TEMPERATURE AND SUPPLY VOLTAGE

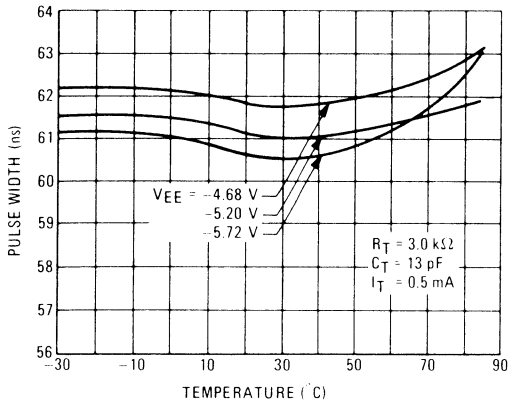


FIGURE 7

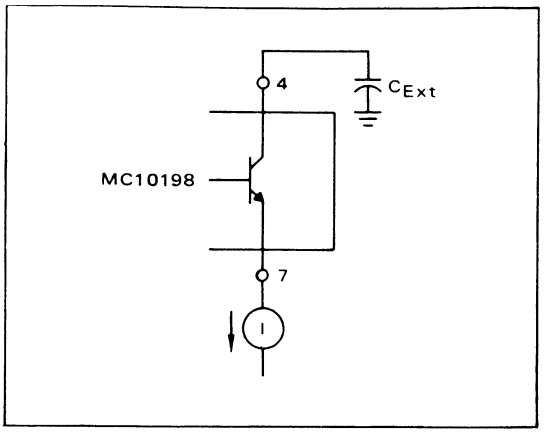


FIGURE 8 – PULSE WIDTH versus I_T @ C_{Ext} = 13 pF

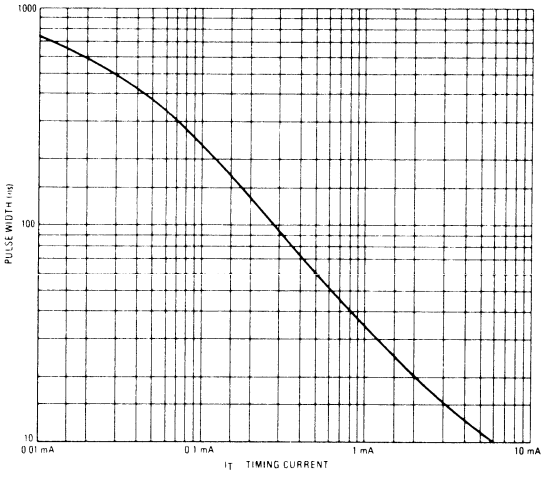


FIGURE 9

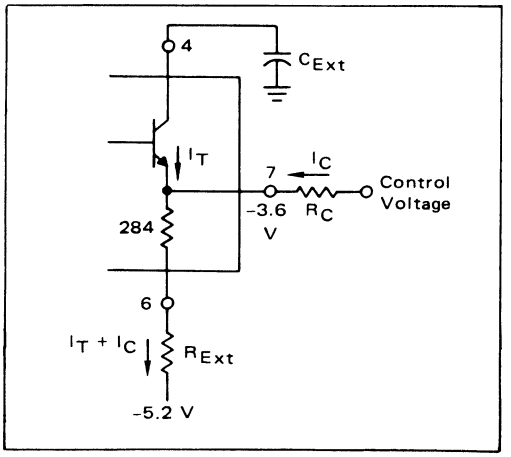
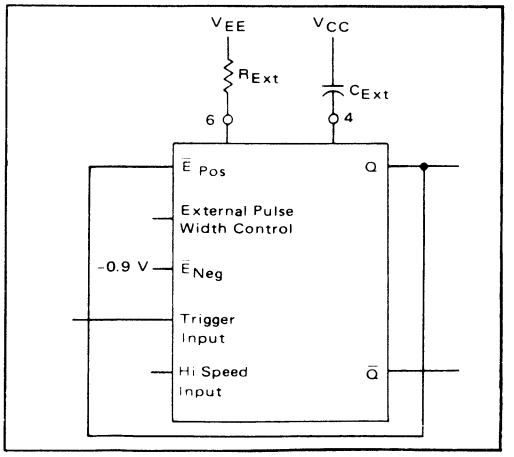


FIGURE 10



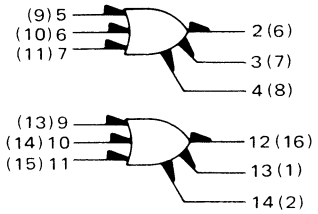
MC10210/MC10610

HIGH-SPEED DUAL 3-INPUT 3-OUTPUT OR GATE

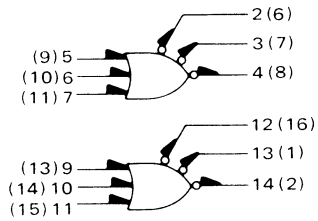
MC10211/MC10611

HIGH-SPEED DUAL 3-INPUT 3-OUTPUT NOR GATE

MC10210/MC10610



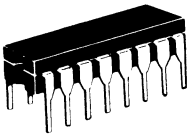
MC10211/MC10611



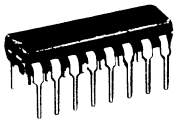
The MC10210/MC10610 and MC10211/MC10611 are higher speed versions of the MC10110/MC10111. They are pin-for-pin replacements for those devices. Three V_{CC} pins are provided and each one should be used.

V_{CC1} = 1 (5), 15 (3)
V_{CC2} = 16 (4)
V_{EE} = 8 (12)

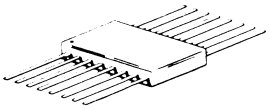
P_D = 160 mW typ/pkg (No Load)
t_{pd} = 1.5 ns typ (All Outputs Loaded)
t^+, t^- = 1.5 ns typ (20% to 80%)
(All Outputs Loaded)



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10210/MC10211
only



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10610/MC10611
only

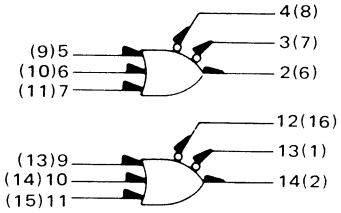
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	-55°C		-30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	42	–	42	–	38	–	42	–	42	mAdc
Input Current	I_{inH}	–	700	–	650	–	410	–	410	–	410	μAdc
Switching Times												ns
Propagation Delay	t_{pd}	1.0	2.9	1.0	2.6	1.0	2.5	1.0	2.8	1.0	3.0	
Rise Time, Fall Time (20% to 80%)	t^+, t^-	1.0	2.9	1.0	2.6	1.0	2.5	1.0	2.8	1.0	3.0	ns

-55°C and +125°C test values apply to MC106xx devices only.

MC10212/MC10612

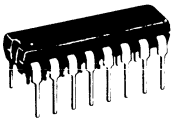
HIGH-SPEED DUAL 3-INPUT 3-OUTPUT OR/NOR GATE



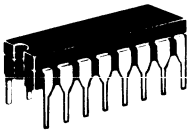
P_D = 160 mW typ/pkg (No Load)
t_{pd} = 1.5 ns typ (All Outputs Loaded)
t_+, t_- = 1.5 ns typ (20% to 80%)
(All Outputs Loaded)

Three V_{CC} pins are provided and each one should be used.

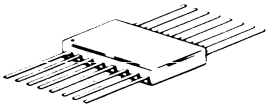
V_{CC1} = 1(5), 15(3)
V_{CC2} = 16(4)
V_{EE} = 8(12)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10212 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10612 only

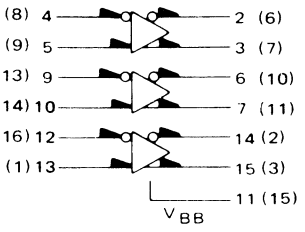
Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	42	–	42	–	38	–	42	–	42	mAdc
Input Current	I_{inH}	–	700	–	650	–	410	–	410	–	410	μAdc
Switching Times Propagation Delay	t_{pd}	1.0	2.9	1.0	2.6	1.0	2.5	1.0	2.8	1.0	3.0	ns
Rise Time, Fall Time (20% to 80%)	t+,t−	1.0	2.9	1.0	2.6	1.0	2.5	1.0	2.8	1.0	3.0	ns

−55°C and +125°C test values apply to MC106xx devices only.

MC10216/MC10616

HIGH-SPEED TRIPLE LINE RECEIVER

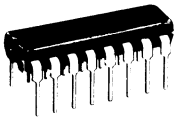


The MC10216/MC10616 is a high speed triple differential amplifier designed for use in sensing differential signals over long lines. The bias supply (V_{BB}) is made available at pin 11 to make the device useful as a Schmitt trigger, or in other applications where a stable reference voltage is necessary.

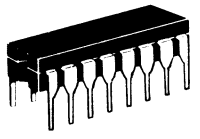
Active current sources provide the MC10216 with excellent common mode noise rejection. If any amplifier in a package is not used, one input of that amplifier must be connected to V_{BB} (pin 11) to prevent upsetting the current source bias network.

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

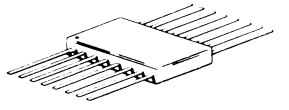
P_D = 100 mW typ/pkg (No Load)
t_{pd} = 1.8 ns typ (Single ended)
= 1.5 ns typ (Differential)



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10216 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10616 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

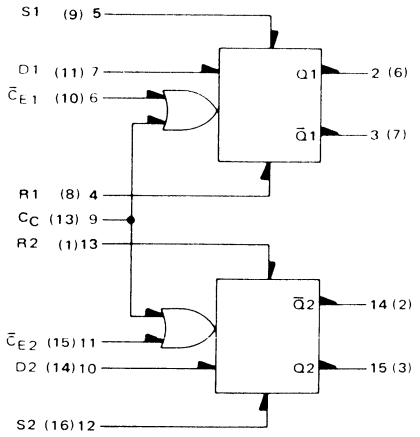
One input from each gate must be tied to V_{BB} during testing.

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	--	28	--	27	--	25	--	27	--	28	mAdc
Input Current	I_{inH}	--	195	--	180	--	115	--	115	--	115	μAdc
	I_{CBO}	--	1.5	--	1.5	--	1.0	--	1.0	--	1.0	μAdc
Reference Voltage	V_{BB}	-1.440	-1.320	-1.420	-1.280	-1.350	-1.230	-1.295	-1.150	-1.240	-1.120	Vdc
Switching Times												ns
Propagation Delay	t_{pd}	1.0	2.7	1.0	2.6	1.0	2.5	1.0	2.8	1.0	2.9	
Rise Time, Fall Time (20% to 80%)	t_+, t_-	1.0	2.7	1.0	2.6	1.0	2.5	1.0	2.8	1.0	2.9	ns

−55°C and +125°C test values apply to MC106xx devices only.

MC10231/MC10631

HIGH-SPEED DUAL TYPE D MASTER-SLAVE FLIP-FLOP



The MC10231/MC10631 is a dual master-slave type D flip flop. Asynchronous Set (S) and Reset (R) override Clock (C_C) and Clock Enable ($\bar{C}_E$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.

The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data (D) input will not affect the output information at any other time due to master slave construction.

R-S TRUTH TABLE

R	S	Q_{n+1}
L	L	Q_n
L	H	H
H	L	L
H	H	N.D.

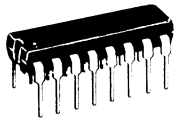
N.D. = Not Defined

CLOCKED TRUTH TABLE

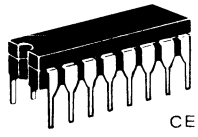
C	D	Q_{n+1}
L	ϕ	Q_n
H*	L	L
H*	H	H

ϕ = Don't Care $C = C_E + C_C$

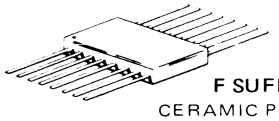
*A clock H is a clock transition from a low to a high state.



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10231 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



P_D = 270 mW typ/pkg (No Load)
f_{Tog} = 225 MHz typ

F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10631 only

$V_{CC}1$ = Pin 1 (5)
$V_{CC}2$ = Pin 16 (4)
V_{EE} = Pin 8 (12)

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125oC		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	72	–	72	–	65	–	72	–	72	mAdc
Input Current	I_{inH}											μAdc
Pins 6,7,10,11		–	375	–	350	–	220	–	220	–	220	
Pin 9		–	495	–	460	–	290	–	290	–	290	
Pins 4,5,12,13		–	700	–	650	–	410	–	410	–	410	
Switching Times												ns
Propagation Delay	t_{pd}											
Clock		1.3	3.7	1.5	3.4	1.5	3.3	1.6	3.7	1.2	3.9	
Set, Reset		1.0	3.7	1.1	3.4	1.1	3.3	1.2	3.7	1.0	3.9	
Rise Time, Fall Time (20% to 80%)	t+,t−	1.0	3.4	0.9	3.3	1.0	3.1	1.0	3.6	1.0	3.6	ns
Setup Time	t_{set}	1.5	–	1.5	–	1.0	–	1.5	–	1.5	–	ns
Hold Time	t_{hold}	0.9	–	0.9	–	0.75	–	0.9	–	0.9	–	ns
Toggle Frequency	f_{Tog}	200	–	200	–	200	–	200	–	200	–	MHz

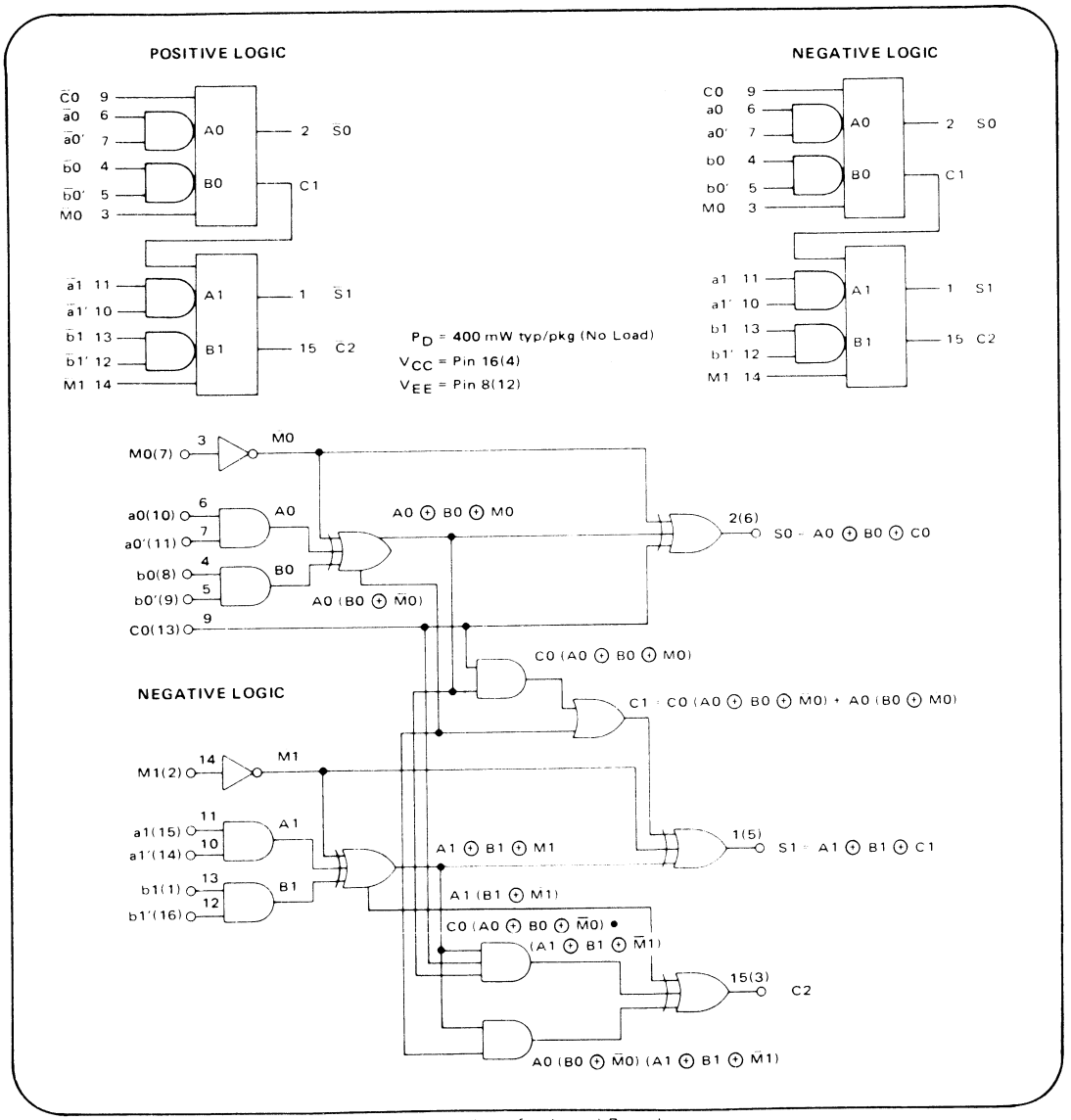
−55°C and +125°C test values apply to MC106xx devices only.

MC10287/MC10687

HIGH-SPEED 2 x 1 BIT ARRAY MULTIPLIER BLOCK

The MC10287/MC10687 is a dual high speed iterative multiplier. It is designed for use as an array multiplier block. Each device is a modified full adder/subtractor that forms a single-bit binary product at each operand input of the adder. Internal carry lookahead is employed for high speed operation.

An addition or subtraction is selected by mode controls (M0, M1). The mode controls are buffered such that they can be grounded or taken to a standard high logic level to accomplish subtraction. When left open or taken to a low logic level, M0 and M1 cause addition.

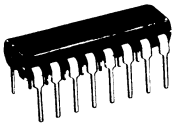


Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

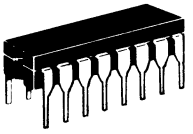
FUNCTIONAL TRUTH TABLE

M1	M0	b1	b1′	a1	a1′	b0	b0′	a0	a0′	C0	S0	S1	C2	
14	3	13	12	11	10	4	5	6	7	9	2	1	15	Word
H	H	H	H	H	H	H	H	H	H	H	H	H	H	0
H	H	H	H	H	H	H	H	H	H	L	L	L	L	1
H	H	H	H	H	H	H	H	L	L	H	L	L	L	2
H	H	H	H	H	H	H	H	L	L	L	H	L	L	3
H	H	H	H	H	H	L	L	H	H	H	L	H	H	4
H	H	H	H	H	H	L	L	H	H	L	H	H	H	5
H	H	H	H	H	H	L	L	L	L	H	H	H	H	6
H	H	H	H	H	H	L	L	L	L	L	L	L	L	7
H	H	H	H	L	L	H	H	H	H	H	L	L	L	8
H	H	H	H	L	L	H	H	H	H	L	L	H	L	9
H	H	H	H	L	L	H	H	L	L	H	L	H	L	10
H	H	H	H	L	L	H	H	L	L	L	H	H	L	11
H	H	H	H	L	L	L	L	H	H	H	L	L	L	12
H	H	H	H	L	L	L	L	H	H	L	H	L	L	13
H	H	H	H	L	L	L	L	L	L	H	H	L	L	14
H	H	H	H	L	L	L	L	L	L	L	L	H	L	15
H	H	L	L	H	H	H	H	H	H	H	H	L	H	16
H	H	L	L	H	H	H	H	H	H	L	L	H	H	17
H	H	L	L	H	H	H	H	L	L	H	L	H	H	18
H	H	L	L	H	H	H	H	L	L	L	H	H	H	19
H	H	L	L	H	H	L	L	H	H	H	L	L	H	20
H	H	L	L	H	H	L	L	H	H	L	H	L	H	21
H	H	L	L	H	H	L	L	L	L	H	H	L	H	22
H	H	L	L	H	H	L	L	L	L	L	L	H	H	23
H	H	L	L	L	L	H	H	H	H	H	H	H	H	24
H	H	L	L	L	L	H	H	H	H	L	L	L	L	25
H	H	L	L	L	L	H	H	L	L	H	L	L	L	26
H	H	L	L	L	L	H	H	L	L	L	H	L	L	27
H	H	L	L	L	L	L	L	H	H	H	L	H	H	28
H	H	L	L	L	L	L	L	H	H	L	H	H	H	29
H	H	L	L	L	L	L	L	L	L	H	H	H	H	30
H	H	L	L	L	L	L	L	L	L	L	L	L	L	31
H	L	H	H	H	H	H	H	H	H	H	H	H	H	32
H	L	H	H	H	H	H	H	H	H	L	L	H	H	33
H	L	H	H	H	H	H	H	L	L	H	L	H	H	34
H	L	H	H	H	H	H	H	L	L	L	H	L	L	35
H	L	H	H	H	H	L	L	H	H	H	L	H	H	36
H	L	H	H	H	H	L	L	H	H	L	H	L	L	37
H	L	H	H	H	H	L	L	L	L	H	H	L	L	38
H	L	H	H	H	H	L	L	L	L	L	L	L	L	39
H	L	H	H	L	L	H	H	H	H	H	H	L	L	40
H	L	H	H	L	L	H	H	H	H	L	L	L	L	41
H	L	H	H	L	L	H	H	L	L	H	L	L	L	42
H	L	H	H	L	L	H	H	L	L	L	H	H	L	43
H	L	H	H	L	L	L	L	H	H	H	L	L	L	44
H	L	H	H	L	L	L	L	H	H	L	H	H	L	45
H	L	H	H	L	L	L	L	L	L	H	H	H	L	46
H	L	H	H	L	L	L	L	L	L	L	L	H	L	47
H	L	L	L	H	H	H	H	H	H	H	H	L	H	48
H	L	L	L	H	H	H	H	H	H	L	L	L	H	49
H	L	L	L	H	H	H	H	L	L	H	L	L	H	50
H	L	L	L	H	H	H	H	L	L	L	H	H	H	51
H	L	L	L	H	H	L	L	H	H	H	L	L	H	52
H	L	L	L	H	H	L	L	H	H	L	H	H	H	53
H	L	L	L	H	H	L	L	L	L	H	H	H	H	54
H	L	L	L	H	H	L	L	L	L	L	H	H	H	55
H	L	L	L	L	L	H	H	H	H	H	H	H	H	56
H	L	L	L	L	L	H	H	H	H	L	L	H	H	57
H	L	L	L	L	L	H	H	L	L	H	L	H	L	58
H	L	L	L	L	L	H	H	L	L	L	H	L	L	59
H	L	L	L	L	L	L	L	H	H	H	L	H	H	60
H	L	L	L	L	L	L	L	H	H	L	H	L	L	61
H	L	L	L	L	L	L	L	L	L	H	L	L	L	62
H	L	L	L	L	L	L	L	L	L	L	L	L	L	63
L	H	H	H	H	H	H	H	H	H	H	H	H	H	64
L	H	H	H	H	H	H	H	H	H	L	L	L	H	65
L	H	H	H	H	H	H	H	L	L	H	L	L	H	66
L	H	H	H	H	H	H	H	L	L	L	H	L	H	67

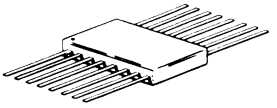
M1	M0	b1	b1′	a1	a1′	b0	b0′	a0	a0′	C0	S0	S1	C2	
14	3	13	12	11	10	4	5	6	7	9	2	1	15	Word
L	H	H	H	H	H	L	L	H	H	H	L	H	H	68
L	H	H	H	H	H	L	L	H	H	L	H	H	H	69
L	H	H	H	H	H	L	L	L	L	H	H	H	H	70
L	H	H	H	H	H	L	L	L	L	L	L	L	H	71
L	H	H	H	L	L	H	H	H	H	H	H	L	H	72
L	H	H	H	L	L	H	H	H	H	L	L	H	L	73
L	H	H	H	L	L	H	H	L	L	H	L	H	L	74
L	H	H	H	L	L	H	H	L	L	L	H	H	L	75
L	H	H	H	L	L	L	L	H	H	H	L	L	H	76
L	H	H	H	L	L	L	L	H	H	L	H	L	H	77
L	H	H	H	L	L	L	L	L	L	H	H	L	H	78
L	H	H	H	L	L	L	L	L	L	L	L	H	L	79
L	H	L	L	H	H	H	H	H	H	H	H	L	H	80
L	H	L	L	H	H	H	H	H	H	L	L	H	L	81
L	H	L	L	H	H	H	H	L	L	H	L	H	L	82
L	H	L	L	H	H	H	H	L	L	L	H	H	L	83
L	H	L	L	H	H	L	L	H	H	H	L	L	H	84
L	H	L	L	H	H	L	L	H	H	L	H	L	H	85
L	H	L	L	H	H	L	L	L	L	H	H	L	H	86
L	H	L	L	H	H	L	L	L	L	L	L	H	L	87
L	H	L	L	L	L	H	H	H	H	H	H	H	L	88
L	H	L	L	L	L	H	H	H	H	L	L	L	L	89
L	H	L	L	L	L	H	H	L	L	H	L	L	L	90
L	H	L	L	L	L	H	H	L	L	L	H	L	L	91
L	H	L	L	L	L	L	L	H	H	H	L	H	L	92
L	H	L	L	L	L	L	L	H	H	L	H	H	L	93
L	H	L	L	L	L	L	L	L	L	H	H	H	L	94
L	H	L	L	L	L	L	L	L	L	L	L	L	L	95
L	L	H	H	H	H	H	H	H	H	H	H	H	H	96
L	L	H	H	H	H	H	H	H	H	L	L	H	H	97
L	L	H	H	H	H	H	H	L	L	H	L	H	H	98
L	L	H	H	H	H	H	H	L	L	L	H	L	H	99
L	L	H	H	H	H	L	L	H	H	H	L	H	H	100
L	L	H	H	H	H	L	L	H	H	L	H	L	H	101
L	L	H	H	H	H	L	L	L	L	H	H	L	H	102
L	L	H	H	H	H	L	L	L	L	L	L	L	H	103
L	L	H	H	L	L	H	H	H	H	H	H	L	H	104
L	L	H	H	L	L	H	H	H	H	L	L	L	H	105
L	L	H	H	L	L	H	H	L	L	H	L	L	H	106
L	L	H	H	L	L	H	H	L	L	L	H	H	L	107
L	L	H	H	L	L	L	L	H	H	H	L	L	H	108
L	L	H	H	L	L	L	L	H	H	L	H	H	L	109
L	L	H	H	L	L	L	L	L	L	H	H	H	L	110
L	L	H	H	L	L	L	L	L	L	L	L	H	L	111
L	L	L	L	H	H	H	H	H	H	H	H	L	H	112
L	L	L	L	H	H	H	H	H	H	L	L	L	H	113
L	L	L	L	H	H	H	H	L	L	H	L	L	H	114
L	L	L	L	H	H	H	H	L	L	L	H	H	L	115
L	L	L	L	H	H	L	L	H	H	H	L	L	H	116
L	L	L	L	H	H	L	L	H	H	L	H	H	L	117
L	L	L	L	H	H	L	L	L	L	H	H	H	L	118
L	L	L	L	H	H	L	L	L	L	L	L	H	L	119
L	L	L	L	L	L	H	H	H	H	H	H	H	L	120
L	L	L	L	L	L	H	H	H	H	L	L	H	L	121
L	L	L	L	L	L	H	H	L	L	H	L	H	L	122
L	L	L	L	L	L	H	H	L	L	L	H	L	L	123
L	L	L	L	L	L	L	L	H	H	H	L	H	L	124
L	L	L	L	L	L	L	L	H	H	L	H	L	L	125
L	L	L	L	L	L	L	L	L	L	H	H	L	L	126
L	L	L	L	L	L	L	L	L	L	L	L	L	L	127
L	L	H	L	L	L	L	L	L	L	L	L	H	L	128
L	L	L	H	L	L	L	L	L	L	L	L	H	L	129
L	L	L	L	H	L	L	L	L	L	L	L	H	L	130
L	L	L	L	L	H	L	L	L	L	L	L	H	L	131
L	L	L	L	L	L	H	L	L	L	L	H	L	L	132
L	L	L	L	L	L	L	H	L	L	L	H	L	L	133
L	L	L	L	L	L	L	L	H	L	L	H	L	L	134
L	L	L	L	L	L	L	L	L	H	L	H	L	L	135



P SUFFIX
PLASTIC PACKAGE
CASE 648
MC10287 only



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650
MC10687 only

Numbers at ends of terminals denote pin numbers for L and P packages.
Numbers in parenthesis denote pin numbers for F package.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	106	–	106	–	96	–	106	–	106	mAdc
Input Current	I_{inH}											μAdc
Pins 3,14		–	340	–	320	–	200	–	200	–	200	
Pins 4,5,12,13		–	375	–	350	–	220	–	220	–	220	
Pins 6,7,10,11		–	450	–	425	–	265	–	265	–	265	
Pin 9		–	700	–	650	–	410	–	410	–	410	
Switching Times												ns
Propagation Delay	t_{pd}											
C0 to S0,C2		1.1	4.0	1.1	3.6	1.1	3.4	1.1	3.7	1.1	4.2	
C0 to S1		1.1	4.9	1.1	4.7	1.1	4.5	1.1	4.7	1.1	4.9	
a0,a0',b0,b0' to S0,C2		1.1	5.0	1.1	4.9	1.1	4.7	1.1	5.2	1.1	7.0	
a0,a0',b0,b0' to S1		2.0	6.2	1.4	6.1	1.4	5.8	1.4	6.4	2.0	6.6	
a1,a1',b1,b1' to S1,C2		1.1	4.7	1.1	4.7	1.1	4.5	1.1	4.8	1.5	5.2	
M0 to S1; M1 to C2		3.0	14	3.0	13	3.0	12.5	3.0	13.5	3.0	14.5	
M0 to C2		2.5	14	2.5	13	3.0	12.5	2.5	13.5	2.5	14.5	
Rise Time, Fall Time (20% to 80%)	t+,t−	1.1	3.4	1.1	3.3	1.1	3.1	1.1	3.4	1.1	3.6	ns

−55°C and +125°C test values apply to MC106xx devices only.

APPLICATION INFORMATION

The MC10287/687 is a stand alone fully iterative dual multiplier cell. It is intended for use in parallel multiplier arrays where maximum speed is desired. Each cell is a modified gated adder/subtractor individually controlled by a mode select line. Internal carry lookahead (also called anticipated carry) is used to minimize sum and carry out delay times.

The mode controls are specifically buffered such that they can be grounded. Normally, MECL 10,000 device inputs should not be placed at ground to establish a high logic level. However, M0 and M1 can be used at ground potential for ease of layout in large arrays.

An array multiplier is defined as a multi-input, multi-output combinational logic circuit that forms the product of two binary numbers. Binary multiplication can be treated in two categories, that is, simple magnitude multiplication and 4-quadrant multiplication (requiring both positive and negative numbers).

MAGNITUDE BINARY MULTIPLICATION

Magnitude multiplication consists of the product of two binary numbers in which all digits are number bits (no sign bit). Magnitude representation then includes only positive numbers.

Thus, for a 4-bit number X the representation is:

$$X = x_3\ x_2\ x_1\ x_0$$

A 4-bit by 4-bit product becomes:

$$Z = X \bullet Y = (x_3\ x_2\ x_1\ x_0) \bullet (y_3\ y_2\ y_1\ y_0)$$

The product consists of the sum of the single-bit products formed by this expression. The standard "parallelogram" matrix of the single-bit products (or summands) can be written:

$$\begin{array}{cccccccc} & & & & x_3y_0 & x_2y_0 & x_1y_0 & x_0y_0 \\ & & & x_3y_1 & x_2y_1 & x_1y_1 & x_0y_1 & \\ & & x_3y_2 & x_2y_2 & x_1y_2 & x_0y_2 & & \\ & x_3y_3 & x_2y_3 & x_1y_3 & x_0y_3 & & & \\ \hline z_7 & z_6 & z_5 & z_4 & z_3 & z_2 & z_1 & z_0 \end{array}$$

The MC10287 is used in an array summing the single-bit products to form the final result. It is observed that the arithmetic product of binary digits x_j and y_i is also the logical product (x_j times y_i = x_j AND y_i. The AND function on the operand inputs of the MC10287 forms the single-bit products of the matrix directly and sums them internally. For magnitude binary multiplication, the MC10287 functions as a dual full adder (M0, M1 are both low).

The partial product array can be summed using a number of different techniques. The fastest technique is some form of matrix reduction scheme that prevents carry propagation until the final level of summation. Several of these schemes are discussed in detail in Reference 1.

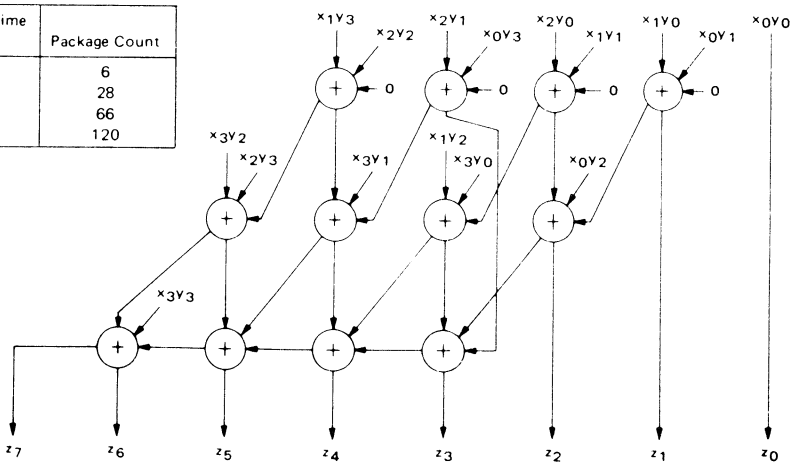
As an example, if the matrix is rearranged and written in a different form:

$$\begin{array}{cccccccc} & & & & x_0y_3 & & & \\ & & & x_1y_3 & x_3y_0 & x_2y_0 & x_1y_0 & x_0y_0 \\ & & x_2y_3 & x_3y_1 & x_2y_1 & x_1y_1 & x_0y_1 & \\ & x_3y_3 & x_3y_2 & x_2y_2 & x_1y_2 & x_0y_2 & & \\ \hline z_7 & z_6 & z_5 & z_4 & z_3 & z_2 & z_1 & z_0 \end{array}$$

TABLE 1 – TYPICAL MULTIPLY TIME FOR AN n-BIT BY n-BIT BINARY MAGNITUDE ARRAY MULTIPLIER

Number of Bits	Total Multiply Time (ns)	Package Count
4	14	6
8	25	28
12	39	66
16	44	120

FIGURE 1 – 4-BIT BY 4-BIT MAGNITUDE ARRAY MULTIPLIER



The summation of the partial products for this configuration is shown in Figure 1. The number of MC10287's for an n-bit by n-bit array is n(n-1)/2. Note also that the least significant product bit ($z_0 = x_0y_0$) is formed by an individual AND gate (negative logic).

Table 1 gives package count and typical multiplication times for n-bit by n-bit magnitude multiplier arrays. The multiply times do not include wiring delays, and the package count does not include the gate for the least significant product bit.

FOUR-QUADRANT MULTIPLICATION

Sign-magnitude and 2's complement representations are commonly used for 4-quadrant multiplication. For sign-magnitude representation, the binary word consists of a sign bit and magnitude bits which indicate the absolute value of the number. For a 4-bit example:

$$X = x_s\ x_2\ x_1\ x_0$$

For $X \bullet Y = Z$

$$Z = X \bullet Y = (x_s\ x_2\ x_1\ x_0) \bullet (y_s\ y_2\ y_1\ y_0)$$

An array multiplier for this representation consists of an (n-1)-bit by (n-1)-bit magnitude multiplier that produces the product of the magnitude bits of X and Y and of logic that produces the proper product sign bit ($z_s = x_s \oplus y_s$).

2's complement representation also includes a sign bit which is a negative bit. That is:

$$X = -x_3\ x_2\ x_1\ x_0$$

where x_3 is the sign bit. The product of two 4-bit 2's complement numbers becomes:

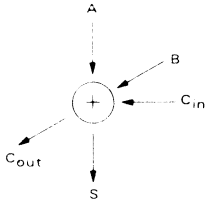
$$Z = X \bullet Y = (-x_3\ x_2\ x_1\ x_0) \bullet (-y_3\ y_2\ y_1\ y_0)$$

The matrix for this expression is:

			$-x_3y_0$	x_2y_0	x_1y_0	x_0y_0	
		$-x_3y_1$	x_2y_1	x_1y_1	x_0y_1		
	$-x_3y_2$	x_2y_2	x_1y_2	x_0y_2			
x_3y_3	$-x_2y_3$	$-x_1y_3$	$-x_0y_3$				
$-z_7$	z_6	z_5	z_4	z_3	z_2	z_1	z_0

The product is the sum of this array of single-bit products. However, notice that several summands are negative quantities. Therefore, they can not be simply added as is the magnitude binary multiplier. The subtraction capability of the MC10287 is utilized when considering these negative quantities.

A standard full adder is symbolized as:



in which all inputs are positive quantities. If one input is negative (such as B), the outputs C_{out} and S must be coded such that they can represent the 4 possible output conditions. If B can be a negative one or zero, the net output can then be:

$$\text{net output} = \begin{cases} -1 \\ 0 \\ +1 \\ +2 \end{cases}$$

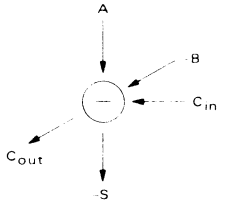
If C_{out}, whose weight is twice that of S, is assigned a positive value and S is a negative value, the above values can be represented:

$$\text{net output} = 2 \bullet C_{out} - S$$

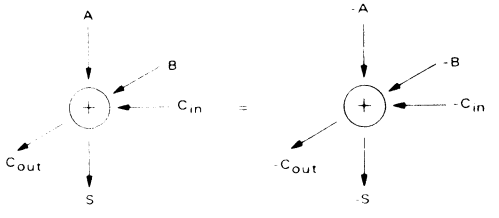
where:

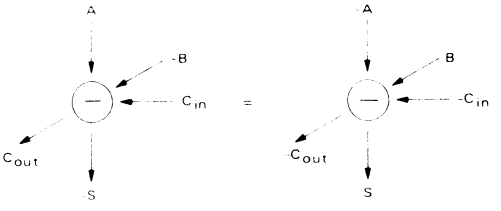
$$-1 = 0 - 1$$
$$0 = 0 - 0$$
$$+1 = 2 - 1$$
$$+2 = 2 - 0$$

If the truth table is written and logic equations generated, the result is a subtractor. That is, a subtractor used in place of a full adder produces the proper outputs. The symbol for the subtractor is:



Also, if the input variables are multiplied by -1, the outputs also are multiplied by -1. Thus, the following devices are equivalent:





A basic adder/subtractor can then handle all the varying situations that appear in the multiplication matrix.

If the 2's complement matrix is rearranged:

			$-x_0y_3$				
		$-x_1y_3$	$-x_3y_0$	x_2y_0	x_1y_0	x_0y_0	
	$-x_2y_3$	$-x_3y_1$	x_2y_1	x_1y_1	x_0y_1		
x_3y_3	$-x_3y_2$	x_2y_2	x_1y_2	x_0y_2			
$-z_7$	z_6	z_5	z_4	z_3	z_2	z_1	z_0

The adder/subtractor array for this configuration is shown in Figure 2. Care must be taken to insure that the proper mode of operation (add or subtract) appears at each summing node as a function of the positive and negative weighted inputs.

The summand matrix can be altered different ways to speed up the multiplier array. Reference 2 discusses the algorithm used with the MC10287 in detail. Also, the techniques of Reference 1 also apply to 2's complement arrays using the MC10287.

Table 2 gives typical multiply times for 2's complement arrays for n-bit by n-bit multipliers.

TABLE 2 – TYPICAL MULTIPLY TIME FOR AN n-BIT BY n-BIT 2's COMPLEMENT ARRAY MULTIPLIER

Number of Bits	Total Multiply Time (ns)	Package Count
4	14	6
8	25	28
12	39	66
16	44	120

IMPROVED SWITCHING DELAYS

The specified ac switching delays are given for output loading of 50 Ω to -2 volts. With lower output current, propagation delays will be improved and decreased multiply times can result. For output loading of 1 kΩ to V_{EE}, the following delays are typical.

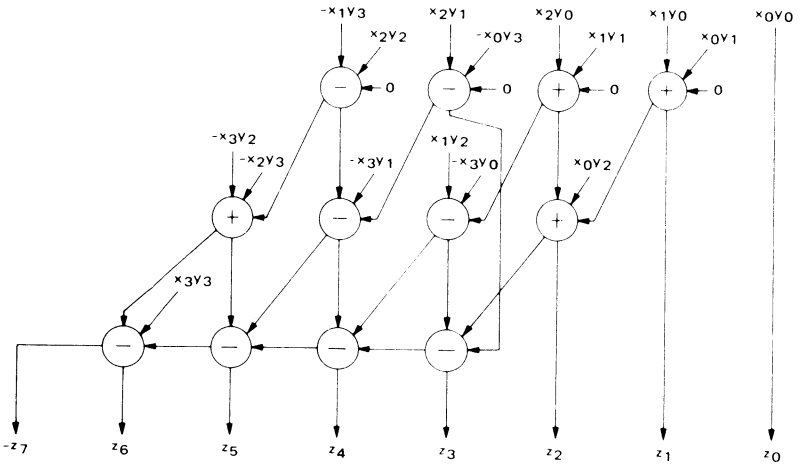
Input	Output	Delay (ns)
C0	C2	1.7
a0	C2	2.8
a0	S0	2.7
b0	S0	3.1
a0	S1	3.9
b0	S1	4.4
M0	S1	8.5

REFERENCE AND ACKNOWLEDGEMENT

The techniques for implementing the MC10287 in multiplier arrays resulted from work done originally at M.I.T. Lincoln Laboratories. Also, applications information presented here developed in part from personal correspondence with P. Blankenship of Lincoln Labs. The following references are useful in developing multipliers using the MC10287:

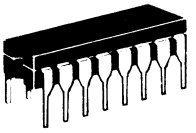
1. A. Habibi and P.A. Wintz, "Fast Multipliers," *IEEE Trans. Computers* (Short Notes), Vol. C-19, Feb. 1970, pp. 153-157.
2. S.D. Pezaris, "A 40-ns 17-Bit by 17-Bit Array Multiplier", *IEEE Trans. Computers,* Vol. C-20, Number 4, April, 1971, pp. 442-447.

FIGURE 2 – 4-BIT BY 4-BIT 2's COMPLEMENT ARRAY MULTIPLIER

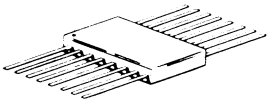


MCM10139/MCM10539

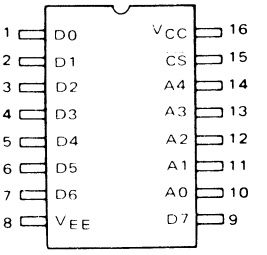
32 x 8-BIT PROGRAMMABLE READ-ONLY MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

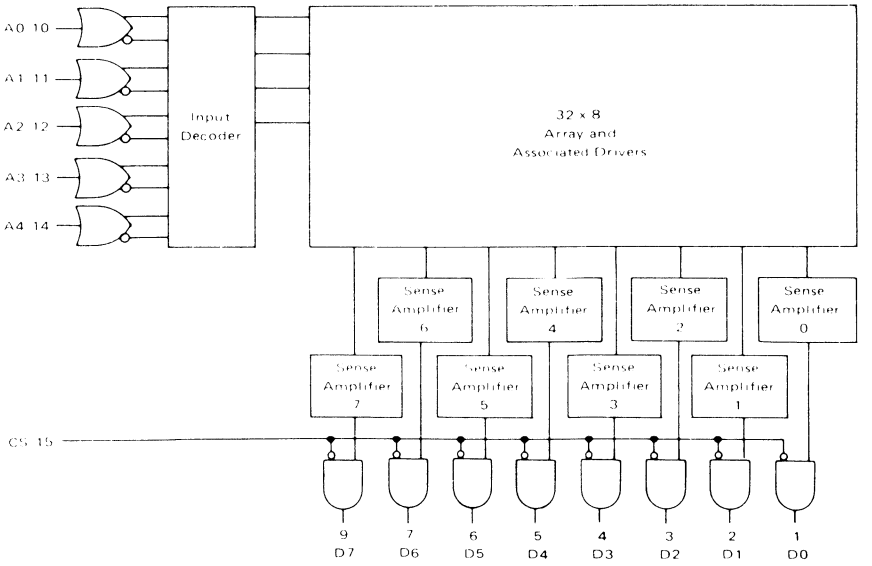


The MCM10139/10539 is a 256-bit field programmable read only memory (PROM). Prior to programming, all stored bits are at logic 0 (low) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The memory has a single negative logic chip enable. When the chip is disabled ($\overline{CS}$ = high), all outputs are forced to a logic 0 (low).

- Typical Address Access Time = 15 ns
- Typical Chip Select Access Time = 10 ns
- 50 kΩ Input Pulldown Resistors on all inputs
- Power Dissipation (520 mW typ @ 25°C) Decreases with Increasing Temperature

3bis

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		-0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	160	–	150	–	145	–	140	–	160	mAdc
Input Current High	I_{inH}	–	450	–	265	–	265	–	265	–	265	μAdc
Logic "0" Output Voltage	V_{OL}											Vdc
MCM10139		–	–	-2.010	-1.665	-1.990	-1.650	-1.970	-1.625	–	–	
MCM10539		-2.060	-1.655	–	–	-1.990	-1.620	–	–	-1.960	-1.545	

3bis

SWITCHING CHARACTERISTICS (Note 1)

Characteristic	Symbol	MCM10139 (V_{EE} = -5.2 Vdc ±5%; T_A = 0°C to +75°C)	MCM10539 (V_{EE} = -5.2 Vdc ± 5 %; T_A = -55°C to +125°C)	Conditions
Chip Select Access Time	t_{ACS}	15 ns Max	*	Measured from 50% of input to 50% of output. See Note 2
Chip Select Recovery Time	t_{RCS}	15 ns Max	*	
Address Access Time	t_{AA}	20 ns Max	*	
Rise and Fall Time	t_r, t_f	3.0 ns Typ	*	Measured between 20% and 80% points.
Input Capacitance	C_{in}	5.0 pF Max	*	Measured with a pulse technique.
Output Capacitance	C_{out}	8.0 pF Max	*	

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10139, 100 Ω, MCM10539. $C_L \leqslant 5.0$ pF including jig and stray capacitance. For Capacitance Loading ≤50 pF, delay should be derated by 30 ps/pF.
2. The maximum Address Access Time is guaranteed to be the Worst Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

*To be determined; contact your Motorola representative for up to date information.

RECOMMENDED PROGRAMMING PROCEDURE*

The MCM10139 is shipped with all bits at logical "0" (low). To write logical "1s", proceed as follows.

MANUAL (See Figure 1)

Step 1 Connect V_{EE} (Pin 8) to -5.2 V and V_{CC} (Pin 16) to 0.0 V. Address the word to be programmed by applying -1.2 to -0.6 volts for a logic "1" and -5.2 to -4.2 volts for a logic "0" to the appropriate address inputs.

Step 2 Raise V_{CC} (Pin 16) to +6.8 volts.

Step 3 After V_{CC} has stabilized at +6.8 volts (including any ringing which may be present on the V_{CC} line), apply a current pulse of 2.5 mA to the output pin corresponding to the bit to be programmed to a logic "1".

Step 4 Return V_{CC} to 0.0 Volts.

CAUTION

To prevent excessive chip temperature rise, V_{CC} should not be allowed to remain at +6.8 volts for more than 1 second.

Step 5 Verify that the selected bit has programmed by connecting a 460 Ω resistor to -5.2 volts and measuring the voltage at the output pin. If a logic "1" is not detected at the output, the procedure should be repeated once. During verification V_{IH} should be -1.0 to -0.6 volts.

Step 6 If verification is positive, proceed to the next bit to be programmed.

AUTOMATIC (See Figure 2)

Step 1 Connect V_{EE} (Pin 8) to -5.2 volts and V_{CC} (Pin 16) to 0.0 volts. Apply the proper address data and raise V_{CC} (Pin 16) to +6.8 volts.

Step 2 After a minimum delay of 100 μs and a maximum delay of 1.0 ms, apply a 2.5 mA current pulse to the first bit to be programmed ($0.1 \leq PW \leq 1$ ms).

Step 3 Repeat Step 2 for each bit of the selected word specified as a logic "1". (Program only one bit at a time. The delay between output programming pulses should be equal to or less than 1.0 ms.)

Step 4 After all the desired bits of the selected word have been programmed, change address data and repeat Steps 2 and 3.

NOTE: If all the maximum times listed above are maintained, the entire memory will program in less than 1 second. Therefore, it would be permissible for V_{CC} to remain at +6.8 volts during the entire programming time.

Step 5 After stepping through all address words, return V_{CC} to 0.0 volts and verify that each bit has programmed. If one or more bits have not programmed, repeat the entire procedure once. During verification V_{IH} should be -1.0 to -0.6 volts.

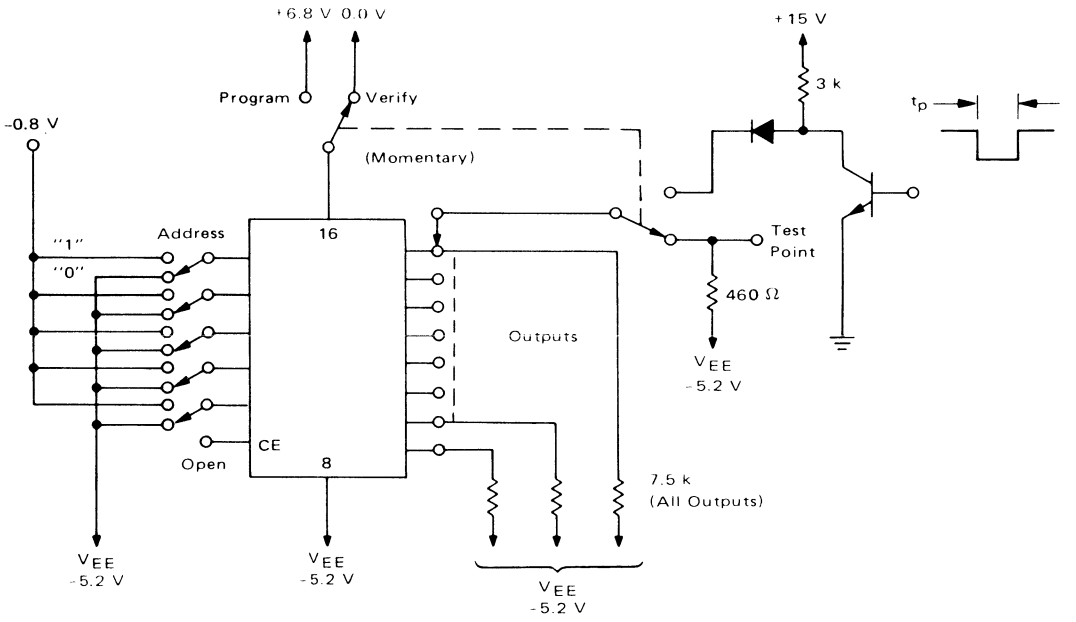
*NOTE: For devices that program incorrectly—return serialized units with individual truth tables. Noncompliance voids warranty.

PROGRAMMING SPECIFICATIONS

Characteristic	Symbol	Limits			Units	Conditions
		Min	Typ	Max		
Power Supply Voltage	V_{EE}	-5.46	-5.2	-4.94	Vdc	
To Program	V_{CCP}	+6.04	+6.8	+7.56	Vdc	
To Verify	V_{CCV}	0	0	0	Vdc	
Programming Supply Current	I_{CCP}	–	200	600	mA	V_{CC} = +6.8 Vdc
Address Voltage	V_{IH} Program	-1.2	–	-0.6	Vdc	
Logical "1"	V_{IH} Verify	-1.0	–	-0.6	Vdc	
Logical "0"	V_{IL}	-5.2	–	-4.2	Vdc	
Maximum Time at $V_{CC} = V_{CCP}$	–	–	–	1.0	sec	
Output Programming Current	I_{OP}	2.0	2.5	3.0	mAdc	
Output Program Pulse Width	t_p	0.5	–	1.0	ms	
Output Pulse Rise Time	–	–	–	10	μs	
Programming Pulse Delay (1)						
Following V_{CC} change	t_d	0.1	–	1.0	ms	
Between Output Pulses	t_d1	0.01	–	1.0	ms	

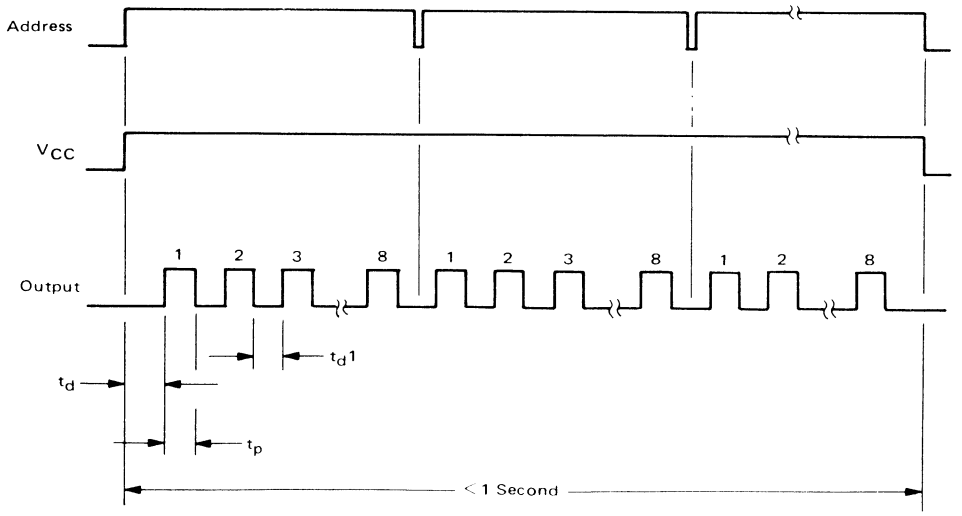
NOTE 1. Maximum is specified to minimize the amount of time V_{CC} is at +6.8 volts.

FIGURE 1 – MANUAL PROGRAMMING CIRCUIT



3bis

FIGURE 2 – AUTOMATIC PROGRAMMING CIRCUIT



8 x 2 MULTIPORT REGISTER FILE (RAM)

The MCM10143 is an 8 word by 2 bit multiport register file (RAM) capable of reading two locations and writing one location simultaneously. Two sets of eight latches are used for data storage in this LSI circuit.

WRITE

The word to be written is selected by addresses A_0–A_2. Each bit of the word has a separate write enable to allow more flexibility in system design. A write occurs on the positive transition of the clock. Data is enabled by having the write enables at a low level when the clock makes the transition. To inhibit a bit from being written, the bit enable must be at a high level when the clock goes low and not change until the clock goes high. Operation of the clock and the bit enables can be reversed. While the clock is low a positive transition of the bit enable will write that bit into the address selected by A_0–A_2.

READ

When the clock is high any two words may be read out simultaneously, as selected by addresses B_0–B_2 and C_0–C_2, including the word written during the preceding half clock cycle. When the clock goes low the addressed data is stored in the slaves. Level changes on the read address lines have no effect on the output until the clock again goes high. Read out is accomplished at any time by enabling output gates (B_0–B_1), (C_0–C_1).

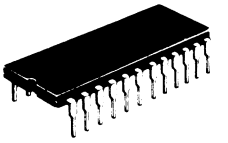
t_{pd}
- Clock to Data out = 5 ns (typ) (Read Selected)
- Address to Data out = 10 ns (typ) (Clock High)
- $\overline{\text{Read Enable}}$ to Data out = 2.8 ns (typ) (Clock high, Addresses present)

P_D 610 mW/pkg (typ no load)

TRUTH TABLE

*MODE	INPUT							OUTPUT			
	**Clock	$\overline{WE}_0$	$\overline{WE}_1$	D_0	D_1	$\overline{RE}_B$	$\overline{RE}_C$	QB_0	QB_1	QC_0	QC_1
Write	L *H	L	L	H	H	H	H	L	L	L	L
Read	H	◇	◇	◇	◇	L	L	H	H	H	H
Read	H *L	◇	◇	◇	◇	L	L	H	H	H	H
Read	L *H *L	H	H	◇	◇	L	L	H	H	H	H
Write	L *H	L	L	L	H	H	H	L	L	L	L
Read	H	◇	◇	◇	◇	L	L	L	H	L	H

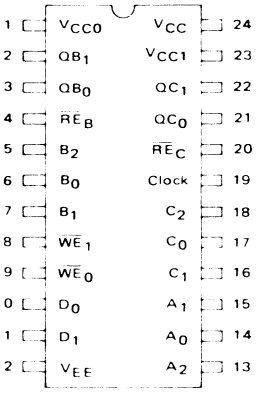
**Note Clock occurs sequentially through Truth Table
*Note A0 A2, B0 B2, and C0 C2 are all set to same address location throughout Table
◇ Don't Care



L SUFFIX
CERAMIC PACKAGE
CASE 623

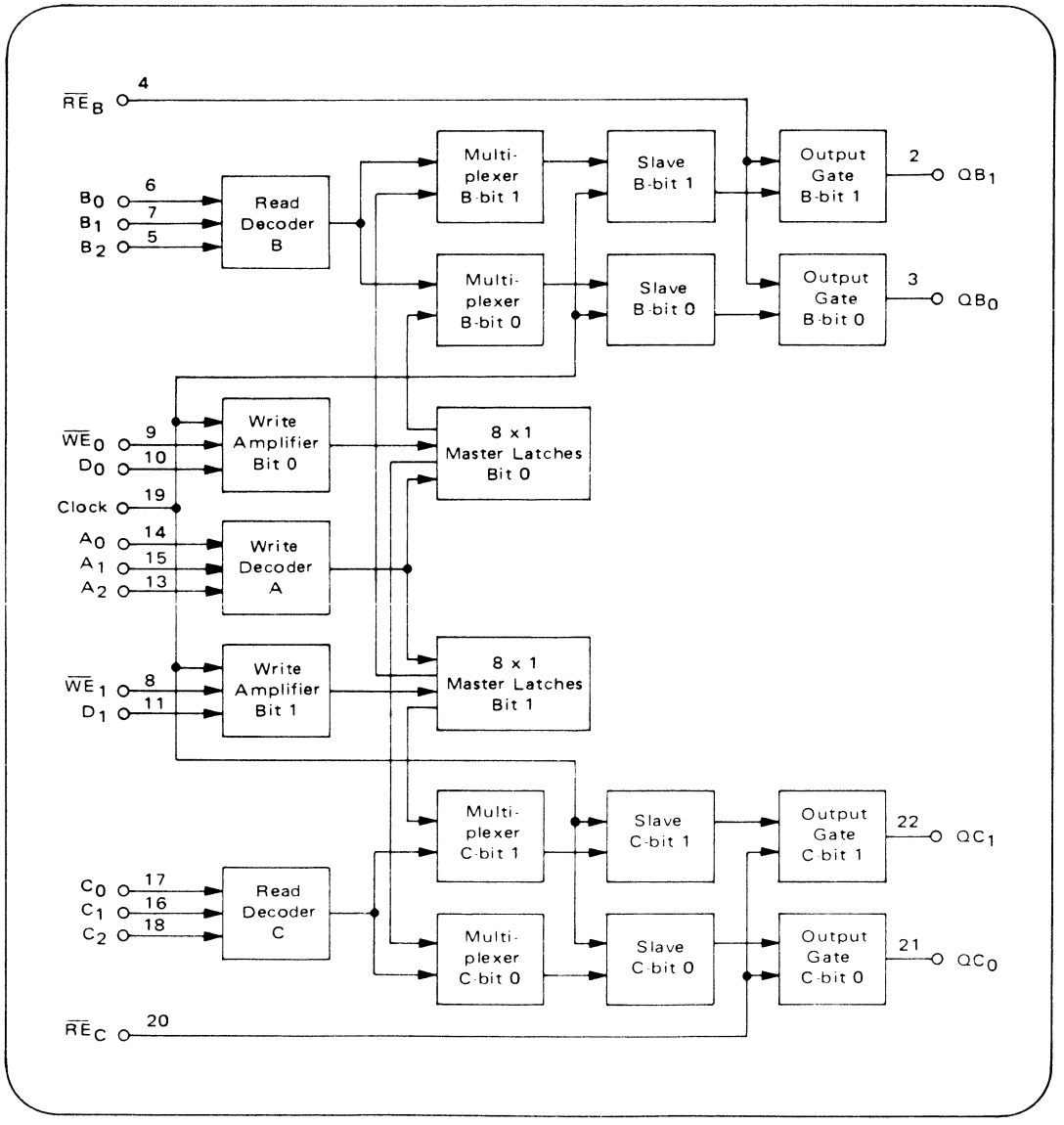
3bis

PIN ASSIGNMENT



3bis

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Characteristics	Symbol	0°C		+25°C			+75°C		Unit
		Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	—	150	—	118	150	—	150	mAdc
Input Current	I_{inH}								μAdc
Pins 10, 11, 19		—	245	—	—	245	—	245	
All other pins		—	200	—	—	200	—	200	
Switching Times ①									ns
Read Mode									
Address Input	$t_{B\pm QB\pm}$	4.0	15.3	4.5	10	14.5	4.5	15.5	
Read Enable	$t_{\overline{RE}-QB+}$	1.1	5.3	1.2	3.5	5.0	1.2	5.5	
Data	$t_{Clock+QB-}$	1.7	7.3	2.0	5.0	7.0	2.0	7.6	
Setup									
Address	$t_{setup(B-Clock-)}$	—	—	8.5	5.5	—	—	—	
Hold									
Address	$t_{hold(Clock-B+)}$	—	—	−1.5	−4.5	—	—	—	
Write Mode									
Setup									
Write Enable	$t_{setup(\overline{WE}-Clock+)}$	—	—	7.0	4.0	—	—	—	
	$t_{setup(\overline{WE}+Clock-)}$	—	—	1.0	−2.0	—	—	—	
Address	$t_{setup(A-Clock+)}$	—	—	8.0	5.0	—	—	—	
Data	$t_{setup(D-Clock+)}$	—	—	5.0	2.0	—	—	—	
Hold									
Write Enable	$t_{hold(Clock-\overline{WE}+)}$	—	—	5.5	2.5	—	—	—	
	$t_{hold(Clock+\overline{WE}-)}$	—	—	1.0	−2.0	—	—	—	
Address	$t_{hold(Clock+A+)}$	—	—	1.0	−3.0	—	—	—	
Data	$t_{hold(Clock+D+)}$	—	—	1.0	−2.0	—	—	—	
Write Pulse Width	$PW_{\overline{WE}}$	—	—	8.0	5.0	—	—	—	
Rise Time, Fall Time (20% to 80%)	t_r, t_f	1.1	4.2	1.1	2.5	4.0	1.1	4.5	

① AC timing figures do not show all the necessary presetting conditions.

READ TIMING DIAGRAMS

Access (Clock High)

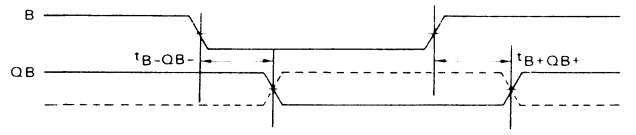


FIGURE 1

Enable

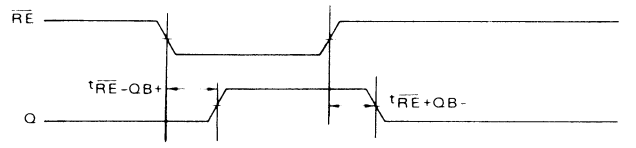


FIGURE 2

3bis

Data
(Address Selected)

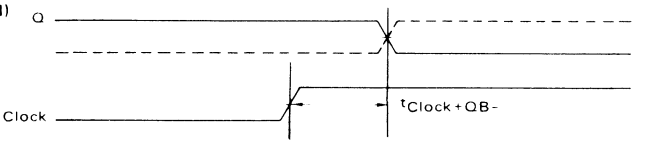


FIGURE 3

Setup and Hold

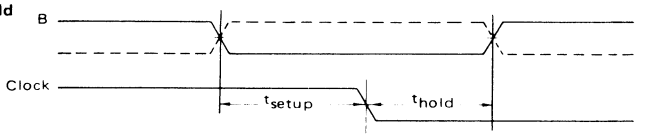


FIGURE 4

WRITE TIMING DIAGRAM

Enable Setup

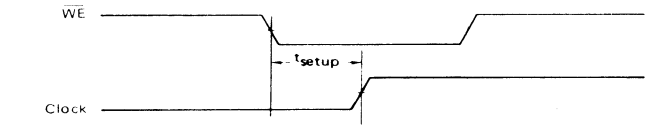


FIGURE 5

Enable Hold

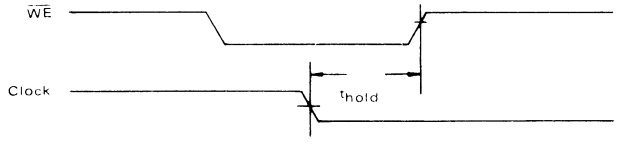


FIGURE 6

Disable

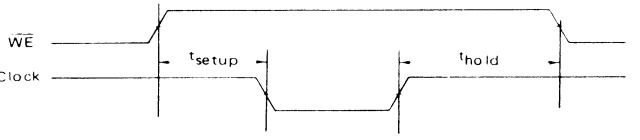


FIGURE 7

Pulse Width

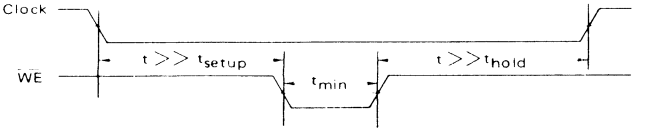


FIGURE 8

Address

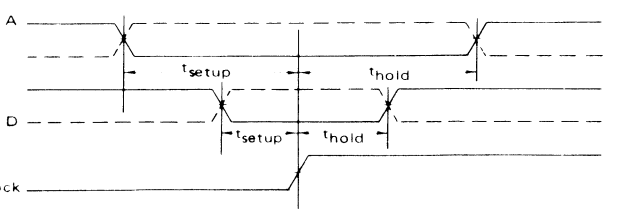
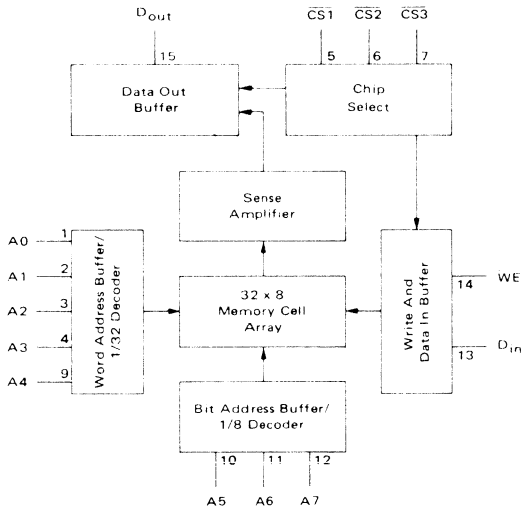


FIGURE 9

MCM10144/MCM10544

256 X 1-BIT RANDOM ACCESS MEMORY



The MCM10144/10544 is a 256 word X 1-bit RAM. Bit selection is achieved by means of an 8-bit address A0 through A7.

The active-low chip select allows memory expansion up to 2048 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

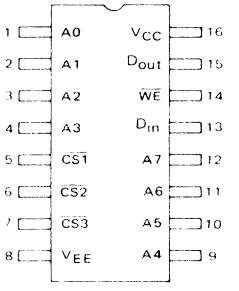
- Typical Address Access Time = 17 ns
- Typical Chip Select Access Time = 4.0 ns
- 50 kΩ Input Pulldown Resistors on Chip Select
- Power Dissipation (470 mW typ @ 25°C) Decreases with Increasing Temperature
- Pin-for-Pin Replacement for F10410

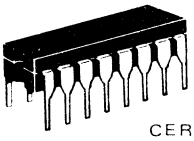
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

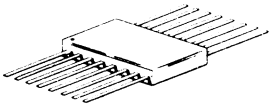
*$\overline{CS} = \overline{CS1} + \overline{CS2} + \overline{CS3}$ ϕ = Don't Care

PIN ASSIGNMENT





L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	140	–	135	–	130	–	125	–	125	mAdc
Input Current High	I_{inH}	–	375	–	220	–	220	–	220	–	220	μAdc

−55°C and +125°C test values apply to MC105xx devices only.

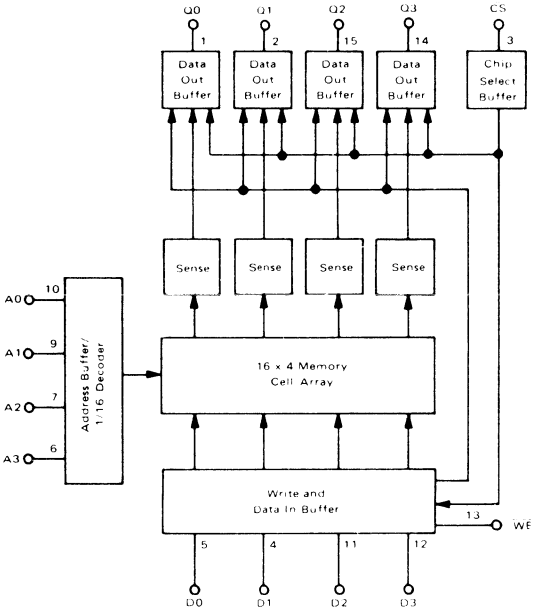
SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10144 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ± 5%		MCM10544 T_A = −55 to +125°C, V_{EE} = −5.2 Vdc ± 5%		Unit	Conditions
		Min	Max	Min	Max		
Read Mode						ns	Measured from 50% of input to 50% of output. See Note 2.
Chip Select Access Time	t_{ACS}	2.0	10	2.0	10		
Chip Select Recovery Time	t_{RCS}	2.0	10	2.0	10		
Address Access Time	t_{AA}	7.0	26	7.0	26		
Write Mode						ns	t_{WSA} = 8.0 ns
Write Pulse Width	t_W	25	–	25	–		Measured at 50% of input to 50% of output. t_W = 25 ns.
Data Setup Time Prior to Write	t_{WSD}	2.0	–	2.0	–		
Data Hold Time After Write	t_{WHD}	2.0	–	2.0	–		
Address Setup Time Prior to Write	t_{WSA}	8.0	–	8.0	–		
Address Hold Time After Write	t_{WHA}	0.0	–	0.0	–		
Chip Select Setup Time Prior to Write	t_{WSCS}	2.0	–	2.0	–		
Chip Select Hold Time After Write	t_{WHCS}	2.0	–	2.0	–		
Write Disable Time	t_{WS}	2.5	10	2.5	10		
Write Recovery Time	t_{WR}	2.5	10	2.5	10		
Rise and Fall Time	t_r, t_f					ns	Measured between 20% and 80% points.
Address to Output		1.5	7.0	1.5	7.0		
$\overline{CS}$ or $\overline{WE}$ to Output		1.5	5.0	1.5	5.0		
Capacitance						pF	Measured with a pulse technique.
Input Capacitance	C_{in}	–	5.0	–	5.0		
Output Capacitance	C_{out}	–	8.0	–	8.0		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10144; 100 Ω, MCM10544. $C_L \leq$ 5.0 pF (including jig and stray capacitance). Delay should be derated 30 ps/pF for capacitive load up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

MCM10145/MCM10545

16 X 4-BIT REGISTER FILE (RAM)



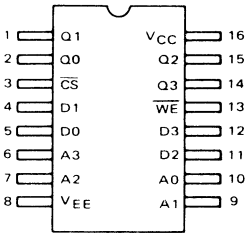
The MCM10145/10545 is a 16 word X 4-bit RAM. Bit selection is achieved by means of a 4-bit address A0 through A3.

The active-low chip select allows memory expansion up to 32 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_n is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at Q_n.

- Typical Address Access Time = 10 ns
- Typical Chip Select Access Time = 4.5 ns
- 50 kΩ Pulldown Resistors on All Inputs
- Power Dissipation (470 mW typ @ 25°C) Decreases with Increasing Temperature

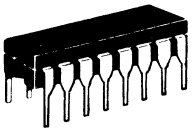
PIN ASSIGNMENT



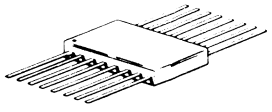
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_n	Q_n
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

ϕ = Don't Care.

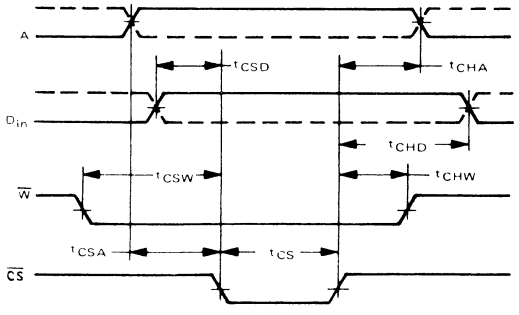


L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

FIGURE 1 – CHIP ENABLE STROBE MODE



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C Min	−55°C Max	0°C Min	0°C Max	+25°C Min	+25°C Max	+75°C Min	+75°C Max	+125°C Min	+125°C Max	Unit
Power Supply Drain Current	I_{EE}	–	135	–	130	–	125	–	120	–	120	mAdc
Input Current High	I_{inH}	–	375	–	220	–	220	–	220	–	220	μAdc

−55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10145 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ± 5% Min	MCM10145 Max	MCM10545 T_A = −55 to +125°C, V_{EE} = −5.2 Vdc ± 5% Min	MCM10545 Max	Unit	Conditions
Read Mode						ns	Measured from 50% of
Chip Select Access Time	t_{ACS}	2.0	8.0	2.0	10		input to 50% of output.
Chip Select Recovery Time	t_{RCS}	2.0	8.0	2.0	10		See Note 2.
Address Access Time	t_{AA}	4.0	15	4.0	18		
Write Mode						ns	t_{WSA} = 5 ns
Write Pulse Width	t_W	8.0	–	8.0	–		Measured at 50% of
Data Setup Time Prior to Write	t_{WSD}	0	–	0	–		input to 50% of output.
Data Hold Time After Write	t_{WHD}	3.0	–	4.0	–		t_W = 8 ns.
Address Setup Time Prior to Write	t_{WSA}	5.0	–	5.0	–		
Address Hold Time After Write	t_{WHA}	1.0	–	3.0	–		
Chip Select Setup Time Prior to Write	t_{WSCS}	0	–	5.0	–		
Chip Select Hold Time After Write	t_{WHCS}	0	–	0	–		
Write Disable Time	t_{WS}	2.0	8.0	2.0	10		
Write Recovery Time	t_{WR}	2.0	8.0	2.0	10		
Chip Enable Strobe Mode						ns	Guaranteed but not
Data Setup Prior to Chip Select	t_{CSD}	0	–	–	–		tested on standard
Write Enable Setup Prior to Chip Select	t_{CSW}	0	–	–	–		product. See Figure 1.
Address Setup Prior to Chip Select	t_{CSA}	0	–	–	–		
Data Hold Time After Chip Select	t_{CHD}	2.0	–	–	–		
Write Enable Hold Time After Chip Select	t_{CHW}	0	–	–	–		
Address Hold Time After Chip Select	t_{CHA}	4.0	–	–	–		
Chip Select Minimum Pulse Width	t_{CS}	18	–	–	–		
Rise and Fall Time	t_r, t_f					ns	Measured between 20%
Address to Output		1.5	7.0	1.5	7.0		and 80% points.
$\overline{CS}$ to Output		1.5	5.0	1.5	5.0		
Capacitance						pF	Measured with a pulse
Input Capacitance	C_{in}	–	6.0	–	6.0		technique.
Output Capacitance	C_{out}	–	8.0	–	8.0		

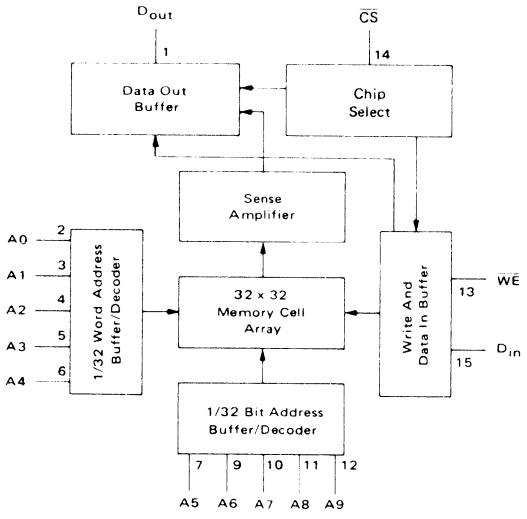
NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10145; 100 Ω, MCM10545. $C_L \leq$ 5.0 pF (including jig and Stray Capacitance). Delay should be derated 30 ps/pF for capacitive loads up to 50 pF.

2. The maximum Address Access Time is guaranteed to be the worst-case bit in the memory.

3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

MCM10146/MCM10546

1024 X 1-BIT RANDOM ACCESS MEMORY



The MCM10146/10546 is a 1024 X 1-bit RAM. Bit selection is achieved by means of a 10-bit address, A0 to A9.

The active-low chip select is provided for memory expansion up to 2048 words.

The operating mode of the RAM ($\overline{CS}$ input low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low, the chip is in the write mode, the output, D_{out}, is low and the data state present at D_{in} is stored at the selected address. With $\overline{WE}$ high, the chip is in the read mode and the data stored at the selected memory location will be presented non-inverted at D_{out}. (See Truth Table.)

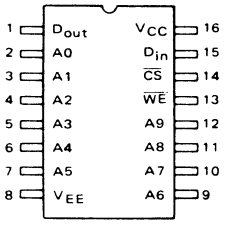
- Pin-for-Pin Compatible with the 10415
- Power Dissipation (520 mW typ @ 25°C) Decreases with Increasing Temperature
- Typical Address Access of 24 ns
- Typical Chip Select Access of 4.0 ns
- 50 kΩ Pulldown Resistor on Chip Select Input

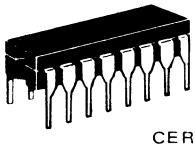
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

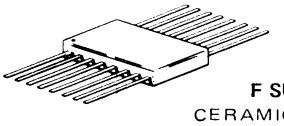
ϕ = Don't Care

PIN ASSIGNMENT





L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650-03

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	155	–	150	–	145	–	125	–	125	mAdc
Input Current High	I_{inH}	–	375	–	220	–	220	–	220	–	220	μAdc
Logic "0" Output Voltage	V_{OL}	-1.970	-1.655	-1.920	-1.665	-1.900	-1.650	-1.880	-1.625	-1.870	-1.545	Vdc

NOTE: -55°C and +125°C test values apply to MCM105XX only.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10146 T_A = 0 to +75°C, V_{EE} = -5.2 Vdc ± 5%		MCM10546 T_A = -55 to +125°C, V_{EE} = -5.2 Vdc ± 5%		Unit	Conditions
		Min	Max	Min	Max		
Read Mode						ns	Measured at 50% of input
Chip Select Access Time	t_{ACS}	2.0	7.0	2.0	8.0		to 50% of output.
Chip Select Recovery Time	t_{RCS}	2.0	7.0	2.0	8.0		See Note 2.
Address Access Time	t_{AA}	8.0	29	8.0	40		
Write Mode						ns	t_{WSA} = 8.0 ns.
Write Pulse Width (To guarantee writing)	t_W	25	–	25	–		Measured at 50% of input to 50% of output.
Data Setup Time Prior to Write	t_{WSD}	5.0	–	5.0	–		t_W = 25 ns
Data Hold Time After Write	t_{WHD}	5.0	–	5.0	–		
Address Setup Time Prior to Write	t_{WSA}	8.0	–	10	–		
Address Hold Time After Write	t_{WHA}	2.0	–	8.0	–		
Chip Select Setup Time Prior to Write	t_{WSCS}	5.0	–	5.0	–		
Chip Select Hold Time After Write	t_{WHCS}	5.0	–	5.0	–		
Write Disable Time	t_{WS}	2.8	7.0	2.8	12		
Write Recovery Time	t_{WR}	2.8	7.0	2.8	12		
Rise and Fall Time	t_r, t_f					ns	Measured between 20% and
$\overline{CS}$ or $\overline{WE}$ to Output		1.5	4.0	1.5	4.0		80% points.
Address to Output		1.5	8.0	1.5	8.0		
Capacitance						pF	Measured with a pulse
Input Capacitance	C_{in}	–	5.0	–	5.0		technique.
Output Capacitance	C_{out}	–	8.0	–	8.0		

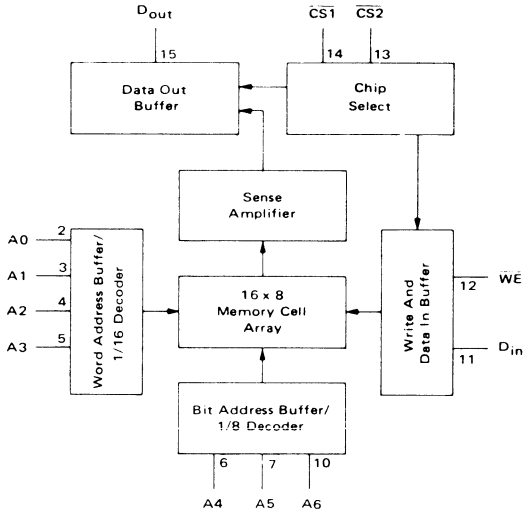
NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10146; 100 Ω, MCM10546. $C_L \leq$ 5.0 pf including jig and stray capacitance. For Capacitance Loading > 50 pF, delay should be derated by 30 ps/pF.

2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.

3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

MCM10147/MCM10547

128 X 1-BIT
RANDOM ACCESS MEMORY



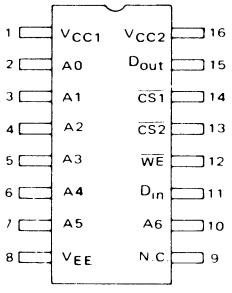
The MCM1047/10547 is a fast 128-word X 1-bit RAM. Bit selection is achieved by means of a 7-bit address, A0 through A6.

The active-low chip selects and fast chip select access time allow easy memory expansion up to 512 words without affecting system performance.

The operating mode ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

- Typical Address Access Time of 10 ns
- Typical Chip Select Access Time of 4.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (420 mW typ @ 25°C) Decreases with Increasing Temperature
- Similar to F10405

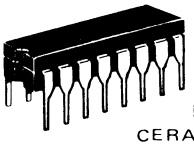
PIN ASSIGNMENT



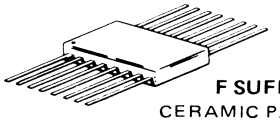
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

*$\overline{CS} = \overline{CS1} + \overline{CS2}$ ϕ = Don't Care.



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	115	–	105	–	100	–	95	–	95	mAdc
Input Current High	I_{inH}	–	375	–	220	–	220	–	220	–	220	μAdc

−55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

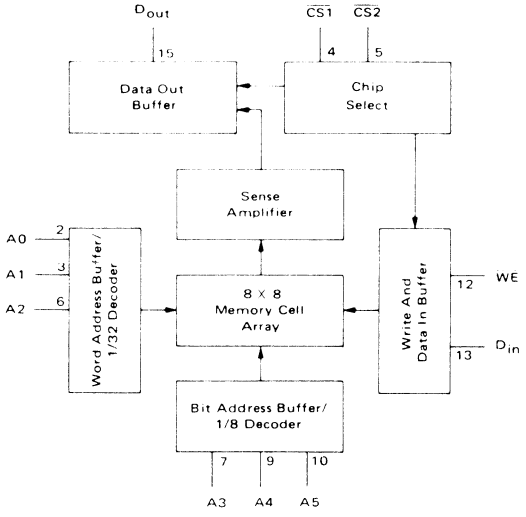
Characteristics	Symbol	MCM10147 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ±5%		MCM10547 T_A = −55 to +125°C, V_{EE} = −5.2 Vdc ±5%		Unit	Conditions
		Min	Max	Min	Max		
Read Mode						ns	Measured from 50% of
Chip Select Access Time	t_{ACS}	2.0	8.0	*	*		input to 50% of output.
Chip Select Recovery Time	t_{RCS}	2.0	8.0	*	*		See Note 2.
Address Access Time	t_{AA}	5.0	15	*	*		
Write Mode						ns	t_{WSA} = 4.0 ns
Write Pulse Width	t_W	8.0	–	*	–		Measured at 50% of input
Data Setup Time Prior to Write	t_{WSD}	1.0	–	*	–		to 50% of output.
Data Hold Time After Write	t_{WHD}	3.0	–	*	–		t_W = 8.0 ns.
Address Setup Time Prior to Write	t_{WSA}	4.0	–	*	–		
Address Hold Time After Write	t_{WHA}	3.0	–	*	–		
Chip Select Setup Time Prior to Write	t_{WSCS}	1.0	–	*	–		
Chip Select Hold Time After Write	t_{WHCS}	1.0	–	*	–		
Write Disable Time	t_{WS}	2.0	8.0	*	*		
Write Recovery Time	t_{WR}	2.0	8.0	*	*		
Rise and Fall Time	t_r, t_f	1.5	5.0	*	*	ns	Measured between 20% and 80% points.
Capacitance						pF	Measured with a pulse
Input Capacitance	C_{in}	–	5.0	–	*		technique.
Output Capacitance	C_{out}	–	8.0	–	*		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10147; 100 Ω, MCM10547.
$C_L \leq 5.0$ pF (including jig and stray capacitance).
Delay should be derated 30 ps/pF for capacitive load up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

*To be determined; contact your Motorola representative for up-to-date information.

MCM10148/MCM10548

64 X 1-BIT
RANDOM ACCESS MEMORY



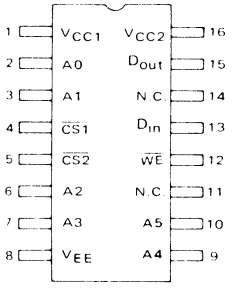
The MCM10148/10548 is a fast 64-word X 1-bit RAM. Bit selection is achieved by means of a 6-bit address, A0 through A5.

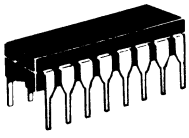
The active-low chip selects and fast chip select access time allow easy memory expansion up to 256 words without affecting system performance.

The operating mode ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

- Typical Address Access Time of 10 ns
- Typical Chip Select Access Time of 4.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (420 mW typ @ 25°C) Decreases with Increasing Temperature

PIN ASSIGNMENT



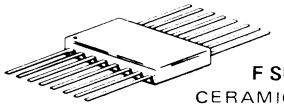


L SUFFIX
CERAMIC PACKAGE
CASE 620

TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

*$\overline{CS} = \overline{CS1} + \overline{CS2} + \overline{CS3}$ ϕ = Don't Care



F SUFFIX
CERAMIC PACKAGE
CASE 650

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	115	–	105	–	100	–	95	–	95	mAdc
Input Current High	I_{inH}	–	375	–	220	–	220	–	220	–	220	μAdc

−55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10148 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ±5%		MCM10548 T_A = −55 to +125°C, V_{EE} = −5.2 Vdc ±5%		Unit	Conditions
		Min	Max	Min	Max		
Read Mode						ns	Measured from 50% of input to 50% of output. See Note 2.
Chip Select Access Time	t_{ACS}	–	7.5	–	*		
Chip Select Recovery Time	t_{RCS}	–	7.5	–	*		
Address Access Time	t_{AA}	–	15	–	*		
Write Mode						ns	t_{WSA} = 5.0 ns Measured at 50% of input to 50% of output. t_W = 8.0 ns.
Write Pulse Width	t_W	8.0	–	*	–		
Data Setup Time Prior to Write	t_{WSD}	3.0	–	*	–		
Data Hold Time After Write	t_{WHD}	2.0	–	*	–		
Address Setup Time Prior to Write	t_{WSA}	5.0	–	*	–		
Address Hold Time After Write	t_{WHA}	3.0	–	*	–		
Chip Select Setup Time Prior to Write	t_{WSCS}	3.0	–	*	–		
Chip Select Hold Time After Write	t_{WHCS}	0	–	*	–		
Write Disable Time	t_{WS}	2.0	7.5	*	*		
Write Recovery Time	t_{WR}	2.0	7.5	*	*		
Rise and Fall Time	t_r, t_f	1.5	5.0	*	*	ns	Measured between 20% and 80% points.
Capacitance						pF	Measured with a pulse technique.
Input Capacitance	C_{in}	–	5.0	–	*		
Output Capacitance	C_{out}	–	8.0	–	*		

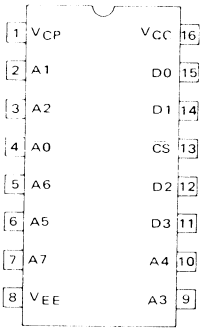
NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10148; 100 Ω, MCM10548.
C_L ≈ 5.0 pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

*To be determined; contact your Motorola representative for up-to-date information.

MCM10149/MCM10549

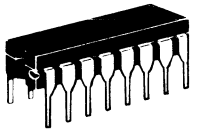
256 X 4-BIT PROGRAMMABLE READ-ONLY MEMORY

PIN ASSIGNMENT

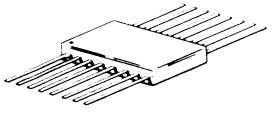


The MCM10149/10549 is a 256-word X 4-bit field programmable read only memory (PROM). Prior to programming, all stored bits are at logic 1 (high) levels. The logic state of each bit can then be changed by on-chip programming circuitry. The memory has a single negative logic chip enable. When the chip is disabled ($\overline{CS}$ = high), all outputs are forced to a logic 0 (low).

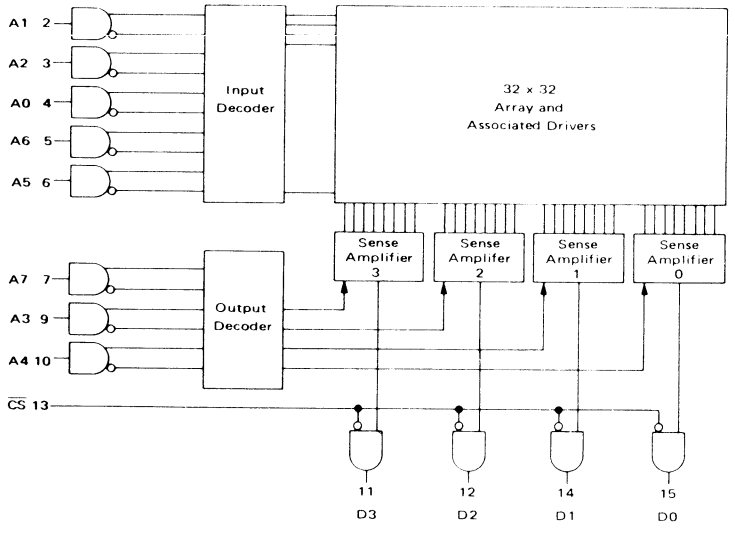
- Typical Address Access Time of 20 ns
- Typical Chip Select Access Time of 8.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (540 mW typ @ 25°C) Decreases with Increasing Temperature



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650



ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	140	–	135	–	130	–	125	–	125	mAdc
Input Current High	I_{inH}	–	450	–	265	–	265	–	265	–	265	μAdc

−55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10149 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ±5%		MCM10549 T_A = −55 to +125°C, V_{EE} = −5.2 Vdc ±5%		Unit	Conditions
		Min	Max	Min	Max		
Read Mode						ns	Measured from 50% of input to 50% of output. See Note 1.
Chip Select Access Time	t_{ACS}	2.0	10	*	*		
Chip Select Recovery Time	t_{RCS}	2.0	10	*	*		
Address Access Time	t_{AA}	7.0	25	*	*		
Rise and Fall Time	t_r, t_f	1.5	7.0	*	*	ns	Measured between 20% and 80% points.
Capacitance						pF	Measured with a pulse technique.
Input Capacitance	C_{in}	–	5.0	–	5.0		
Output Capacitance	C_{out}	–	8.0	–	8.0		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10149; 100 Ω, MCM10549.
$C_L \leq$ 5.0 pF (including jig and stray capacitance)
Delay should be derated 30 ps/pF for capacitive load up to 50 pF
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.
4. $V_{CP} = V_{CC}$ = Gnd for normal operation.

*To be determined; contact your Motorola representative for up-to-date information.

PROGRAMMING THE MCM10149 †

During programming of the MCM10149, input pins 7, 9, and 10 are addressed with standard MECL 10K logic levels. However, during programming input pins 2, 3, 4, 5, and 6 are addressed with 0 V $\leq V_{IH} \leq$ + 0.25 V and $V_{EE} \leq V_{IL} \leq$ −3.0 V. It should be stressed that this deviation from standard input levels is required only during the programming mode. During normal operation, standard MECL 10,000 input levels must be used.

With these requirements met, and with $V_{CP} = V_{CC}$ = 0 V and V_{EE} = − 5.2 V ± 5%, the address is set up. After a minimum of 100 ns delay, V_{CP} (pin 1) is ramped up to +12 V ± 0.5 V (total voltage V_{CP} to V_{EE} is now 17.2 V, +12 V − [−5.2 V]). The rise time of this V_{CP} voltage pulse should be in the 1-10 μs range, while its pulse width (t_{W1}) should be greater than 100 μs but less than 1 ms. The V_{CP} supply current at +12 V will be approximately 525 mA while current drain from V_{CC} will be approximately 175 mA. A current limit should therefore be set on both of these supplies. The current limit on the V_{CP} supply should be set at 700 mA while the V_{CC} supply should be limited to 250 mA. It should be noted that the V_{EE} supply must be capable of sinking the combined current of the V_{CC} and V_{CP} supplies while maintaining a voltage of −5.2 V ± 5%.

Coincident with, or at some delay after the V_{CP} pulse has reached its 100% level, the desired bit to be fused can be selected. This is done by taking the corresonding output pin to a voltage of +2.85 V ±5%. It is to be noted that only one bit is to be fused at a time. The other three unselected outputs should remain terminated through their 50 ohm load resistor (100 ohm for MCM10549) to −2.0 V. Current into the selected output is 5 mA maximum.

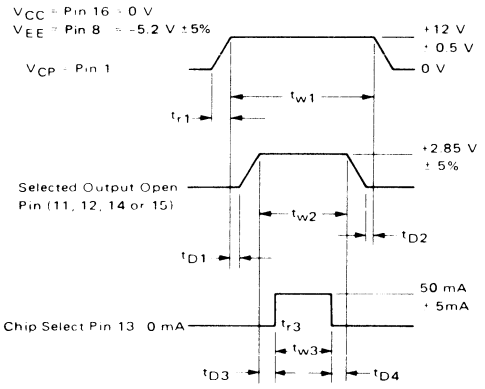
After the bit select pulse has been applied to the appropriate output, the fusing current is sourced out of the chip select pin 13. The 0% to 100% rise time of this current pulse should be 250 ns max. Its pulse width should be greater than 100 μs. Pulse magnitude is 50 mA ±5.0 mA. The voltage clamp on this current source is to be −6.0 V.

After the fusing current source has returned 0 mA, the bit select pulse is returned to it initial level, i.e., the output is returned through its load to −2.0 V. Thereafter, V_{CP} is returned to 0 V. Strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} has returned to 0 V. The remaining bits are programmed in a similar fashion.

† NOTE: For devices that program incorrectly, return serialized units with individual truth tables. Non compliance voids warranty.

PROGRAMMING SPECIFICATIONS

The following timing diagrams and fusing information represent programming specifications for the MCM10149.



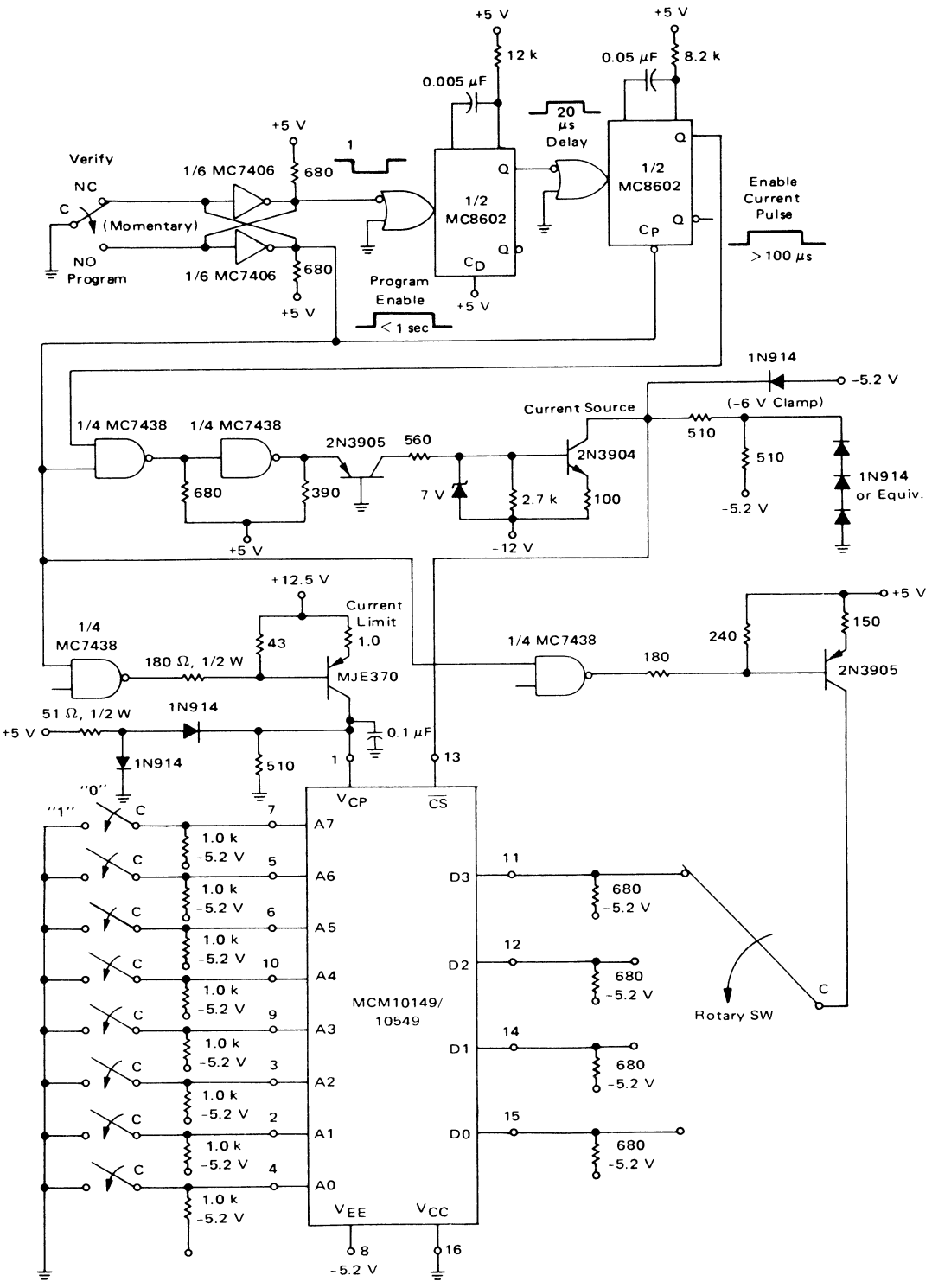
The timing diagram is shown for programming one bit. Note that only one bit is blown at a time. All addressing must be done 100 ns prior to the beginning of the V_{CP} pulse, i.e., V_{CP} = 0 V. Likewise, strobing of the outputs to determine success in programming should occur no sooner than 100 ns after V_{CP} returns to 0 V.

Note that the fusing current is defined as a positive current out of the chip select, pin 13. A programming duty cycle of $\leq$ 15% is to be observed.

Definitions and values of timing symbols are as follows.

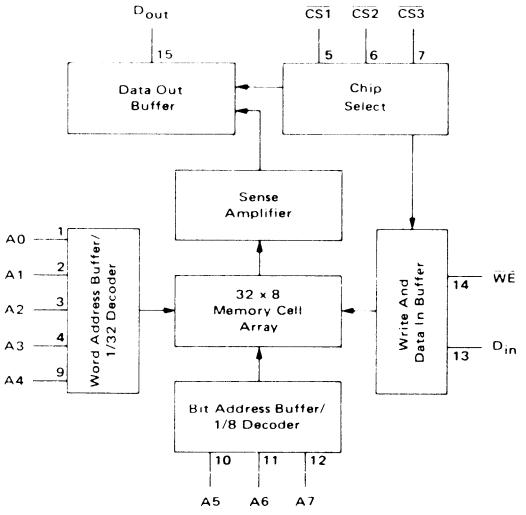
Symbol	Definition	Value
t_{r1}	Rise Time, Programming Voltage	$\geq$ 1 μs
t_{w1}	Pulse Width, Programming Voltage	$\geq$ 100 μs < 1 ms
t_{D1}	Delay Time, Programming Voltage Pulse to Bit Select Pulse	$\geq$ 0
t_{w2}	Pulse Width, Bit Select	$\geq$ 100 μs
t_{D2}	Delay Time, Bit Select Pulse to Programming Voltage Pulse	$\geq$ 0
t_{D3}	Delay Time, Bit Select Pulse to Programming Current Pulse	$\geq$ 1 μs
t_{r3}	Rise Time, Programming Current Pulse	250 ns max
t_{w3}	Pulse Width, Programming Current Pulse	$\geq$ 100 μs
t_{D4}	Delay Time, Programming Current Pulse to Bit Select Pulse	$\geq$ 1 μs

MANUAL PROGRAMMING CIRCUIT



MCM10152/MCM10552

256 X 1-BIT
RANDOM ACCESS MEMORY



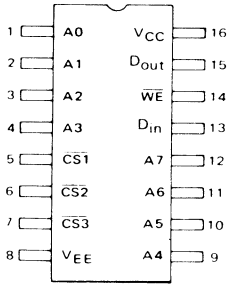
The MCM10152/10552 is a 256-word X 1-bit RAM. Bit selection is achieved by means of an 8-bit address A0 through A7.

The active-low chip select allows memory expansion up to 2048 words. The fast chip select access time allows memory expansion without affecting system performance.

The operating mode of the RAM ($\overline{CS}$ inputs low) is controlled by the $\overline{WE}$ input. With $\overline{WE}$ low the chip is in the write mode—the output is low and the data present at D_{in} is stored at the selected address. With $\overline{WE}$ high the chip is in the read mode—the data state at the selected memory location is presented non-inverted at D_{out}.

- Typical Address Access Time = 11 ns
- Typical Chip Select Access Time = 4.0 ns
- 50 kΩ Input Pulldown Resistors on All Inputs
- Power Dissipation (570 mW typ @ 25°C) Decreases with Increasing Temperature
- Pin-for-Pin Compatible with F10410/10414

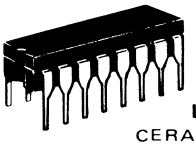
PIN ASSIGNMENT



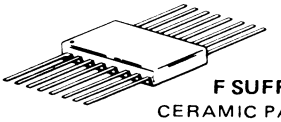
TRUTH TABLE

MODE	INPUT			OUTPUT
	$\overline{CS}$*	$\overline{WE}$	D_{in}	D_{out}
Write "0"	L	L	L	L
Write "1"	L	L	H	L
Read	L	H	ϕ	Q
Disabled	H	ϕ	ϕ	L

*$\overline{CS} = \overline{CS1} + \overline{CS2} + \overline{CS3}$ ϕ = Don't Care.



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−55°C		0°C		+25°C		+75°C		+125°C		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_{EE}	–	140	–	135	–	130	–	125	–	125	mAdc
Input Current High	I_{inH}	–	375	–	220	–	220	–	220	–	220	μAdc

−55°C and +125°C test values apply to MC105xx devices only.

SWITCHING CHARACTERISTICS (Note 1)

Characteristics	Symbol	MCM10152 T_A = 0 to +75°C, V_{EE} = −5.2 Vdc ± 5%		MCM10552 T_A = −55 to +125°C, V_{EE} = −5.2 Vdc ± 5%		Unit	Conditions
		Min	Max	Min	Max		
Read Mode							Measured from 50% of
Chip Select Access Time	t_{ACS}	2.0	7.5	*	*		input to 50% of output.
Chip Select Recovery Time	t_{RCS}	2.0	7.5	*	*		See Note 2.
Address Access Time	t_{AA}	7.0	15	*	*		
Write Mode						ns	t_{WSA} = 5.0 ns
Write Pulse Width	t_W	10	–	*	–		Measured at 50% of input
Data Setup Time Prior to Write	t_{WSD}	2.0	–	*	–		to 50% of output.
Data Hold Time After Write	t_{WHD}	2.0	–	*	–		t_W = 10 ns.
Address Setup Time Prior to Write	t_{WSA}	5.0	–	*	–		
Address Hold Time After Write	t_{WHA}	3.0	–	*	–		
Chip Select Setup Time Prior to Write	t_{WSCS}	2.0	–	*	–		
Chip Select Hold Time After Write	t_{WHCS}	2.0	–	*	–		
Write Disable Time	t_{WS}	2.5	7.5	*	*		
Write Recovery Time	t_{WR}	2.5	7.5	*	*		
Rise and Fall Time	t_r, t_f	1.5	5.0	*	*	ns	Measured between 20% and 80% points.
Capacitance						pF	Measured with a pulse
Input Capacitance	C_{in}	–	5.0	–	*		technique.
Output Capacitance	C_{out}	–	8.0	–	*		

NOTES: 1. Test circuit characteristics: R_T = 50 Ω, MCM10152; 100 Ω, MCM10552.
C_L = 5.0 pF (including jig and stray capacitance).
Delay should be derated 30 ps/pF for capacitive load up to 50 pF.
2. The maximum Address Access Time is guaranteed to be the Worst-Case Bit in the Memory.
3. For proper use of MECL Memories in a system environment, consult MECL System Design Handbook.

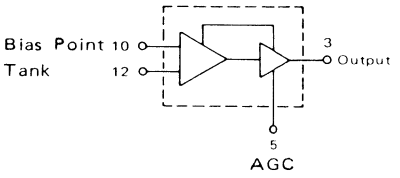
*To be determined; contact your Motorola representative for up-to-date information.

MECL III
MC1600 Series

4

MC1648/MC1648M

VOLTAGE-CONTROLLED OSCILLATOR



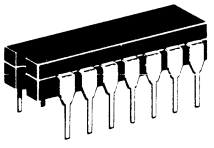
Input Capacitance = 6 pF typ
Maximum Series Resistance for L (External Inductance) = 50 Ω typ
Power Dissipation = 150 mW typ/pkg (+5.0 Vdc Supply)
Maximum Output Frequency = 225 MHz typ

The MC1648 requires an external parallel tank circuit consisting of the inductor (L) and capacitor (C).

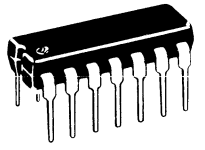
A varactor diode may be incorporated into the tank circuit to provide a voltage variable input for the oscillator (VCO). The MC1648 was designed for use in the Motorola Phase-Locked Loop shown in Figure 9. This device may also be used in many other applications requiring a fixed or variable frequency clock source of high spectral purity. (See Figure 2.)

The MC1648 may be operated from a +5.0 Vdc supply or a −5.2 Vdc supply, depending upon system requirements.

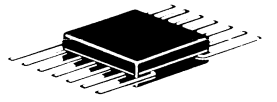
Supply Voltage	Gnd Pins	Supply Pins
+5.0 Vdc	7, 8	1, 14
−5.2 Vdc	1, 14	7, 8



L SUFFIX
CERAMIC PACKAGE
CASE 632



P SUFFIX
PLASTIC PACKAGE
CASE 646



F SUFFIX
CERAMIC PACKAGE
CASE 607

4

FIGURE 1 – CIRCUIT SCHEMATIC

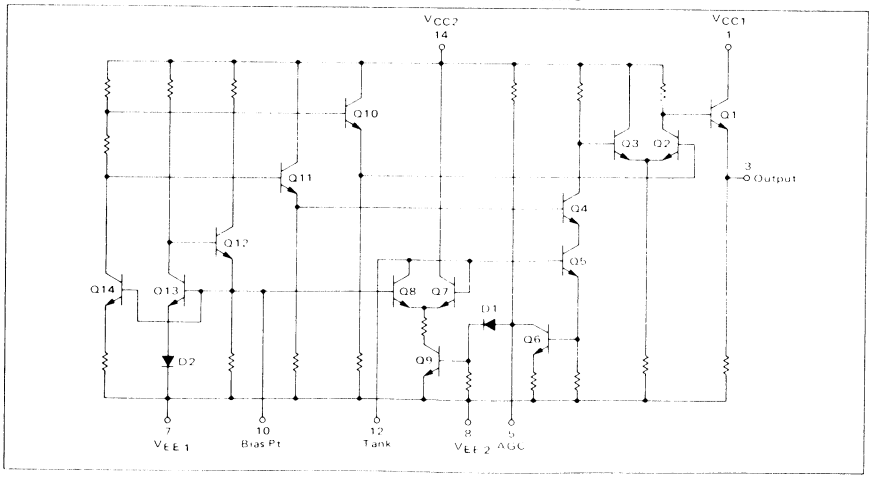
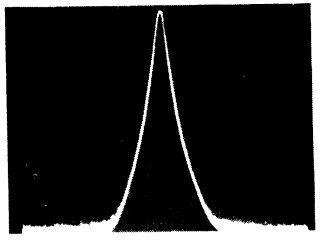
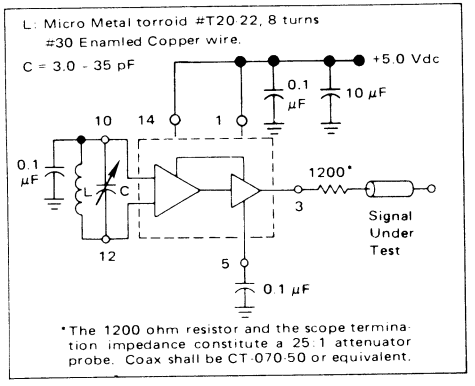


FIGURE 2 – SPECTRAL PURITY OF SIGNAL AT OUTPUT



B.W. = 10 kHz
Center Frequency = 100 MHz
Scan Width = 50 kHz/div
Vertical Scale = 10 dB/div



@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{CC}	mAdc I_L
MC1648				
-30°C	+2.00	+1.50	5.0	-5.0
+25°C	+1.85	+1.35	5.0	-5.0
+85°C	+1.70	+1.20	5.0	-5.0
MC1648M				
-55°C	+2.07	+1.57	5.0	-5.0
+25°C	+1.85	+1.35	5.0	-5.0
+125°C	+1.60	+1.10	5.0	-5.0

ELECTRICAL CHARACTERISTICS

Supply Voltage = +5.0 Volts

Characteristic	Symbol	-55°C Min	-55°C Max	-30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	+125°C Min	+125°C Max	Unit	Conditions
Power Supply Drain Current	I_E	–	–	–	–	–	41	–	–	–	–	mAdc	Inputs and outputs open.
Logic "1" Output Voltage	V_{OH}	3.92	4.13	3.955	4.185	4.04	4.25	4.11	4.36	4.16	4.40	Vdc	V_{ILmin} to Pin 12, I_L @ Pin 3.
Logic "0" Output Voltage	V_{OL}	3.13	3.38	3.16	3.40	3.20	3.43	3.22	3.475	3.23	3.51	Vdc	V_{IHmax} to Pin 12, I_L @ Pin 3.
Bias Voltage	V_{Bias}*	1.67	1.97	1.60	1.90	1.45	1.75	1.30	1.60	1.20	1.50	Vdc	V_{ILmin} to Pin 12.
		Min	Typ Max	Min	Typ Max	Min	Typ Max	Min	Typ Max	Min	Typ Max		
Peak-to-Peak Tank Voltage	V_{P-P}	–	– –	–	– –	–	400 –	–	– –	–	– –	mV	See Figure 3.
Output Duty Cycle	V_{DC}	–	– –	–	– –	–	50 –	–	– –	–	– –	%	
Oscillation Frequency	f_{max}**	–	225 –	–	225 –	200	225 –	–	225 –	–	225 –	MHz	

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor turning diode at this point.

**Frequency variation over temperature is a direct function of the $\Delta C/\Delta$ Temperature and $\Delta L/\Delta$ Temperature.

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{CC}	mAdc I_L
	MC1648			
−30°C	−3.20	−3.70	−5.2	−5.0
+25°C	−3.35	−3.85	−5.2	−5.0
+85°C	−3.50	−4.00	−5.2	−5.0
	MC1648M			
−55°C	−3.13	−3.63	−5.2	−5.0
+25°C	−3.35	−3.85	−5.2	−5.0
+125°C	−3.60	−4.10	−5.2	−5.0

ELECTRICAL CHARACTERISTICS

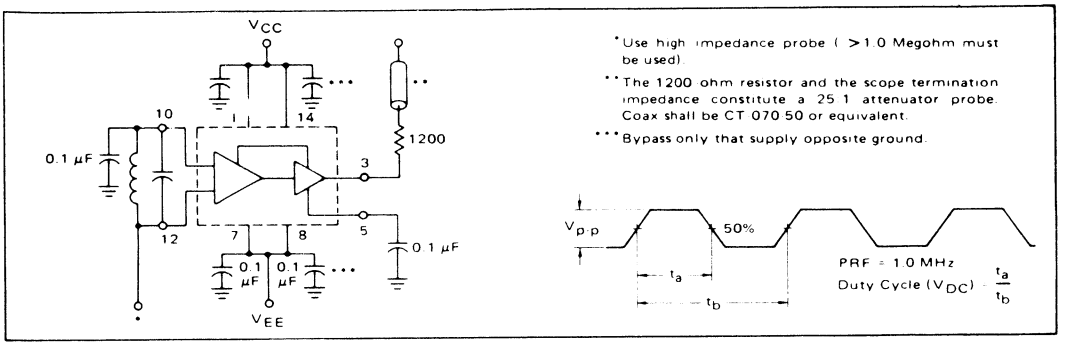
Supply Voltage = −5.2 Volts

Characteristic	Symbol	−55°C		−30°C		+25°C		+85°C		+125°C		Unit	Conditions
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Power Supply Drain Current	I_E	–	–	–	–	–	41	–	–	–	–	mAdc	Inputs and outputs open.
Logic "1" Output Voltage	V_{OH}	−1.080	−0.870	−1.045	−0.815	−0.960	−0.750	−0.890	−0.640	−0.840	−0.600	Vdc	V_{ILmin} to Pin 12, I_L @ Pin 3.
Logic "0" Output Voltage	V_{OL}	−1.920	−1.670	−1.890	−1.650	−1.850	−1.620	−1.830	−1.575	−1.820	−1.540	Vdc	V_{IHmax} to Pin 12, I_L @ Pin 3.
Bias Voltage	V_{Bias}*	−3.53	−3.23	−3.60	−3.30	−3.75	−3.45	−3.90	−3.60	−4.00	−3.70	Vdc	V_{ILmin} to Pin 12.
		Min Typ Max		Min Typ Max		Min Typ Max		Min Typ Max		Min Typ Max			
Peak-to-Peak Tank Voltage	V_{P-P}	– – –		– – –		– 400 –		– – –		– – –		mV	See Figure 3.
Output Duty Cycle	V_{DC}	– – –		– – –		– 50 –		– – –		– – –		%	
Oscillation Frequency	f_{max}**	– 225 –		– 225 –		200 225 –		– 225 –		– 225 –		MHz	

*This measurement guarantees the dc potential at the bias point for purposes of incorporating a varactor turning diode at this point.

**Frequency variation over temperature is a direct function of the ΔC/Δ Temperature and ΔL/Δ Temperature.

FIGURE 3 – TEST CIRCUIT AND WAVEFORMS



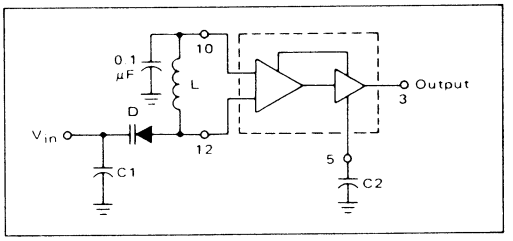
OPERATING CHARACTERISTICS

Figure 1 illustrates the circuit schematic for the MC1648. The oscillator incorporates positive feedback by coupling the base of transistor Q7 to the collector of Q8. An automatic gain control (AGC) is incorporated to limit the current through the emitter-coupled pair of transistors (Q7 and Q8) and allow optimum frequency response of the oscillator.

In order to maintain the high Q of the oscillator, and provide high spectral purity at the output, transistor Q4 is used to translate the oscillator signal to the output differential pair Q2 and Q3. Q2 and Q3, in conjunction with output transistor Q1, provides a highly buffered output which produces a square wave. Transistors Q9 and Q11 provide the bias drive for the oscillator and output buffer. Figure 2 indicates the high spectral purity of the oscillator output (pin 3).

When operating the oscillator in the voltage controlled mode (Figure 4), it should be noted that

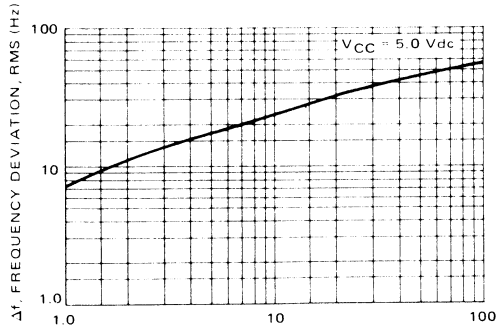
FIGURE 4 – THE MC1648 OPERATING IN THE VOLTAGE CONTROLLED MODE



the cathode of the varactor diode (D) should be biased at least 2 V_{BE} above V_{EE} ($\approx$1.4 V for positive supply operation).

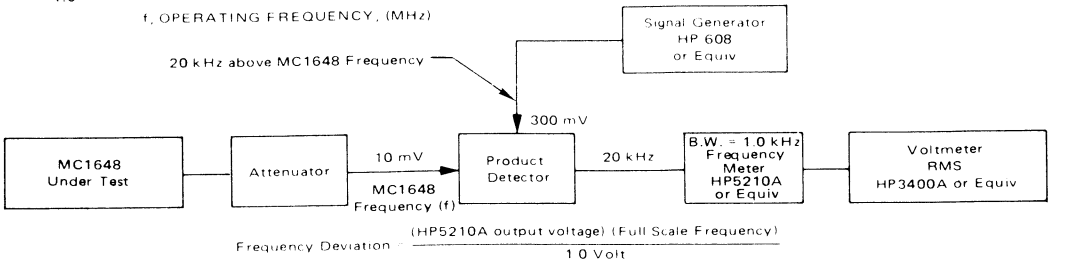
When the MC1648 is used with a constant dc voltage to the varactor diode, the output frequency will vary slightly because of internal noise. This variation is plotted versus operating frequency in Figure 5.

FIGURE 5 – NOISE DEVIATION TEST CIRCUIT AND WAVEFORM



Oscillator Tank Components
(Circuit of Figure 4)

f MHz	D	L μH
1.0-10	MV2115	100
10-60	MV2115	2.3
60-100	MV2106	0.15



$$\text{Frequency Deviation} = \frac{\text{(HP5210A output voltage) (Full Scale Frequency)}}{\text{1.0 Volt}}$$

NOTE: Any frequency deviation caused by the signal generator and MC1648 power supply should be determined and minimized prior to testing.

4

TRANSFER CHARACTERISTICS IN THE VOLTAGE CONTROLLED MODE USING EXTERNAL VARACTOR DIODE AND COIL. $T_A = 25^oC$

FIGURE 6

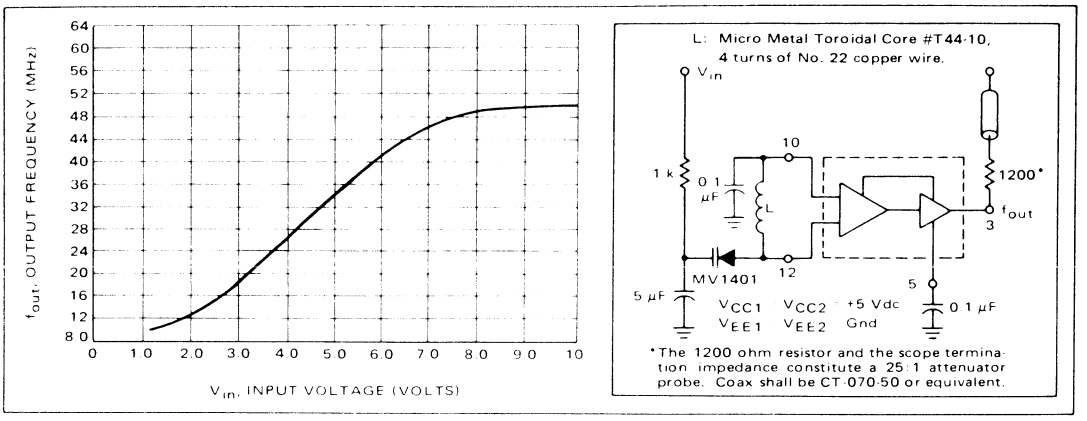


FIGURE 7

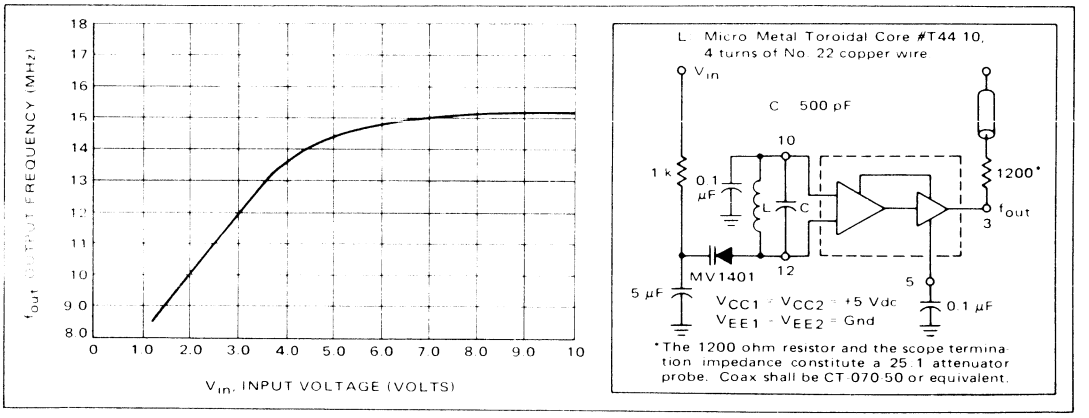
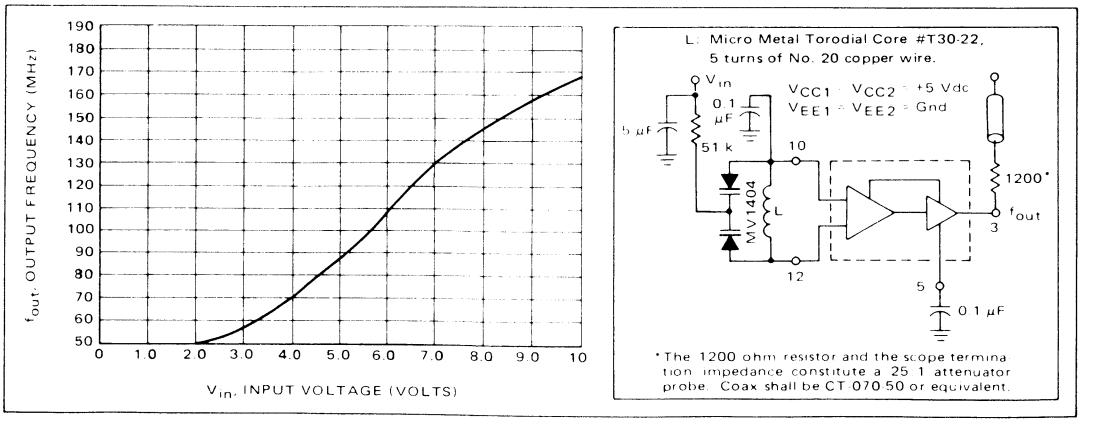


FIGURE 8



Typical transfer characteristics for the oscillator in the voltage controlled mode are shown in Figures 6, 7, and 8. Figures 6 and 8 show transfer characteristics employing only the capacitance of the varactor diode (plus the input capacitance of the oscillator, 6 pF typical). Figure 7 illustrates the oscillator operating in a voltage controlled mode with the output frequency range limited. This is achieved by adding a capacitor in parallel with the tank circuit as shown. The 1 kΩ resistor in Figures 6 and 7 is used to protect the varactor diode during testing. It is not necessary as long as the dc input voltage does not cause the diode to become forward biased. The larger-valued resistor (51 kΩ) in Figure 8 is required to provide isolation for the high-impedance junctions of the two varactor diodes.

The tuning range of the oscillator in the voltage controlled mode may be calculated as:

$$\frac{f_{max}}{f_{min}} = \frac{\sqrt{C_D(max) + C_S}}{\sqrt{C_D(min) + C_S}}$$

where $f_{min} = \frac{1}{2\pi\sqrt{L(C_D(max) + C_S)}}$

C_S = shunt capacitance (input plus external capacitance).

C_D = varactor capacitance as a function of bias voltage.

Good RF and low-frequency bypassing is necessary on the power supply pins. (See Figure 2.)

Capacitors (C1 and C2 of Figure 4) should be used to bypass the AGC point and the VCO input (varactor diode), guaranteeing only dc levels at these points.

For output frequency operation between 1 MHz and 50 MHz a 0.1 μF capacitor is sufficient for C1 and C2. At higher frequencies, smaller values of capacitance should be used; at lower frequencies, larger values of capacitance. At high frequencies the value of bypass capacitors depends directly upon the physical layout of the system. All bypassing should be as close to the package pins as possible to minimize unwanted lead inductance.

The peak-to-peak swing of the tank circuit is set internally by the AGC circuitry. Since voltage swing of the tank circuit provides the drive for the output buffer, the AGC potential directly affects the output waveform. If it is desired to have a sine wave at the output of the MC1648, a series resistor is tied from the AGC point to the most negative power potential (ground if +5.0 volt supply is used, -5.2 volts if a negative supply is used) as shown in Figure 10.

At frequencies above 100 MHz typ, it may be desirable to increase the tank circuit peak-to-peak voltage in order to shape the signal at the output of the MC1648. This is accomplished by tying a series resistor (1 kΩ minimum) from the AGC to the most positive power potential (+5.0 volts if a +5.0 volt supply is used, ground if a -5.2 volt supply is used). Figure 11 illustrates this principle.

4

APPLICATIONS INFORMATION

The phase locked loop shown in Figure 9 illustrates the use of the MC1648 as a voltage controlled oscillator. The figure illustrates a frequency synthesizer useful in tuners for FM broadcast, general aviation, maritime and landmobile communications, amateur and CB receivers. The system operates from a single +5.0 Vdc supply, and requires no internal translations, since all components are compatible.

Frequency generation of this type offers the advantages of single crystal operation, simple channel selection, and elimination of special circuitry to prevent harmonic lockup. Additional features include dc digital switching (preferable over RF switching with a multiple crystal system), and a broad range of tuning (up to 150 MHz, the range being set by the varactor diode).

The output frequency of the synthesizer loop is determined by the reference frequency and the number programmed at the programmable counter; $f_{out} = Nf_{ref}$. The channel spacing is equal to frequency (f_{ref}).

For additional information on applications and designs for phase locked loops and digital frequency synthesizers, see Motorola Application Notes AN 532A, AN 535, AN 553, AN 564 or AN594.

FIGURE 9 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION

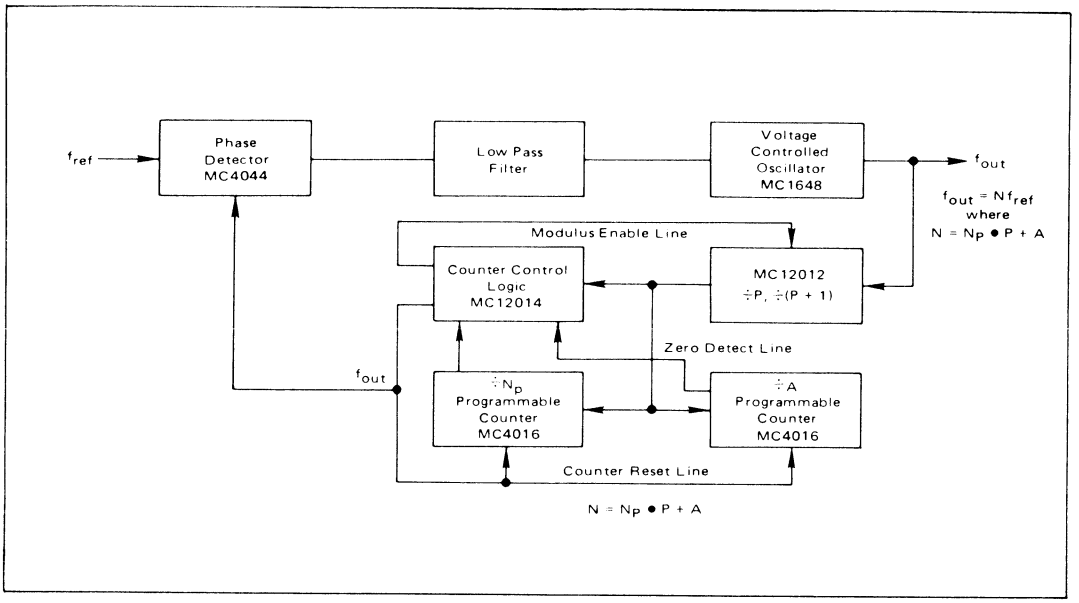


Figure 10 shows the MC1648 in the variable frequency mode operating from a +5.0 Vdc supply. To obtain a sine wave at the output, a resistor is added from the AGC circuit (pin 5) to V_{EE}.

Figure 11 shows the MC1648 in the variable frequency mode operating from a +5.0 Vdc supply. To extend the useful range of the device (maintain a square wave output above 175 MHz), a resistor is added to the AGC circuit at pin 5 (1 k-ohm minimum).

Figure 12 shows the MC1648 operating from +5.0 Vdc and +9.0 Vdc power supplies. This permits a higher voltage swing and higher output power than is possible from the MECL output (pin 3). Plots of output power versus total collector load resistance at pin 1 are given in Figures 13 and 14 for 100 MHz and 10 MHz operation. The total collector load includes R in parallel with Rp of L1 and C1 at resonance. The optimum value for R at 100 MHz is approximately 850 ohms.

FIGURE 10 – METHOD OF OBTAINING A SINE-WAVE OUTPUT

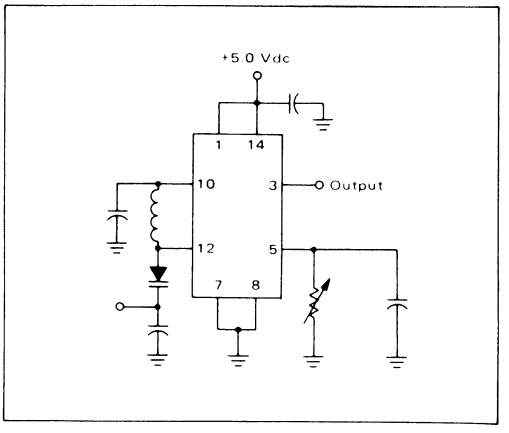


FIGURE 11 – METHOD OF EXTENDING THE USEFUL RANGE OF THE MC1648 (SQUARE WAVE OUTPUT)

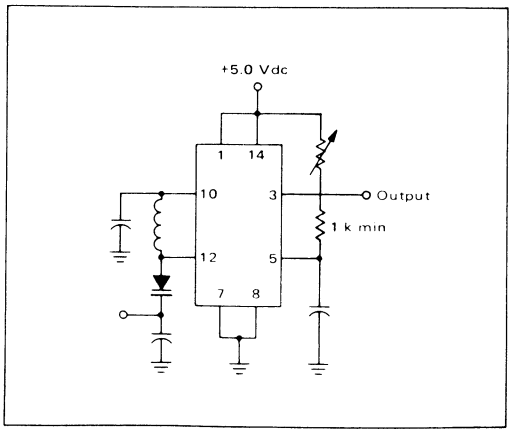


FIGURE 12 – CIRCUIT USED FOR
COLLECTOR OUTPUT OPERATION

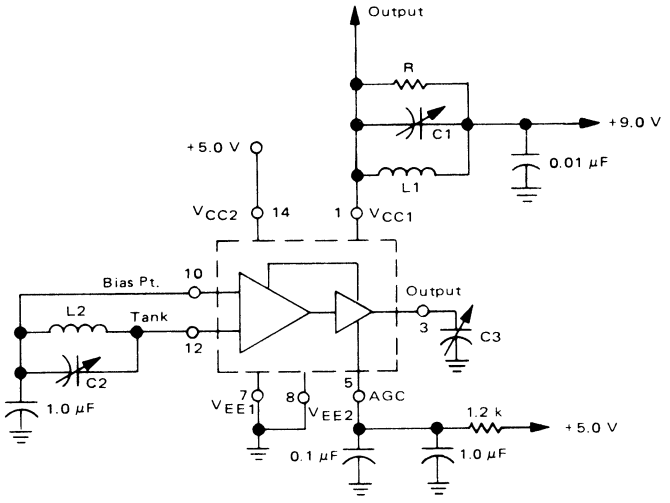


FIGURE 13 – POWER OUTPUT versus COLLECTOR LOAD

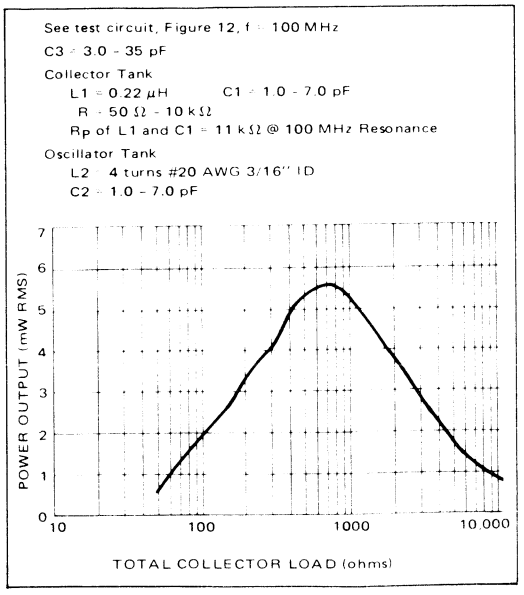
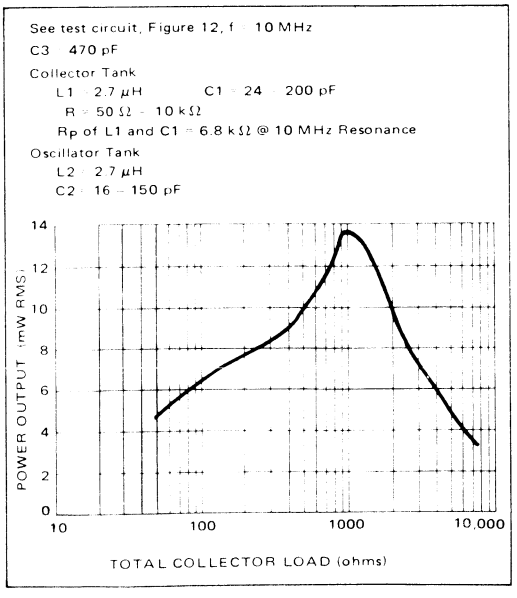
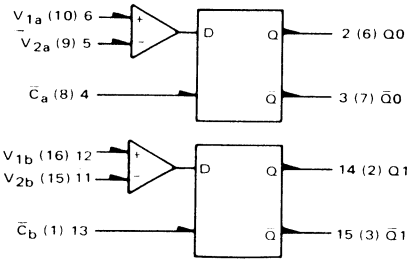


FIGURE 14 – POWER OUTPUT versus COLLECTOR LOAD



MC1650/MC1651

DUAL A/D CONVERTER



V_{CC} = +5.0 V = Pin 7,10 (11), (14)
V_{EE} = -5.2 V = Pin 8 (12)
Gnd = Pin 1,16 (4) (5)

- P_D = 330 mW typ/pkg (No Load)
- t_{pd} = 3.5 ns typ (MC1650)
  = 3.0 ns typ (MC1651)
- Input Slew Rate = 350 V/μs (MC1650)
  = 500 V/μs (MC1651)
- Differential Input Voltage:
  5.0 V (-30°C to +85°C)
- Common Mode Range:
  -3.0 V to +2.5 V (-30°C to +85°C) (MC1651)
  -2.5 V to +3.0 V (-30°C to +85°C) (MC1650)
- Resolution: ≤ 20 mV (-30°C to +85°C)
- Drives 50 Ω lines

Number at end of terminal denotes pin number for L package (Case 620).
Number in parenthesis denotes pin number for F package (Case 650).

THe MC1650 and the MC1651 are very high speed comparators utilizing differential amplifier inputs to sense analog signals above or below a reference level. An output latch provides a unique sample-hold feature. The MC1650 provides high impedance Darlington inputs, while the MC1651 is a lower impedance option, with higher input slew rate and higher speed capability.

The clock inputs ($\bar{C}_a$ and $\bar{C}_b$) operate from MECL III or MECL 10,000 digital levels. When $\bar{C}_a$ is at a logic high level, Q0 will be at a logic high level provided that $V_1 > V_2$ (V_1 is more positive than V_2). $\bar{Q}0$ is the logic complement of Q0. WHen the cock input goes to a low logic level, the outputs are latched in their present state.

Assessment of the performance differences between the MC1650 and the MC1651 may be based upon the relative behaviors shown in Figures 4 and 7.

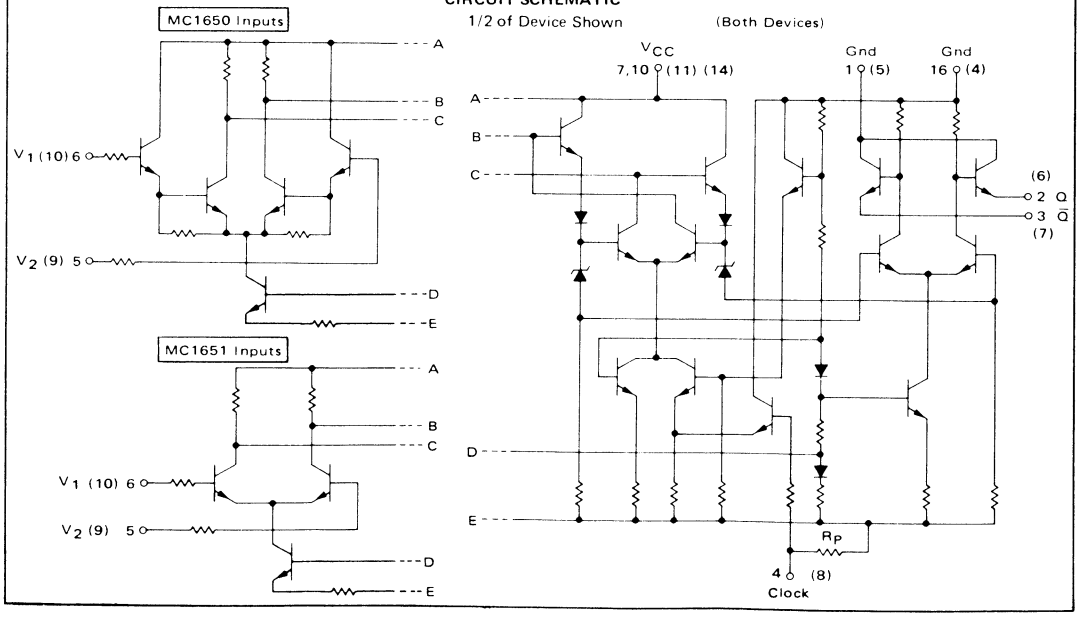
TRUTH TABLE

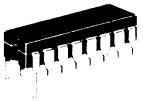
$\bar{C}$	V_1, V_2	$Q0_{n+1}$	$\bar{Q}0_{n+1}$
H	$V_1 > V_2$	H	L
H	$V_1 < V_2$	L	H
L	ϕ ϕ	$Q0_n$	$\bar{Q}0_n$

ϕ = Don't Care

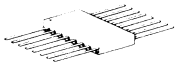
CIRCUIT SCHEMATIC

1/2 of Device Shown (Both Devices)





L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	V_{CC} ③	V_{EE} ③
-30°C	-0.875	-1.890	-1.180	-1.515	+0.020	-0.020	See Note ④				+5.0	-5.2
+25°C	-0.810	-1.850	-1.095	-1.485	+0.020	-0.020					+5.0	-5.2
+85°C	-0.700	-1.830	-1.025	-1.440	+0.020	-0.020					+5.0	-5.2

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{A1}	V_{A2}	V_{A3}	V_{A4}	V_{A5}	V_{A6}	Gnd
Power Supply Drain Current								mAdc											
Positive	I_{CC}				25*					4,13			6,12						1,5,11,16
Negative	I_E				55*				4,13				6,12						1,5,11,16
Input Current	I_{in}							µAdc											
MC1650					10				4	13			12		6				1,5,11,16
MC1651					40														
Input Leakage Current	I_R							µAdc											
MC1650					7.0				4	13			12				6		1,5,11,16
MC1651					10														
Clock Input Current	I_{inH}				350			µAdc	4	13			6,12						1,5,11,16
Logic "1" Output Voltage	V_{OH}	-1.045	-0.875	0.960	-0.810	-0.890	-0.700	Vdc	4,13				6,12						1,5,11,16
														5,11					1,6,12,16
															6,12	5,11			1,16
																	5,11	6,12	1,16
														6,12					1,5,11,16
													5,11						1,6,12,16
															5,11	6,12			1,16
																	6,12	5,11	1,16
Logic "0" Output Voltage	V_{OL}	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	4,13					6,12					1,5,11,16
													5,11						1,6,12,16
															5,11	6,12			1,16
																	6,12	5,11	1,16
													6,12						1,5,11,16
														5,11					1,6,12,16
															6,12	5,11			1,16
																	5,11	6,12	1,16
Logic "1" Threshold Voltage ②	V_{OHA}	-1.065		-0.980		-0.910		Vdc		13	4		6						1,5,16
												4			6				
											4				6				
												4	6						
Logic "0" Threshold Voltage ②	V_{OLA}		-1.630		-1.600		-1.555	Vdc		13	4		6						1,5,16
												4			6				
											4				6				
												4	6						

NOTES: ① All data is for 1/2 MC1650 or MC1651, except data marked (*) which refers to the entire package.
② These tests done in order indicated. See Figure 5.
③ Maximum Power Supply Voltages (beyond which device life may be impaired)
$|V_{EE}| + |V_{CC}| \geq 12$ Vdc

④

All Temperatures	V_{A3}	V_{A4}	V_{A5}	V_{A6}
MC1650	+3.000	+2.980	-2.500	-2.480
MC1651	+2.500	+2.480	-3.000	-2.980

@ Test Temperature	SWITCHING TEST VOLTAGE VALUES (Volts)					
	V_{R1}	V_{R2} V_{R3}	V_X	V_{XX}	V_{CC} (1)	V_{EE} (1)
-30°C	+2.000	See Note (4)	+1.040	+2.00	+7.00	-3.20
+25°C	+2.000		+1.110	+2.00	+7.00	-3.20
+85°C	+2.000		+1.190	+2.00	+7.00	-3.20

Characteristic	Symbol	-30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit	Conditions (See Figures 1-3)
Switching Times									
Propagation Delay (50% to 50%) V-Input	t_{pd}	2.0	5.0	2.0	5.0	2.0	5.7	ns	V_{R1} to V_2, V_X to Clock, P_1 to V_1, or, V_{R2} to V_2, V_X to Clock, P_2 to V_1, or, V_{R3} to V_2, V_X to Clock, P_3 to V_1.
Clock (2)		2.0	4.7	2.0	4.7	2.0	5.2		V_{R1} to V_2, P_1 to V_1 and P_4 to Clock, or, V_{R1} to V_1, P_1 to V_2 and P_4 to Clock.
Clock Enable (3)	t_{setup}	–	–	2.5	–	–	–	ns	V_{R1} to V_2, P_1 to V_1, P_4 to Clock
Clock Aperture (3)	t_{ap}	–	–	1.5	–	–	–	ns	
Rise Time (10% to 90%)	t+	1.0	3.5	1.0	3.5	1.0	3.8	ns	V_{R1} to V_2, V_X to Clock, P_1 to V_1.
Fall Time (10% to 90%)	t-	1.0	3.0	1.0	3.0	1.0	3.3	ns	

NOTES: (1) Maximum Power Supply Voltages (beyond which device life may be impaired: $|V_{CC}| + |V_{EE}| \geqslant 12$ Vdc.

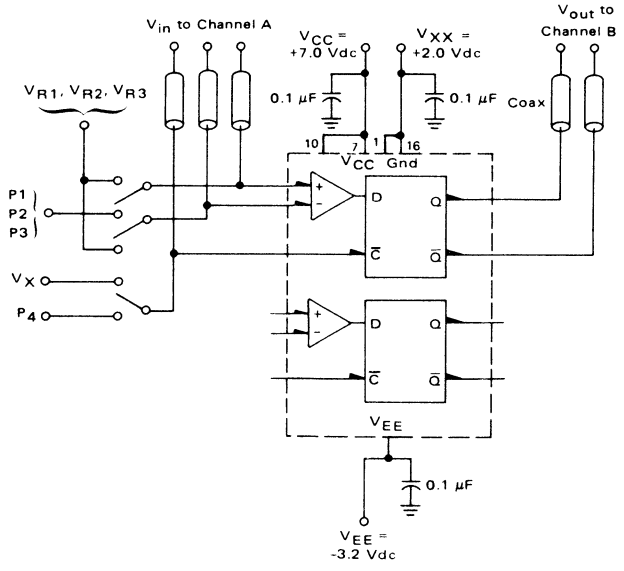
(2) Unused clock inputs may be tied to ground.

(3) See Figure 3.

(4)

All Temperatures	V_{R2}	V_{R3}
MC1650	+4.900	-0.400
MC1651	+4.400	-0.900

FIGURE 1 – SWITCHING TIME TEST CIRCUIT @ 25°C



Note: All power supply and logic levels are shown shifted 2 volts positive.

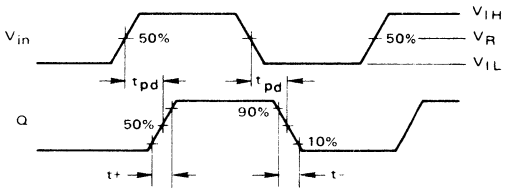
50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.

FIGURE 2 – SWITCHING AND PROPAGATION WAVEFORMS @ 25°C

The pulse levels shown are used to check ac parameters over the full common-mode range.

V – Input to Output

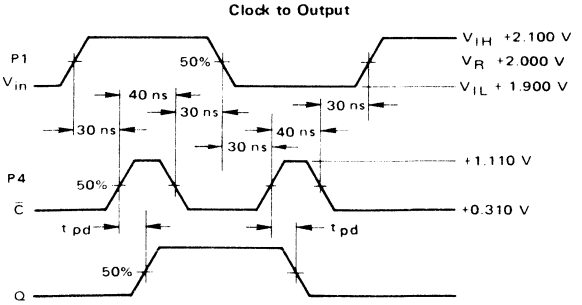


Test pulses: t_+, t_- = 1.5 ±0.2 ns (10% to 90%)
f = 5.0 MHz
50% Duty Cycle

TEST PULSE LEVELS

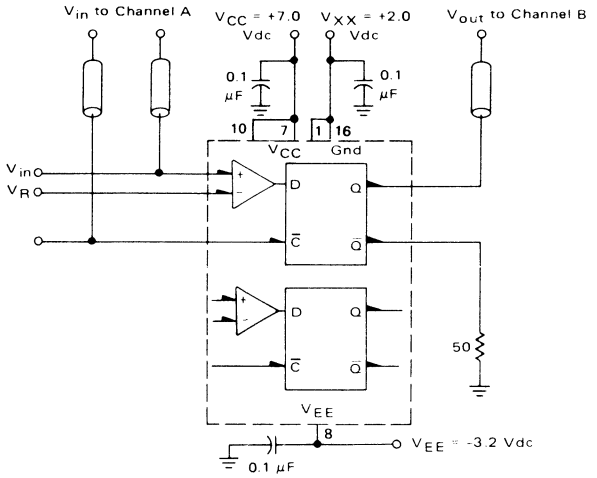
	P1		P2		P3	
	MC1650	MC1651	MC1650	MC1651	MC1650	MC1651
V_{IH}	+2.100 V	+2.100 V	+5.000 V	+4.500 V	-0.300 V	-0.800 V
V_R	+2.000 V	+2.000 V	+4.900 V	+4.400 V	-0.400 V	-0.900 V
V_{IL}	+1.900 V	+1.900 V	+4.800 V	+4.300 V	-0.500 V	-1.000 V

Clock to Output



P4: t_+, t_- = 1.5 ± 0.2 ns.

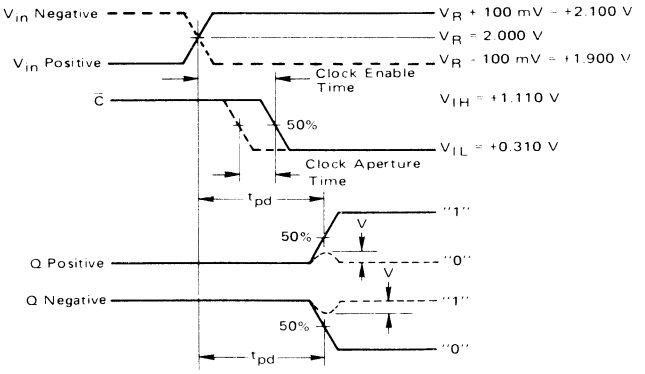
FIGURE 3 – CLOCK ENABLE AND APERTURE TIME TEST CIRCUIT AND WAVEFORMS @ 25°C



50 ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable.

Analog Signal Positive and Negative Slew Case

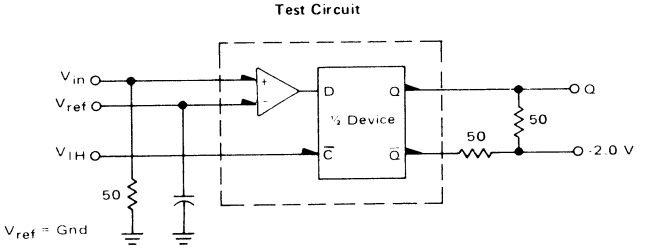


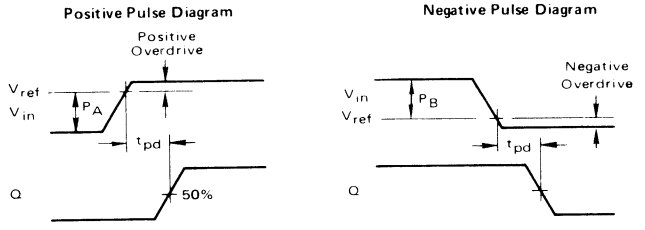
——— Clock enable time = minimum time between analog and clock signal such that output switches, and t_{pd} (analog to Q) is not degraded by more than 200 ps.

– – – – – – Clock aperture time = time difference between clock enable time and time that output does not switch and V is less than 150 mV.

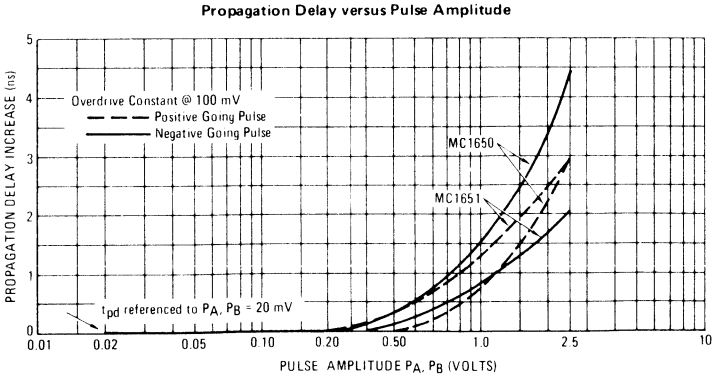
Note: All power supply and logic levels are shown shifted 2 volts positive.

FIGURE 4 – PROPAGATION DELAY (t_{pd}) versus INPUT PULSE AMPLITUDE AND CONSTANT OVERDRIVE





Input switching time is constant at 1.5 ns (10% to 90%).



(continued)

FIGURE 4 (continued)

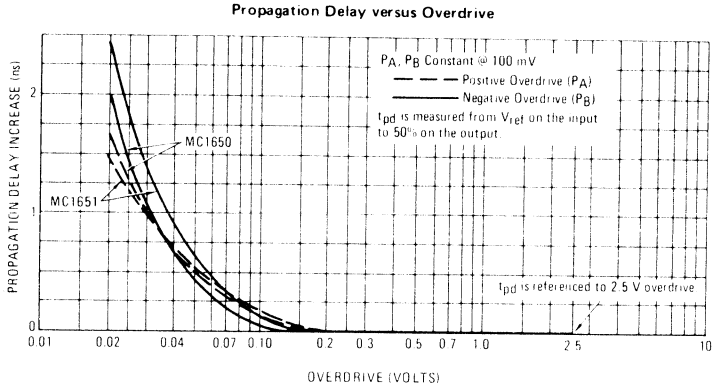


FIGURE 5 – LOGIC THRESHOLD TESTS (WAVEFORM SEQUENCE DIAGRAM)

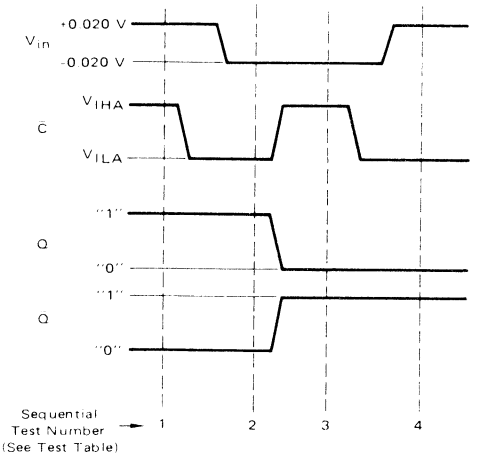
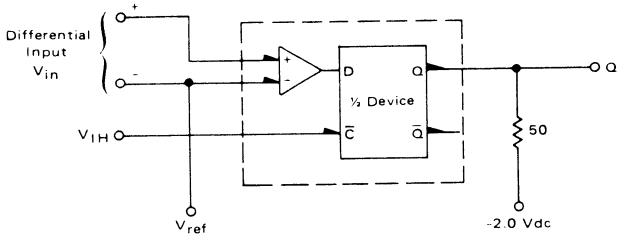


FIGURE 6 – TRANSFER CHARACTERISTICS (Q versus V_{in})

Test Configuration



$-2.5\ Vdc \leqslant V_{ref} \leqslant +2.5\ Vdc$

Typical Transfer Curves

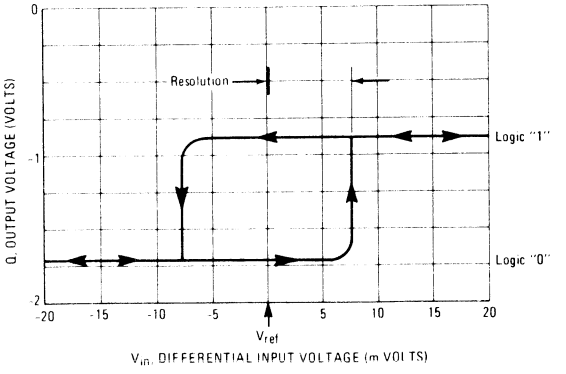
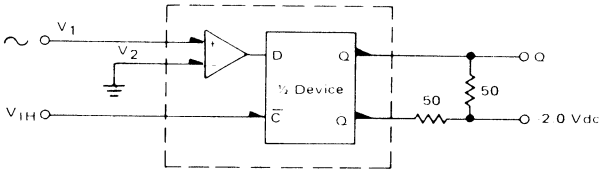
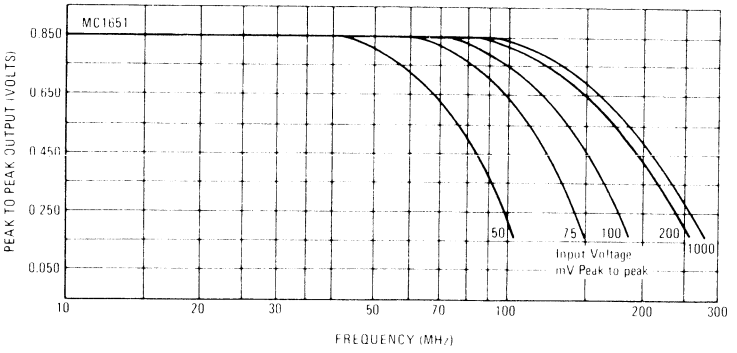


FIGURE 7 – OUTPUT VOLTAGE SWING versus FREQUENCY

(A) Test Circuit



(B) Typical Output Logic Swing versus Frequency



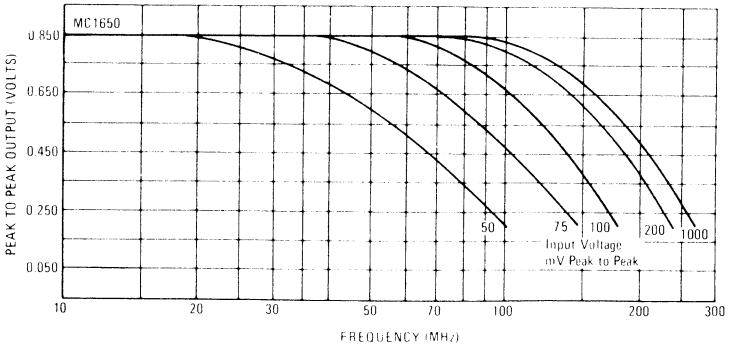
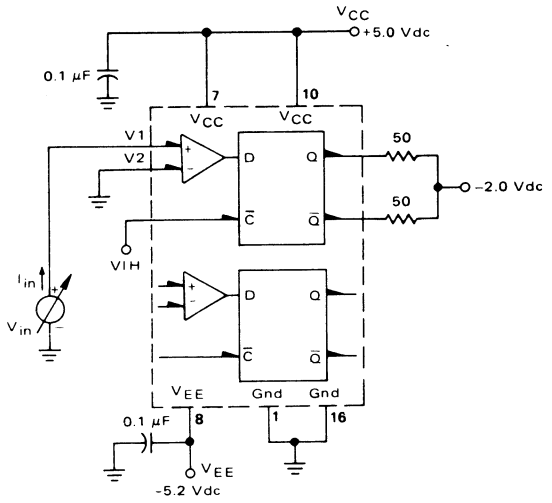
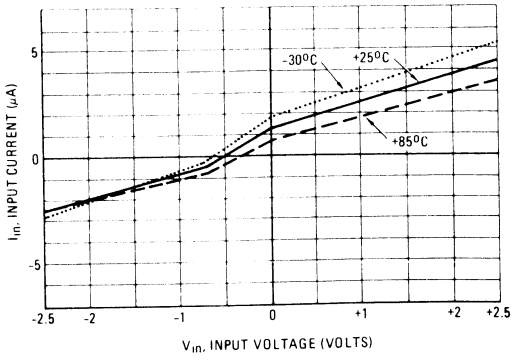


FIGURE 8 – INPUT CURRENT versus INPUT VOLTAGE

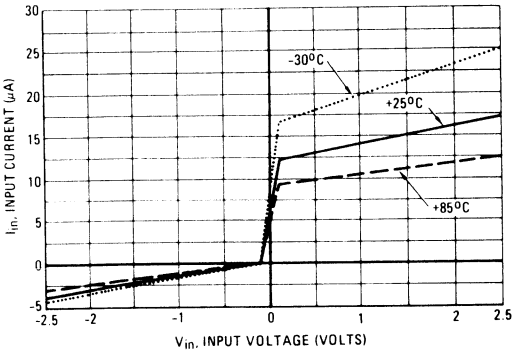
TEST CIRCUIT



Typical MC1650 (Complementary Input Grounded)



Typical MC1651 (Complementary Input Grounded)



MC1654

BINARY COUNTER

TRUTH TABLE

INPUTS							OUTPUTS			
R	S0	S1	S2	S3	C1	C2	Q0	Q1	Q2	Q3
1	0	0	0	0	ϕ	ϕ	0	0	0	0
0	1	1	1	1	ϕ	ϕ	1	1	1	1
0	0	0	0	0	1	ϕ	No Count			
0	0	0	0	0	ϕ	1	No Count			
0	0	0	0	0	··		0	0	0	0
0	0	0	0	0	··		1	0	0	0
0	0	0	0	0	··		0	1	0	0
0	0	0	0	0	··		1	1	0	0
0	0	0	0	0	··		0	0	1	0
0	0	0	0	0	··		1	0	1	0
0	0	0	0	0	··		0	1	1	0
0	0	0	0	0	··		1	1	1	0
0	0	0	0	0	··		0	0	0	1
0	0	0	0	0	··		1	0	0	1
0	0	0	0	0	··		0	1	0	1
0	0	0	0	0	··		1	1	0	1
0	0	0	0	0	··		0	0	1	1
0	0	0	0	0	··		1	0	1	1
0	0	0	0	0	··		0	1	1	1
0	0	0	0	0	··		1	1	1	1

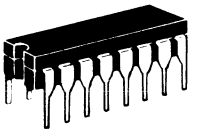
ϕ = Don't Care

·· V_{IL} → V_{IH} Clock transition from V_{IL} to V_{IH} may be applied to C1 or C2 or both for same effect.

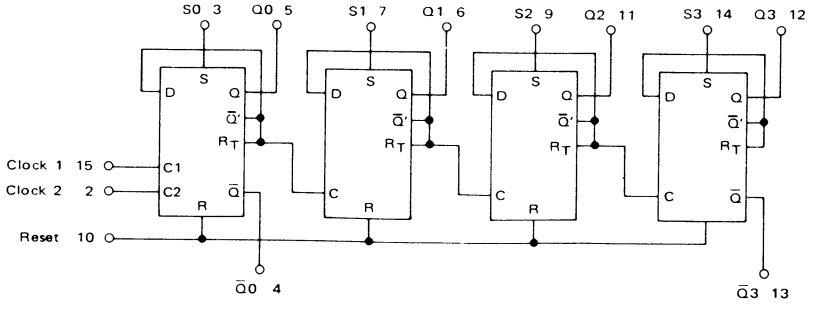
The MC1654 is a four-bit counter capable of divide-by-two, divide-by-four, divide-by-eight, or divide-by-16 functions. When used independently, the divide-by-16 section will toggle at 325 MHz typically. Clock inputs trigger on the positive-going edge of the Clock pulse.

Set and Reset inputs override the Clock, allowing asynchronous "set" or "clear." Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

Power Dissipation = 750 mW typ
f_{Tog} = 325 MHz typ



L SUFFIX
CERAMIC PACKAGE
CASE 620

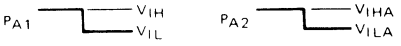


V_{CC} = 1, 16
V_{EE} = 8

ELECTRICAL CHARACTERISTICS

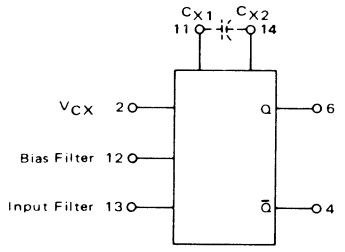
Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	–	–	200	–	–	mAdc
Input Current	I_{inH}							mAdc
Reset		–	–	–	1.00	–	–	
Set, Clock		–	–	–	0.60	–	–	
Switching Times								ns
Propagation Delay	t_{pd}							
Clock		1.0	2.9	1.0	2.7	1.0	3.1	
Set, Reset		2.0	3.9	2.0	3.7	2.0	4.1	
Rise Time (10% to 90%)	t+	1.0	2.9	1.0	2.7	1.0	3.1	ns
Fall Time (10% to 90%)	t-	1.0	2.8	1.0	2.6	1.0	3.0	ns
Maximum Toggle Frequency	f_{tog}	260	–	300	–	260	–	MHz

(1) For V_{OH}/V_{OL} testing reset all four flip-flops by applying P_{A1} to Reset and apply V_{ILmin} to Set inputs, or set all four flip-flops by applying P_{A1} simultaneously to all Set inputs and apply V_{ILmin} to Reset. For V_{OHA}/V_{OLA} testing follow the same procedure using P_{A2} and V_{ILAmax}.



MC1658

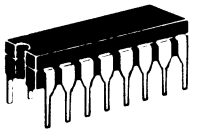
VOLTAGE-CONTROLLED MULTIVIBRATOR



V_{CC1} = Pin 1
V_{CC2} = Pin 5
V_{EE} = Pin 8

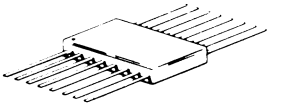
The MC1658 is a voltage-controlled multivibrator which provides appropriate level shifting to produce an output compatible with MECL III and MECL 10,000 logic levels. Frequency control is accomplished through the use of voltage-variable current sources which control the slew rate of a single external capacitor.

The bias filter may be used to help eliminate ripple on the output voltage levels at high frequencies and the input filter may be used to decouple noise from the analog input signal.



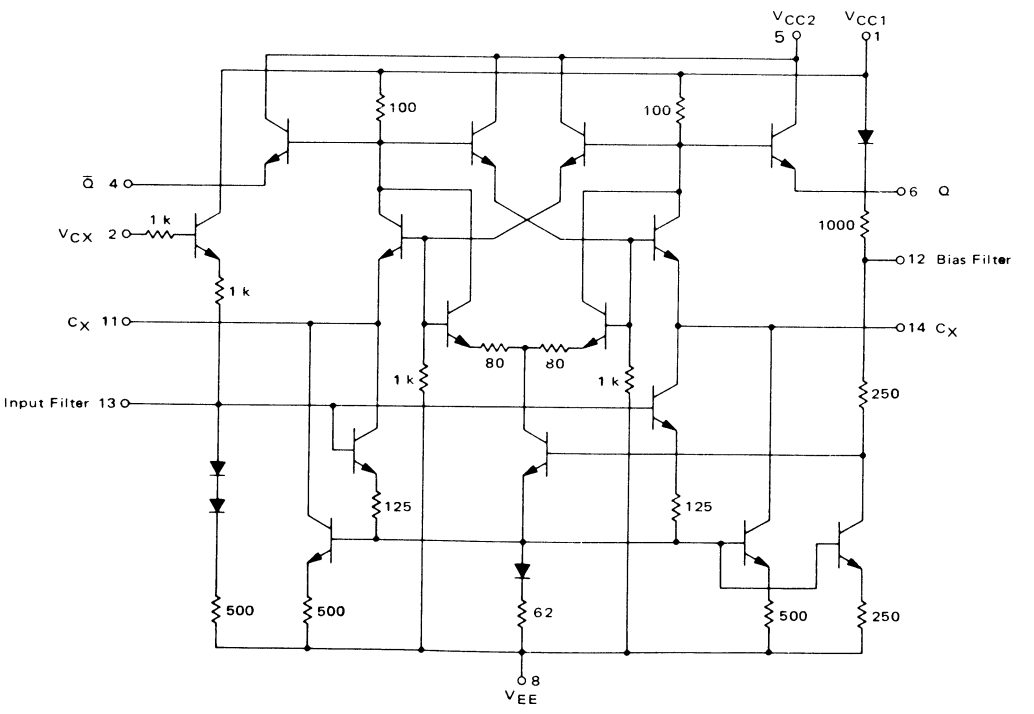
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648



F SUFFIX
CERAMIC PACKAGE
CASE 650

FIGURE 1 – CIRCUIT SCHEMATIC



@ Test Temperature	TEST VOLTAGE VALUES Vdc ±1%				
	V_{IH}	V_{IL}	V_3	V_{IHA}	V_{EE}
-30°C	0.0	-2.0	-1.0	+2.0	-5.2
+25°C	0.0	-2.0	-1.0	+2.0	-5.2
+85°C	0.0	-2.0	-1.0	+2.0	-5.2

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit	Conditions
		Min	Max	Min	Max	Min	Max		
Power Supply Drain Current	I_E	–	–	–	32	–	–	mAdc	V_{IH} to V_{CX} Limit applies for (1) or (2)
Input Current	I_{inH}	–	–	–	350	–	–	μAdc	V_{IH} to V_{CX} (1)
"Q" High Output Voltage	V_{OH}	-1.045	-0.875	-0.960	-0.810	-0.890	-0.700	Vdc	V_3 to V_{CX}. Limits apply for (1) or (2)
"$\bar{Q}$" Low Output Voltage	V_{OL}	-1.890	-1.650	-1.850	-1.620	-1.830	-1.575	Vdc	

AC CHARACTERISTICS

	Symbol	Min	Max	Min	Typ	Max	Min	Max	Unit	Conditions See Figure 2.
Rise Time (10% to 90%)	t+	–	2.7	–	1.6	2.7	–	3.0	ns	V_{IHA} to V_{CX}, CX2 (5) from pin 11 to pin 14.
Fall Time (10% to 90%)	t-	–	2.7	–	1.4	2.7	–	3.0	ns	
Oscillator Frequency	f_{osc1}	130	–	130	155	175	110	–	MHz	
	f_{osc2}	–	–	78	90	100	–	–	MHz	V_{IHA} to V_{CX}, CX1 (4) from pin 11 to pin 14.
Tuning Ration Test	TR (3)	–	–	3.1	4.5	–	–	–	–	CX1 (4) from pin 11 to pin 14.

(1) Germanium diode (0.4 drop) forward biased from 11 to 14 (11 —▶|— 14).

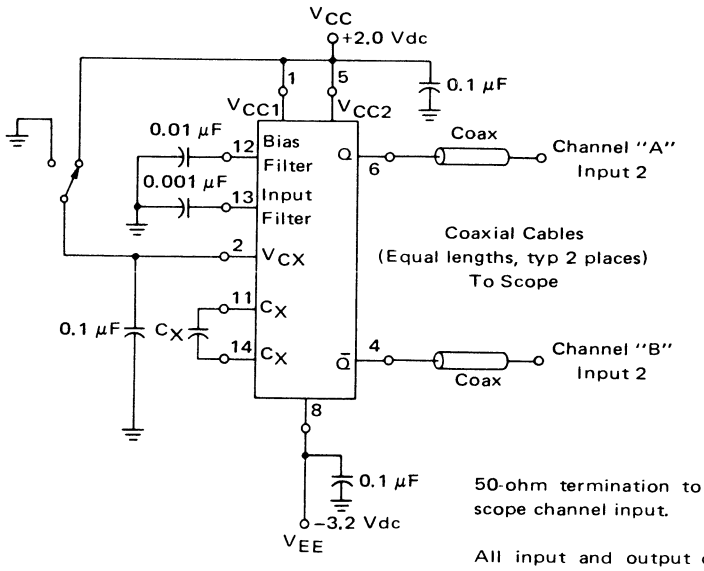
(2) Germanium diode (0.4 drop) forward biased from 14 to 11 (11 —|◀— 14).

(3) $TR = \dfrac{\text{Output frequency at } V_{CX} = \text{Gnd}}{\text{Output frequency at } V_{CX} = -2.0\ V}$

(4) C_{X1} = 10 pF connected from pin 11 to pin 14.

(5) C_{X2} = 5 pF connected from pin 11 to pin 14.

FIGURE 2 – AC TEST CIRCUIT AND WAVEFORMS



50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be $<$ 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

Note: All power supply and logic levels are shown shifted 2 volts positive.

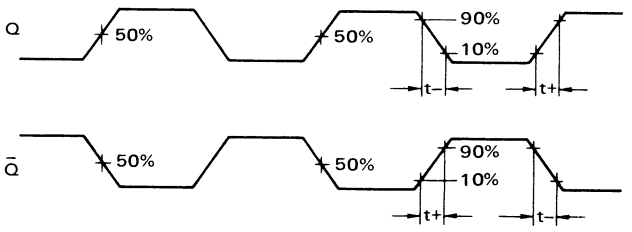


FIGURE 3 – OUTPUT FREQUENCY versus CAPACITANCE FOR VARIOUS VALUES OF INPUT VOLTAGE

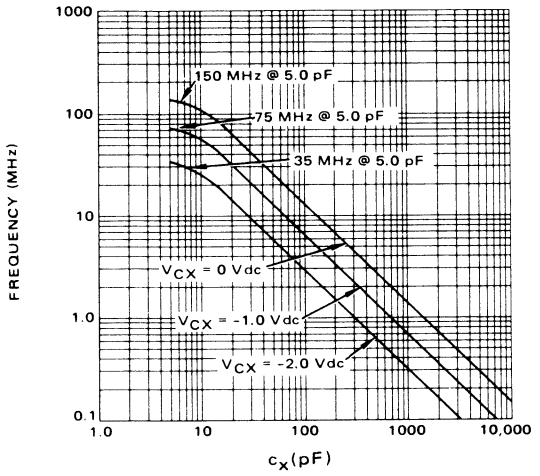


FIGURE 4 – RMS NOISE DEVIATION versus OPERATING FREQUENCY

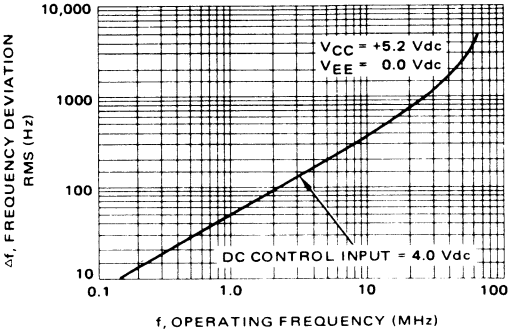
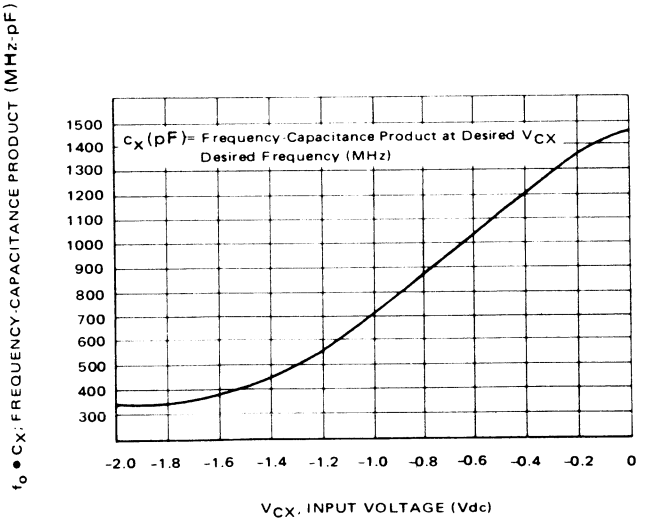
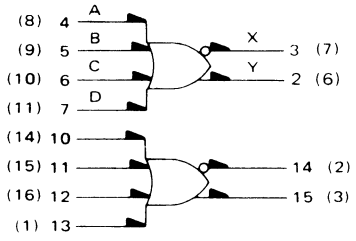


FIGURE 5 – FREQUENCY-CAPACITANCE PRODUCT versus CONTROL VOLTAGE (V_{CX})



MC1660

DUAL 4-INPUT GATE



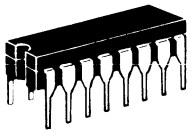
$X = \overline{A + B + C + D}$

$Y = A + B + C + D$

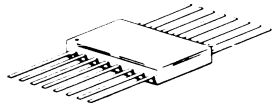
V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)

P_D = 120 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max



L SUFFIX
CERAMIC PACKAGE
CASE 620



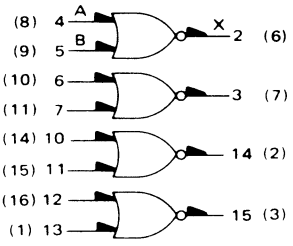
F SUFFIX
CERAMIC PACKAGE
CASE 650

Numbers at ends of terminals denote pin numbers for L package
Numbers in parenthesis denote pin numbers for F package

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	–	–	28	–	–	mAdc
Input Current	I_{inH}	–	–	–	350	–	–	μAdc
Switching Times								ns
Propagation Delay	t^{+-}	0.6	1.8	0.6	1.7	0.6	1.9	
	t^{-+}	0.6	1.6	0.6	1.5	0.6	1.7	
Rise Time, Fall Time (10% to 90%)	t^+, t^-	0.6	2.2	0.6	2.1	0.6	2.3	ns

MC1662

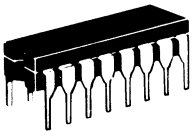
QUAD 2-INPUT NOR GATE



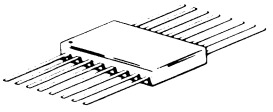
$X = \overline{A + B}$

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)
P_D = 240 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max



L SUFFIX
CERAMIC PACKAGE
CASE 620



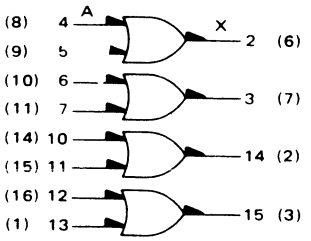
F SUFFIX
CERAMIC PACKAGE
CASE 650

Number at end of terminals denotes pin number of L package.
Number in parenthesis denotes pin number for F package.

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Max	Max	Min	Max	
Power Supply Drain Current	I_E	–	–	–	56	–	–	mAdc
Input Current	I_{inH}	–	–	–	350	–	–	μAdc
Switching Times								ns
Propagation Delay	t^{+-}	0.6	1.6	0.6	1.5	0.6	1.7	
	t^{-+}	0.6	1.8	0.6	1.7	0.6	1.9	
Rise Time, Fall Time (10% to 90%)	t^+, t^-	0.6	2.2	0.6	2.1	0.6	2.3	ns

MC1664

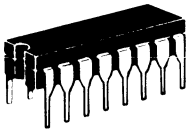
QUAD 2-INPUT OR GATE



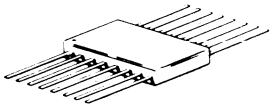
X = A + B

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)
P_D = 240 mW typ/pkg (No load)
Full Load Current, I_L = -25 mAdc max



L SUFFIX
CERAMIC PACKAGE
CASE 620



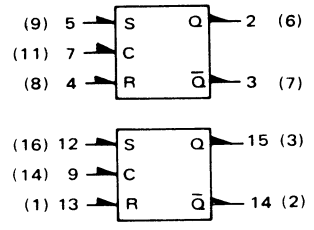
F SUFFIX
CERAMIC PACKAGE
CASE 650

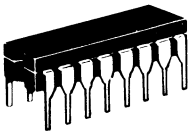
Number at end of terminals denotes pin number of L package.
Number in parenthesis denotes pin number for F package.

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	–	–	56	–	–	mAdc
Input Current	I_{inH}	–	–	–	350	–	–	μAdc
Switching Times								ns
Propagation Delay	t^{++}	0.6	1.6	0.6	1.5	0.6	1.7	
	t^{--}	0.6	1.8	0.6	1.7	0.6	1.9	
Rise Time, Fall Time (10% to 90%)	t^+,t^-	0.6	2.2	0.6	2.1	0.6	2.3	ns

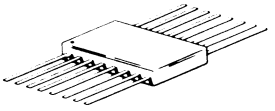
MC1666

DUAL CLOCKED R-S FLIP-FLOP





L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

TRUTH TABLE

S	R	C	Q_{n+1}
ϕ	ϕ	0	Q_n
0	0	1	Q_n
1	0	1	1
0	1	1	0
1	1	1	N.D.

ϕ = Don't Care
N.D. = Not Defined

t_{pd} = 1.6 ns typ (510-ohm load)
= 1.8 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (No Load)

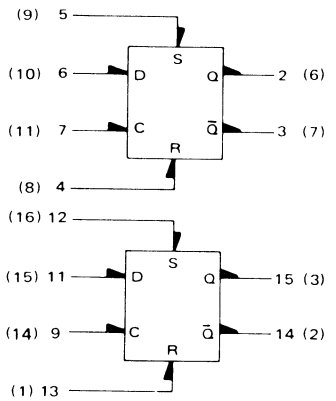
V_{CC1} = Pin 1(5)
V_{CC2} = Pin 16(4)
V_{EE} = Pin 8(12)

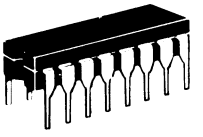
Number at end of terminal denotes pin number for L package
Number in parenthesis denotes pin number for F package

Characteristic	Symbol	−30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	–	–	55	–	–	mAdc
Input Current	I_{inH}							μAdc
Set, Reset		–	–	–	370	–	–	
Clock		–	–	–	225	–	–	
Switching Times								ns
Propagation Delay	t_{pd}							
Clock		1.0	2.7	1.0	2.5	1.1	2.8	
Set, Reset		1.0	2.5	1.1	2.3	1.1	2.7	
Rise Time (10% to 90%)	t+	0.8	2.8	0.8	2.5	0.9	2.9	ns
Fall Time (10% to 90%)	t−	0.5	2.4	0.5	2.2	0.5	2.6	ns

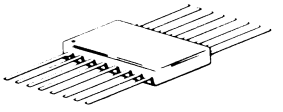
MC1668

DUAL CLOCKED LATCH





L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

TRUTH TABLE

S	R	D	C	Q_{n+1}
0	0	ϕ	0	Q_n
1	0	ϕ	0	1
0	1	ϕ	0	0
1	1	ϕ	0	**
ϕ	ϕ	0	1	0
ϕ	ϕ	1	1	1

**Output state not defined ϕ = Don't Care

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

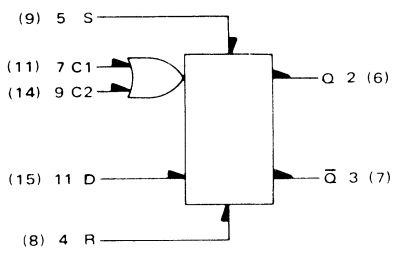
t_{pd} = 1.6 ns typ (510-ohm load)
= 1.8 ns typ (50-ohm load)
P_D = 220 mW typ/pkg (No load)

Number at end of terminal denotes pin number for L package
Number in parenthesis denotes pin number for F package

Characteristic	Symbol	−30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	–	–	55	–	–	mAdc
Input Current	I_{inH}							μAdc
Data, Set, Reset		–	–	–	370	–	–	
Clock		–	–	–	225	–	–	
Switching Times								ns
Propagation Delay	t_{pd}							
Clock		1.0	2.7	1.0	2.5	1.1	2.8	
Set, Reset		1.0	2.5	1.0	2.3	1.1	2.7	
Rise Time (10% to 90%)	t+	0.8	2.8	0.9	2.5	0.9	2.9	ns
Fall Time (10% to 90%)	t-	0.5	2.4	0.5	2.2	0.5	2.6	ns

MC1670

MASTER-SLAVE FLIP-FLOP



Master slave construction renders the MC1670 relatively insensitive to the shape of the clock waveform, since only the voltage levels at the clock inputs control the transfer of information from data input (D) to output.

When both clock inputs (C1 and C2) are in the low state, the data input affects only the "Master" portion of the flip-flop. The data present in the "Master" is transferred to the "Slave" when clock inputs (C1 "OR" C2) are taken from a low to a high level. In other words, the output state of the flip flop changes on the positive transition of the clock pulse.

While either C1 "OR" C2 is in the high state, the "Master" (and data input) is disabled.

Asynchronous Set (S) and Reset (R) override Clock (C) and Data (D) inputs.

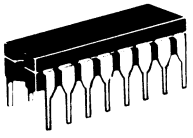
TRUTH TABLE

R	S	D	C	Q_{n+1}
L	H	ϕ	ϕ	H
H	L	ϕ	ϕ	L
H	H	ϕ	ϕ	N.D.
L	L	L	L	Q_n
L	L	L	↗	L
L	L	L	H	Q_n
L	L	H	L	Q_n
L	L	H	↗	H
L	L	H	H	Q_n

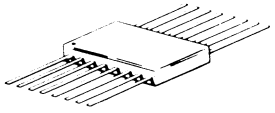
ϕ = Don't Care
ND = Not Defined
C = C1 + C2

V_{CC1} = Pin 1(5)
V_{CC2} = Pin 16(4)
V_{EE} = Pin 8(12)

Power Dissipation = 220 mW typical (No Load)
f_{Tog} = 350 MHz typ



L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

Number at end of terminal denotes pin number for L package
Number in parenthesis denotes pin number for F package

Characteristic	Symbol	-30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit
Power Supply Drain Current	I_E	–	–	–	48	–	–	mAdc
Input Current	I_{inH}							μAdc
Set, Reset		–	–	–	550	–	–	
Clock		–	–	–	250	–	–	
Data		–	–	–	270	–	–	
Switching Times								ns
Propagation Delay	t_{pd}	1.0	2.7	1.1	2.5	1.1	2.9	
Rise Time (10% to 90%)	t_+	0.9	2.7	1.0	2.5	1.0	2.9	ns
Fall Time (10% to 90%)	t_-	0.5	2.1	0.6	1.9	0.6	2.3	ns
Setup Time	$t_{S"1"}$	–	–	0.4	–	–	–	ns
	$t_{S"0"}$	–	–	0.5	–	–	–	
Hold Time	$t_{H"1"}$	–	–	0.3	–	–	–	ns
	$t_{H"0"}$	–	–	0.5	–	–	–	
Toggle Frequency	f_{Tog}	270	–	300	–	270	–	MHz

FIGURE 1 – TOGGLE FREQUENCY WAVEFORMS

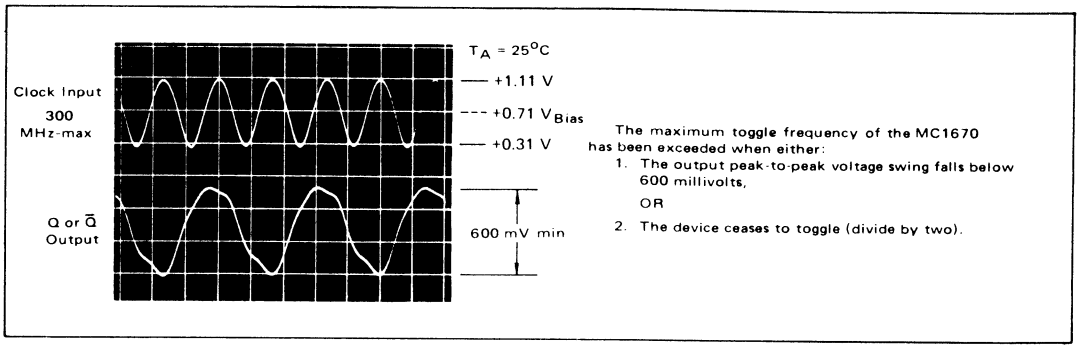


FIGURE 2 – MAXIMUM TOGGLE FREQUENCY (TYPICAL)

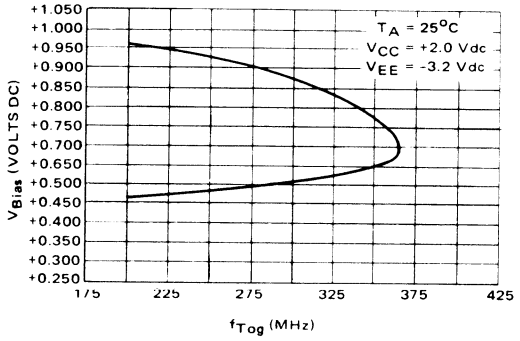
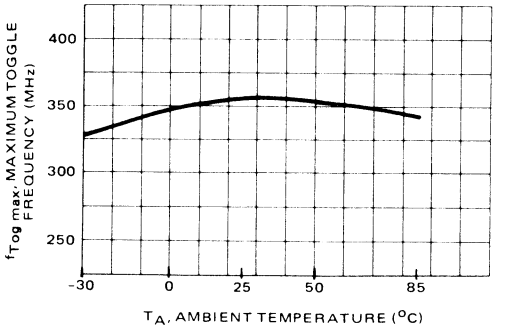


Figure 2 illustrates the variation in toggle frequency with the dc offset voltage (V_{Bias}) of the input clock signal.

Figures 4 and 5 illustrate minimum clock pulse width recommended for reliable operation of the MC1670.

FIGURE 3 – TYPICAL MAXIMUM TOGGLE FREQUENCY versus TEMPERATURE



Temperature	-30°C	+25°C	+85°C
V_{Bias}	+0.660 Vdc	+0.710 Vdc	+0.765 Vdc

Note: All power supply and logic levels are shown shifted 2 volts positive.

FIGURE 4 – MINIMUM "DOWN TIME" TO CLOCK
OUTPUT LOAD = 50Ω

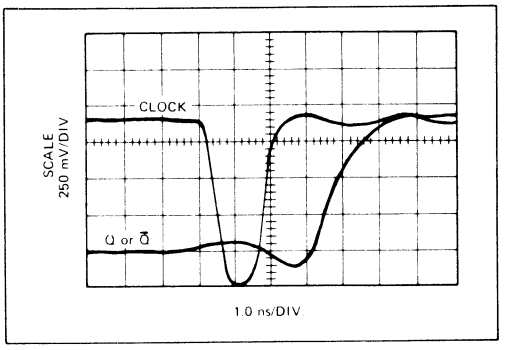
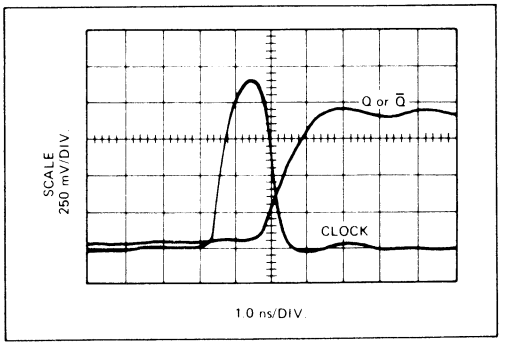
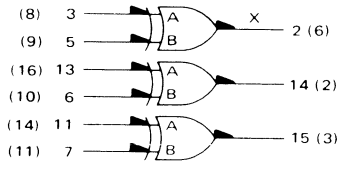


FIGURE 5 – MINIMUM "UP TIME" TO CLOCK
OUTPUT LOAD = 50Ω



MC1672

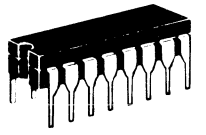
TRIPLE 2-INPUT EXCLUSIVE-OR GATE



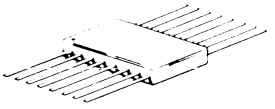
$X = A \bullet \bar{B} + \bar{A} \bullet B$

V_{CC1} = Pin 1(5)
V_{CC2} = Pin 16(4)
V_{EE} = Pin 8(12)

t_{pd} = 1.1 ns typ (510 ohm load)
= 1.3 ns typ (50 ohm load)
P_D = 220 mW typ/pkg
Full Load Current, I_L = −25 mAdc max



L SUFFIX
CERAMIC PACKAGE
CASE 620



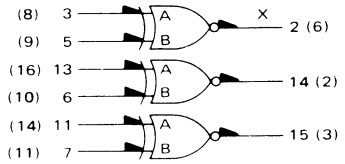
F SUFFIX
CERAMIC PACKAGE
CASE 650

Number at end of terminal denotes pin number for L package.
Number in parenthesis denotes pin number for F package.

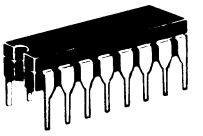
Characteristic	Symbol	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit
Power Supply Drain Current	I_E	–	–	–	55	–	–	mAdc
Input Current								μAdc
A Inputs	I_{inH}	–	–	–	350	–	–	
B Inputs	I_{inH}	–	–	–	270	–	–	
Switching Times								ns
Propagation Delay A Inputs	t++,t−+	–	2.0	–	1.8	–	2.3	
	t+−,t−−	–	2.1	–	1.9	–	2.4	
B Inputs	t++,t−+	–	2.5	–	2.3	–	2.8	
	t+−,t−−	–	2.5	–	2.3	–	2.8	
Rise Time (10% to 90%)	t+	–	2.7	–	2.5	–	2.9	ns
Fall Time (10% to 90%)	t−	–	2.4	–	2.2	–	2.6	ns

MC1674

TRIPLE 2-INPUT EXCLUSIVE-NOR GATE



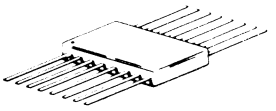
$X = \overline{A} \bullet \overline{B} + A \bullet B$



L SUFFIX
CERAMIC PACKAGE
CASE 620

V_{CC1} = Pin 1(5)
V_{CC2} = Pin 16(4)
V_{EE} = Pin 8(12)

t_{pd} = 1.1 ns typ (510 ohm load)
= 1.3 ns typ (50 ohm load)
P_D = 220 mW typ/pkg
Full Load Current, I_L = -25 mAdc max



F SUFFIX
CERAMIC PACKAGE
CASE 650

Number at end of terminal denotes pin number for L package.
Number in parenthesis denotes pin number for F package.

Characteristic		Symbol	-30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit
Power Supply Drain Current		I_E	—	—	—	55	—	—	mAdc
Input Current									μAdc
	A Inputs	I_{inH}	—	—	—	350	—	—	
	B Inputs	I_{inH}	—	—	—	270	—	—	
Switching Times									ns
Propagation Delay	A Inputs	t++,t−+	—	2.0	—	1.8	—	2.3	
		t+−,t−−	—	2.1	—	1.9	—	2.4	
	B Inputs	t++,t−+	—	2.5	—	2.3	—	2.8	
		t+−,t−−	—	2.5	—	2.3	—	2.8	
Rise Time (10% to 90%)		t+	—	2.7	—	2.5	—	2.9	ns
Fall Time (10% to 90%)		t−	—	2.4	—	2.2	—	2.6	ns

MC1678

BI-QUINARY COUNTER

The MC1678 is a four-bit counter capable of divide-by-two, divide-by-five, or divide-by-10 functions. When used independently, the divide-by-two section will toggle at 350 MHz typically, while the divide-by-five section will toggle at 325 MHz typically. Clock inputs trigger on the positive going edge of the clock pulse.

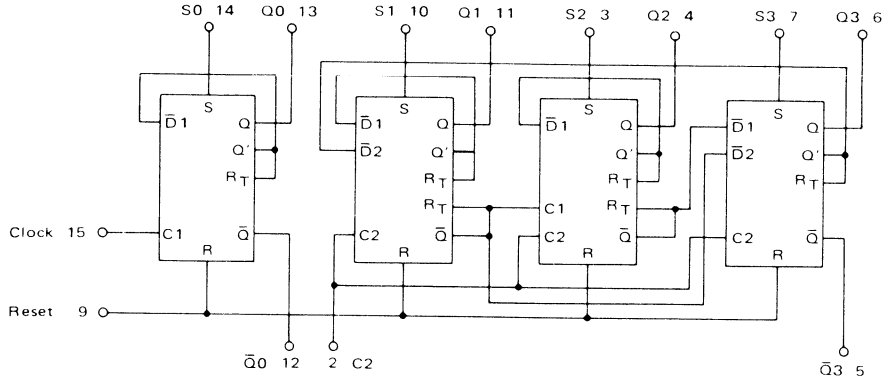
Set and Reset inputs override the clock, allowing asynchronous "set" or "clear". Individual Set and common Reset inputs are provided, as well as complementary outputs for the first and fourth bits. True outputs are available at all bits.

DC Input Loading Factor — R = 2.40, C1 = 0.77, C2 = 1.23, S = 1.00

DC Output Loading Factor = 70

Power Dissipation = 750 mW typ

f_{Tog} = 350 MHz typ



COUNTER TRUTH TABLES

BCD
(Clock connected to C1 and $\bar{Q}0$ connected to C2)

COUNT	Q0	Q1	Q2	Q3
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	H	L	H	L
6	L	H	H	L
7	H	H	H	L
8	L	L	L	H
9	H	L	L	H

BI-QUINARY
(Clock connected to C2 and $\bar{Q}3$ connected to C1)

COUNT	Q1	Q2	Q3	Q0
0	L	L	L	L
1	H	L	L	L
2	L	H	L	L
3	H	H	L	L
4	L	L	H	L
5	L	L	L	H
6	H	L	L	H
7	L	H	L	H
8	H	H	L	H
9	L	L	H	H

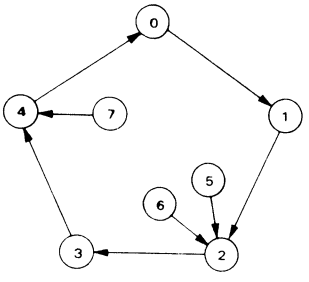
R-S

C	R	S	Q_{n+1}
ϕ	L	L	Q_n
ϕ	H	L	L
ϕ	L	H	H
ϕ	H	H	ND

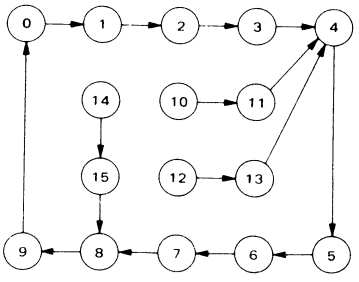
ϕ = Don't Care
ND = Not Defined

COUNTER STATE DIAGRAM – POSITIVE LOGIC

Clock connected to C2



Q0 connected to C2

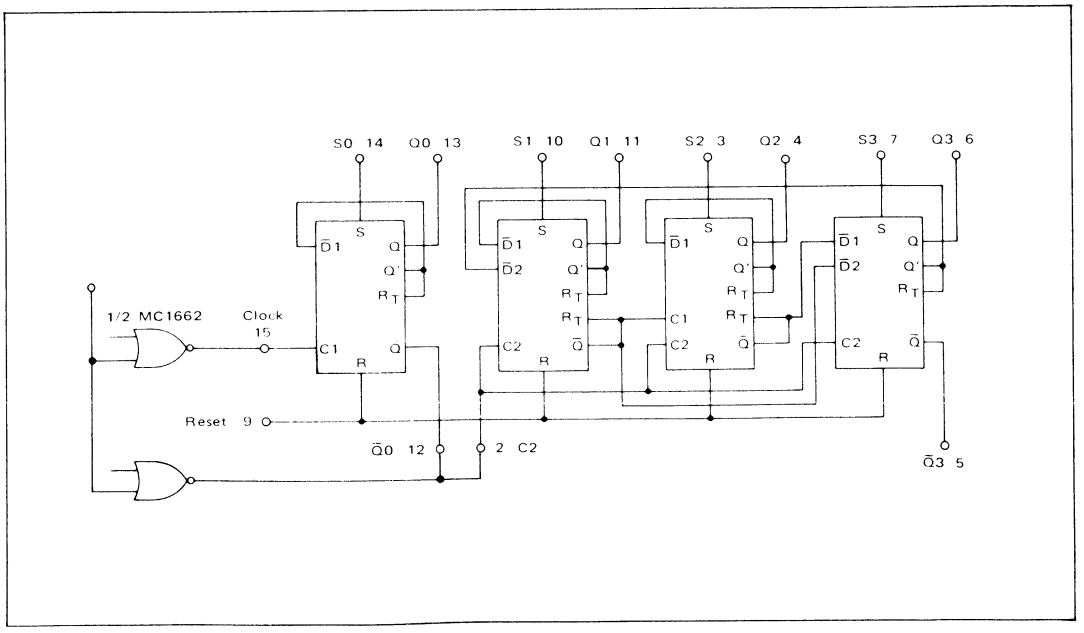


ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	−30°C Min	−30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit
Power Supply Drain Current	I_E	–	–	–	200	–	–	mAdc
Input Current	I_{inH}							mAdc
Reset		–	–	–	1.00	–	–	
C2		–	–	–	0.70	–	–	
Set, Clock		–	–	–	0.45	–	–	
Switching Times								ns
Propagation Delay	t_{pd}							
Clock to $\overline{Q}0$, Q0		1.0	2.9	1.0	2.7	1.0	3.1	
C2 to Q1, Q2, Q3, $\overline{Q}3$		1.0	3.2	1.0	3.0	1.0	3.4	
Set, Reset		2.0	3.9	2.0	3.7	2.0	4.1	
Rise Time (10% to 90%)	t+	1.0	2.9	1.0	2.7	1.0	3.1	ns
Fall Time (10% to 90%)	t−	1.0	2.8	1.0	2.6	1.0	3.0	ns
Toggle Frequency	f_{Tog}							MHz
Q0		260	–	300	–	260	–	
Q3		250	–	275	–	250	–	

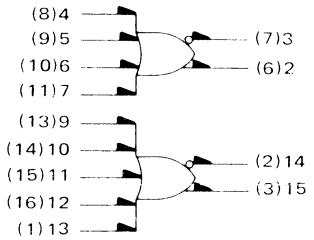
APPLICATIONS INFORMATION

With the addition of a single gate package, the MC1678 will count in a fully synchronous mode, as shown below.



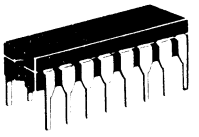
MC1688

DUAL 4-5-INPUT OR/NOR GATE

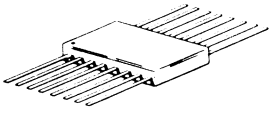


V_{CC1} = Pin 1(5)
V_{CC2} = Pin 16(4)
V_{EE} = Pin 8(12)

t_{pd} = 0.8 ns typ
P_D = 125 mW typ/pkg (No Load)
Output Rise and Fall Times
(10% to 90%) 1.1 ns



L SUFFIX
CERAMIC PACKAGE
CASE 620



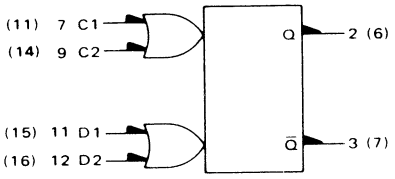
F SUFFIX
CERAMIC PACKAGE
CASE 650

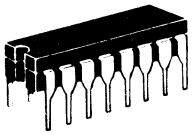
Number at end of terminal denotes pin number for L package
Number in parenthesis denotes pin number for F package

Characteristic	Symbol	−30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	–	–	30	–	–	mAdc
Input Current	I_{inH}	–	–	–	350	–	–	μAdc
Switching Times								ns
Propagation Delay	t_{pd}	0.5	1.5	0.5	1.3	0.5	1.5	
Rise Time, Fall Time (10% to 90%)	t+,t−	0.5	1.6	0.5	1.4	0.5	1.6	ns

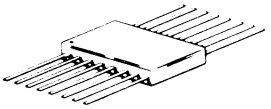
MC1690

UHF PRESCALER
TYPE D FLIP-FLOP





L SUFFIX
CERAMIC PACKAGE
CASE 620



F SUFFIX
CERAMIC PACKAGE
CASE 650

TRUTH TABLE

C	D	Q_{n+1}
L	ϕ	Q_n
H	ϕ	Q_n
⌐⌐	L	L
⌐⌐	H	H

C = C1 + C2 ϕ = Don't Care
D = D1 + D2

V_{CC1} = Pin 1(5)
V_{CC2} = Pin 16(4)
V_{EE} = Pin 8(12)

P_D = 200 mW typ/pkg (No Load)
f_{Tog} = 500 MHz min

Number at end of terminal denotes pin number for L package
Number in parenthesis denotes pin number for F package

Characteristic	Symbol	-30°C		+25°C			+85°C		Unit
		Min	Max	Min	Typ	Max	Min	Max	
Power Supply Drain Current	I_E	—	—	—		59	—	—	mAdc
Input Current	I_{inH}								μAdc
Pins 7,9		—	—	—		250	—	—	
Pins 11,12		—	—	—		270	—	—	
Switching Times				Min	Typ	Max			ns
Propagation Delay	t_{pd}	—	—	—	1.5	—	—	—	
Rise Time, Fall Time (10% to 90%)	t+,t−	—	—	—	1.3	—	—	—	ns
Setup Time	t_{setup}	—	—	—	0.3	—	—	—	ns
Hold Time	t_{hold}	—	—	—	0.3	—	—	—	
Toggle Frequency	f_{Tog}	500	—	500	540	—	500	—	MHz

FIGURE 1 – TOGGLE FREQUENCY TEST CIRCUIT

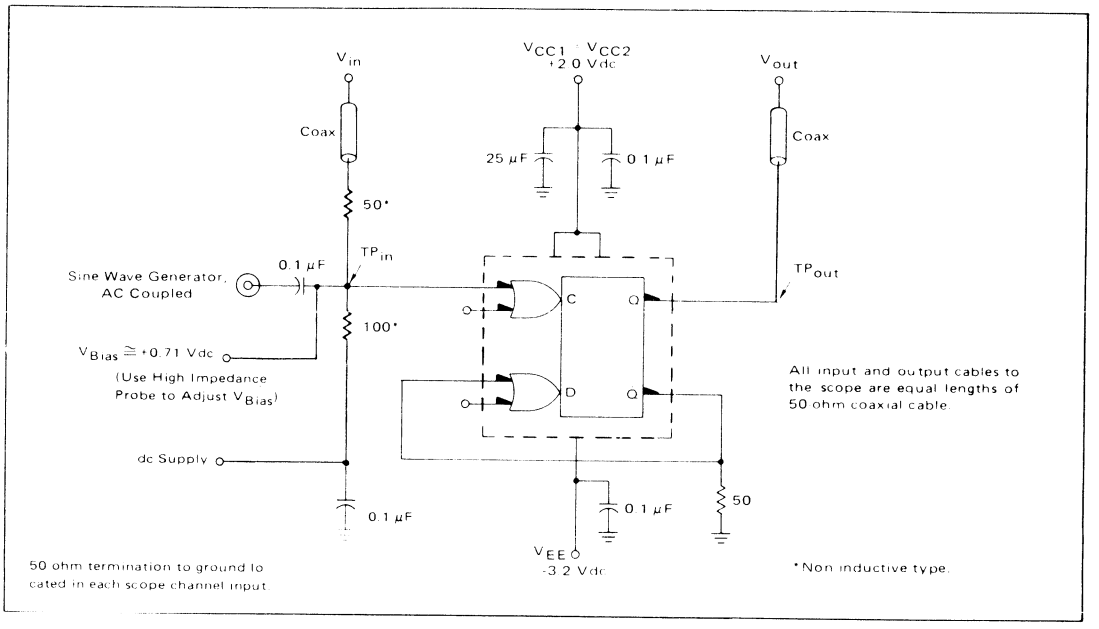
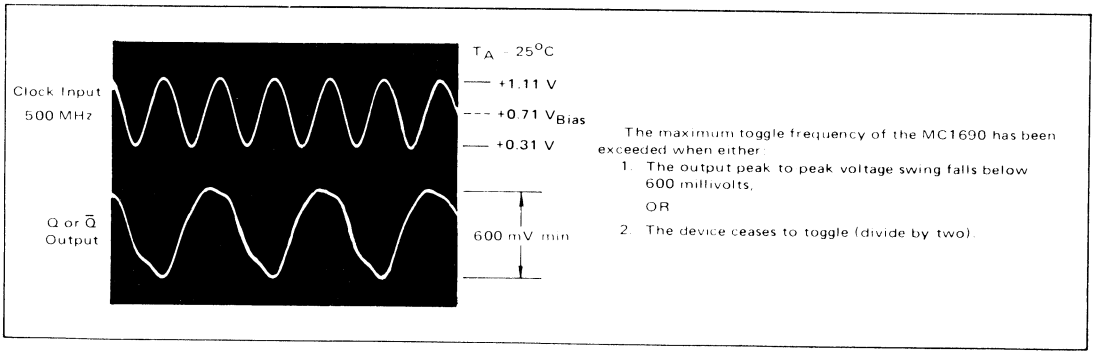


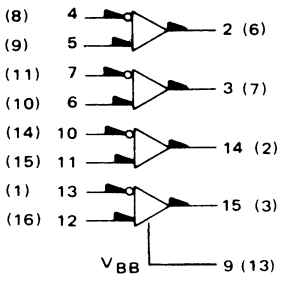
FIGURE 2 – TOGGLE FREQUENCY WAVEFORMS

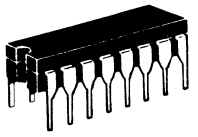


Note: All power supply and logic levels are shown shifted 2 volts positive.

MC1692

QUAD LINE RECEIVER



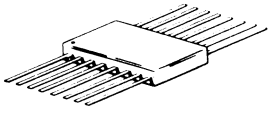


L SUFFIX
CERAMIC PACKAGE
CASE 620

V_{CC1} = Pin 1 (5)
V_{CC2} = Pin 16 (4)
V_{EE} = Pin 8 (12)

t_{pd} = 0.9 ns typ (510-ohm load)
= 1.1 ns typ (50-ohm load)

P_D = 220 mW typ/pkg (No Load)
Full Load Current, I_L = -25 mAdc max



F SUFFIX
CERAMIC PACKAGE
CASE 650

Numbers at ends of terminals denote pin numbers for L package
Numbers in parenthesis denote pin numbers for F package

Characteristic	Symbol	-30°C		+25°C		+85°C		Unit
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	—	—	—	50	—	—	mAdc
Input Current	I_{in}	—	—	—	250	—	—	μAdc
Input Leakage Current	I_R	—	—	—	100	—	—	μAdc
Reference Voltage	V_{BB}	- 1.375	-1.275	-1.35	-1.25	-1.30	-1.20	Vdc
Switching Times								ns
Propagation Delay	t^{-+}	0.6	1.6	0.6	1.5	0.6	1.7	
	t^{+-}	0.6	1.8	0.6	1.7	0.6	1.9	
Rise Time, Fall Time (10% to 90%)	t^+, t^-	0.6	2.2	0.6	2.1	0.6	2.3	ns

APPLICATION INFORMATION

The MC1692 quad line receiver is used primarily to receive data from balanced twisted pair lines, as indicated in Figure 1. The line is driven with a MC1660 OR/NOR gate. The MC1660 is terminated with 50 ohm resistors to -2.0 volts. At the end of the twisted pair a 100 ohm termination resistor is placed across the differential line receiver inputs of the MC1692. Illustrated in Figure 2 is the sending and receiving waveforms at a data rate of 400 megabits per second over an 18 foot twisted pair cable. The waveform picture of Figure 3 shows a 5 nanosecond pulse being propagated down the 18 foot line. The delay time for the line is 1.68 ns/foot.

The MC1692 may also be applied as a high frequency schmitt trigger as illustrated in Figure 4. This circuit has been used in excess of 200 MHz. The MC1692 when loaded into 50 ohms will produce an output rising edge of about 1.5 nanoseconds.

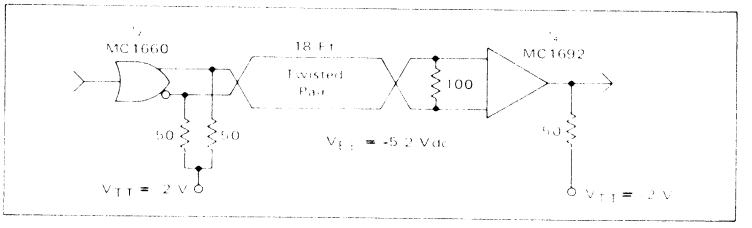


FIGURE 1 – LINE DRIVER/RECEIVER

FIGURE 2 – 400 MBS WAVEFORMS

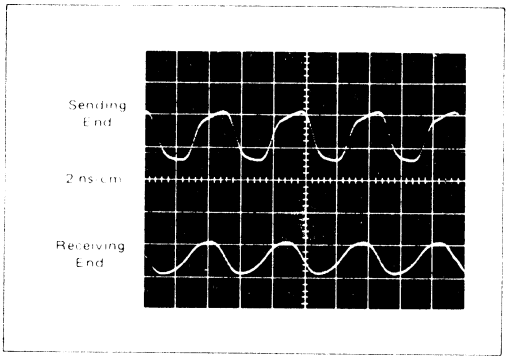
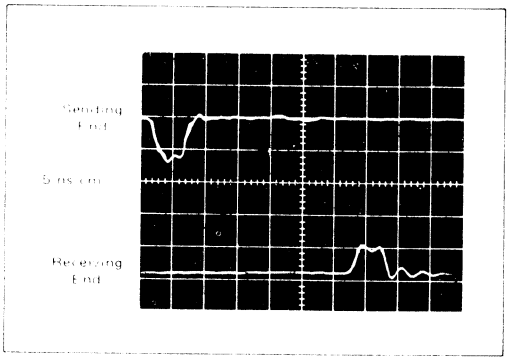


FIGURE 3 – PULSE PROPAGATION WAVEFORMS



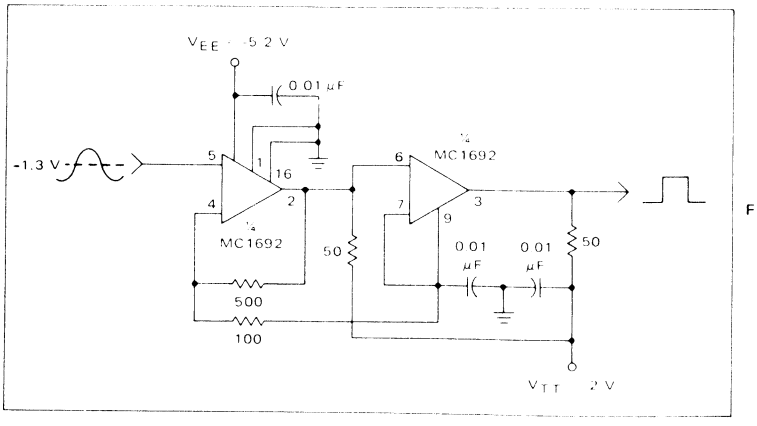


FIGURE 4 – 200 MHz SCHMITT TRIGGER

MC1694

4-BIT SHIFT REGISTER

FLIP-FLOP TRUTH TABLE

Inputs				Output
D	C	R	S	Q_n
0	0	0	0	$Q_{n\,1}$
0	0	0	1	1
0	0	1	0	0
0	0	1	1	*
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	*
1	0	0	0	$Q_{n\,1}$
1	0	0	1	1
1	0	1	0	0
1	0	1	1	*
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	*

*Output State Undefined

V_{CC1} = 1
V_{CC2} = 16
V_{EE} = 8

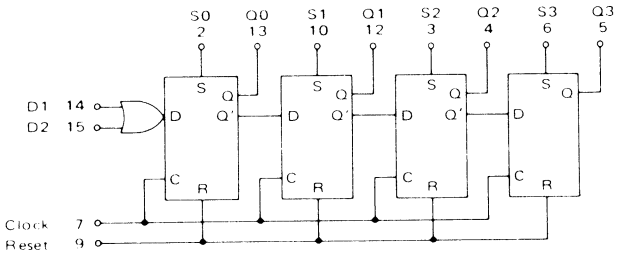
The MC1694 is a 4-Bit register capable of shift rates up to 325 MHz (typical) in the shift-right mode, accepting serial data at either data input D1 or D2. A master reset and individual set inputs override the clock allowing asynchronous entry of information.

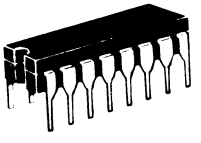
DC Input Loading Factors
Reset = 2.5 Set = 1.0
Clock = 1.6 Data = 0.9

DC Output Loading Factor = 70

Total Power Dissipation = 750 mW typ/pkg

Shift Frequency = 325 MHz typ





L SUFFIX
CERAMIC PACKAGE
CASE 620

Characteristic	Symbol	-30°C Min	-30°C Max	+25°C Min	+25°C Max	+85°C Min	+85°C Max	Unit
Power Supply Drain Current	I_E	—	—	—	200	—	—	mAdc
Input Current	I_{inH}							mAdc
Pin 9		—	—	—	1.0	—	—	
Pin 7		—	—	—	0.75	—	—	
Pins 2,3,6,10		—	—	—	0.6	—	—	
Pins 14,15		—	—	—	0.5	—	—	
Switching Times								ns
Propagation Delay	t_{pd}							
Clock		1.0	3.2	1.0	3.0	1.0	3.4	
Set, Reset		2.0	3.9	2.0	3.7	2.0	4.1	
Rise Time (10% to 90%)	t+	1.0	2.9	1.0	2.7	1.0	3.1	ns
Fall Time (10% to 90%)	t-	1.0	2.8	1.0	2.6	1.0	3.0	ns
Shift Rate		240	—	275	—	250	—	MHz

MC1697

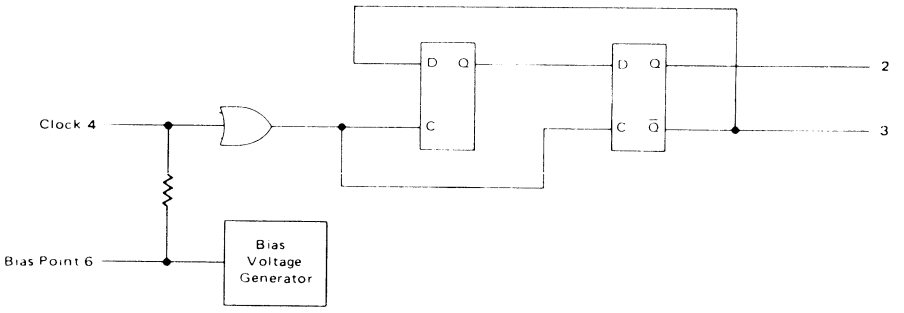
1-GHz DIVIDE-BY-FOUR PRESCALER

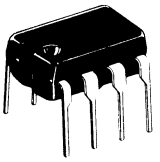
The MC1697 is a divide-by-four gigahertz prescaler in an 8 pin plastic package. The clock input requires an ac coupled driving signal of 800 mV amplitude (typical). The clock toggles two divide-by-two stages, and the complementary outputs (50% duty cycle) are taken from the second stage. The complementary outputs are capable of driving 50-ohm lines.

Pin 6 is available for connection of a decoupling capacitor to ground. This capacitor stabilizes the reference point which is internally coupled to the clock input.

V_{CC1} = Pin 1
V_{CC2} = Pin 8
V_{EE} = Pin 5

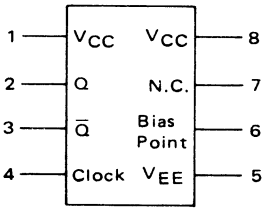
Power Dissipation = 320 mW Typ/Pkg
(No Load – 7.0 V Supply)





P SUFFIX
PLASTIC PACKAGE
CASE 626

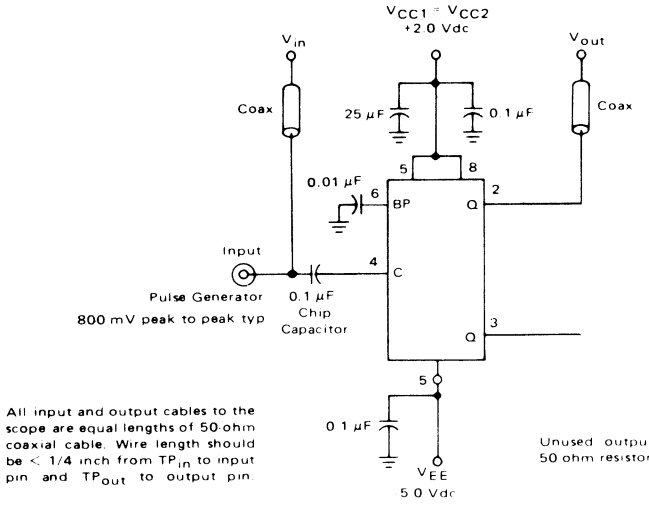
PIN ASSIGNMENT



ELECTRICAL CHARACTERISTICS

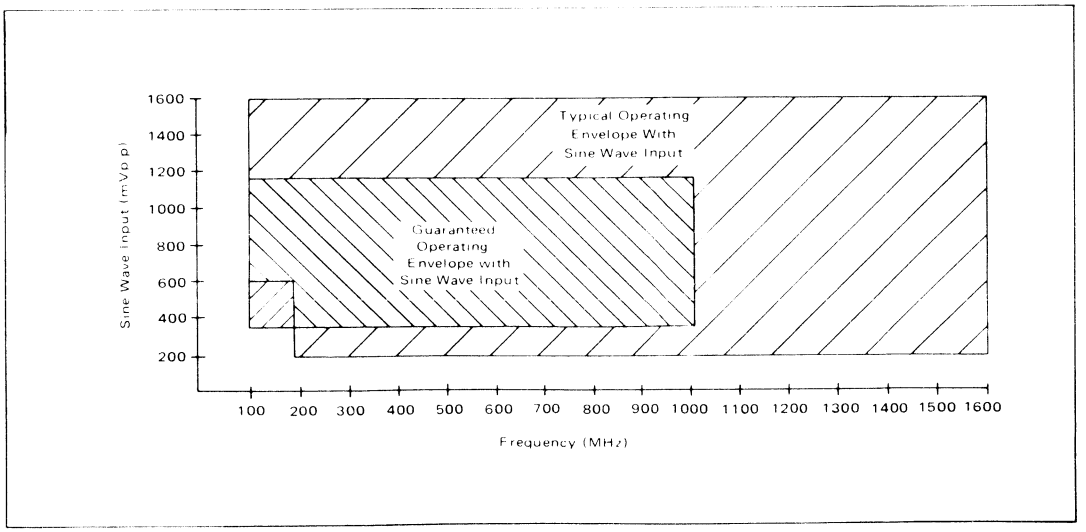
Characteristic	Symbol	MC1697P Test Limits						Unit
		0°C		+25°C		+75°C		
		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	I_E	–	–	–	57	–	–	mAdc
Toggle Frequency (high frequency operation)	f_{Tog}	1.0	–	1.0	–	1.0	–	GHz
Toggle Frequency (low frequency sine wave input)	f_{Tog}	–	–	–	100	–	–	MHz

COUNT FREQUENCY TEST CIRCUIT



Note: All power supply and logic levels are shown shifted 2 volts positive.

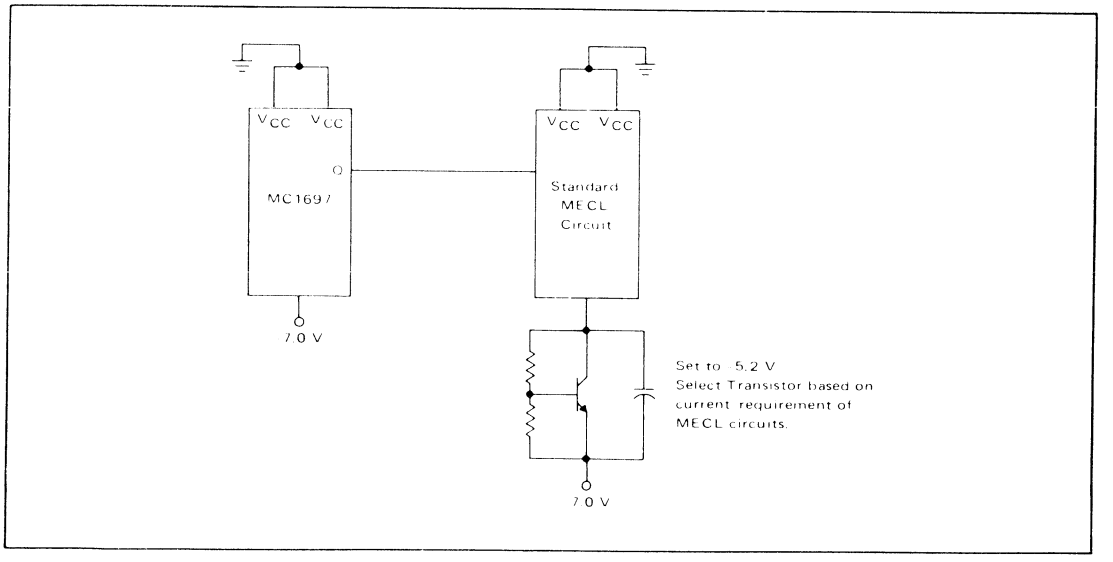
TIMING DIAGRAM



APPLICATION INFORMATION

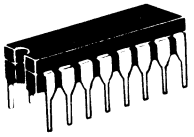
The MC1697 is a very high speed divide by four prescaler designed to operate on a nominal supply voltage of -7.0 volt. In some applications it may be necessary to interface the output of the MC1697 with other MECL circuits requiring a supply voltage of -5.2 volts. One method of interfacing the circuits is shown below. This configuration is adequate for frequencies up to 1 GHz over the temperature range of 0^{o} to $+75^{o}C$. For best performance it is recommended that separate regulated supplies be used.

METHOD OF INTERFACING MC1697 WITH STANDARD MECL CIRCUITS

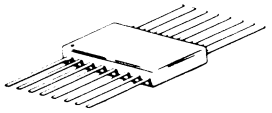


MC1699

DIVIDE-BY-FOUR GIGAHERTZ COUNTER



L SUFFIX
CERAMIC PACKAGE
CASE 620

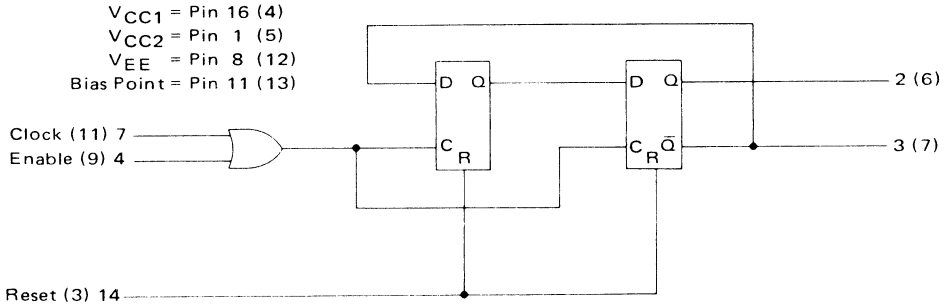


F SUFFIX
CERAMIC PACKAGE
CASE 650

The MC1699 is a divide-by-four gigahertz counter. The clock input requires an ac coupled driving signal of 800 mV amplitude (typical). The clock toggles two divide-by-two stages, and the complementary outputs (50% duty cycle) are taken from the second stage.

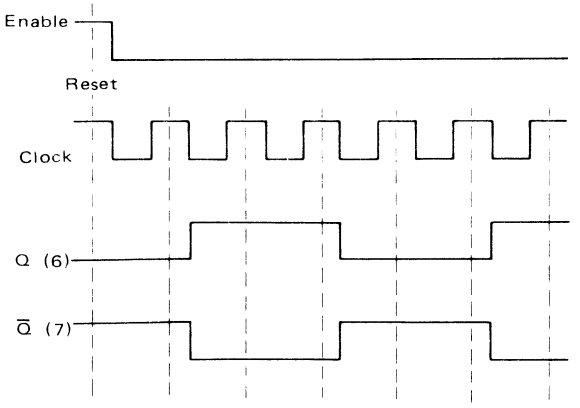
The MC1699 includes clock enable and reset. The reset is compatible with MECL III voltage levels. The enable input requires a V_{IL} of -2.0 V max. Reset operates only when either the clock or the enable is high.

Pin 11 (13) is available for connection of a decoupling capacitor to ground. This capacitor stabilizes the reference point which is internally coupled to the clock input.



Number at end of terminal denotes pin number for L package (Case 620).
Number in parenthesis denotes pin number for F package (Case 650).

TIMING DIAGRAM

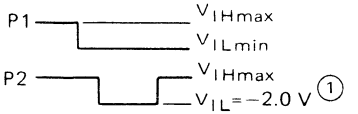


ELECTRICAL CHARACTERISTICS

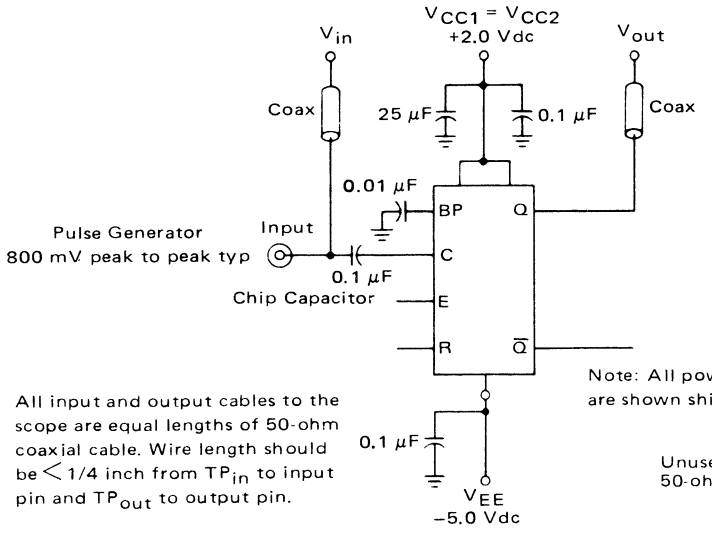
Characteristic	Symbol	-30°C		+25°C		+85°C		Unit	Conditions
		Min	Max	Min	Max	Min	Max		
Power Supply Drain Current	I_E	–	–	–	57	–	–	mAdc	All inputs and outputs open except Clock = $V_{IHC} \cong$ -4.0 Vdc
Input Current	I_{inH}							μAdc	
Reset		–	–	–	500	–	–		V_{IHmax} to Reset, V_{IL} to Enable, V_{EE} to Clock.
Enable		–	–	–	265	–	–		V_{ILmin} to reset, V_{IHmax} to Enable, V_{EE} to Clock.
Logic "1" Output Voltage	V_{OH}	-1.085	-0.875	-1.000	-0.810	-0.930	-0.700	Vdc	See Note ② . Or, apply P1 to Reset and V_{IHmax} to Enable
Logic "0" Output Voltage	V_{OL}	–	-1.630	–	-1.600	–	-1.555	Vdc	
Toggle Frequency (high frequency operation)	f_{Tog}	1.0	–	1.0	–	1.0	–	GHz	V_{IL} ① to Enable. See Test Circuit and Application Information on next page.
Toggle Frequency (low frequency sine wave input)	f_{Tog}	–	–	–	100	–	–	MHz	

① Enable input requires V_{IL} = -2.0 V max.

② Reset counter by applying pulse P1 to pin 14, then toggle outputs by applying pulse P2 to pin 4 for 2 cycles. Hold power during pulse sequence. Hold clock input @ V_{EE}.



TOGGLE FREQUENCY TEST CIRCUIT



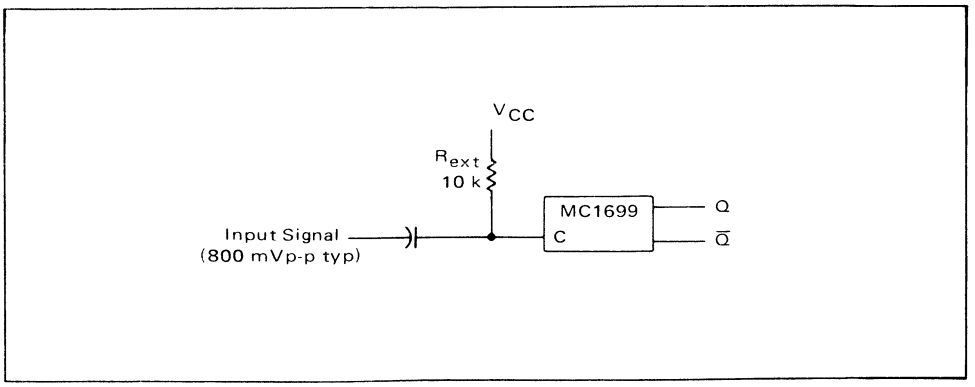
APPLICATION INFORMATION

The MC1699 is a very high speed divide-by-four counter intended for prescaler applications. The reset provides increased flexibility for counter and time measuring requirements.

The clock input is designed to accept a capacitor-coupled sine wave signal for frequencies above 100 MHz. Below 100 MHz waveshaping is recommended to obtain good MECL III or MECL 10,000 edge speeds.

With a continuous input signal the clock can be capacitor-coupled with no problems. However, if the clock is interrupted and the clock input floats to the bias point reference voltage, the counter may oscillate. To prevent this oscillation, an external resistor can be added as shown in Figure 1. This resistor is recommended only when the clock is interrupted and serves no useful function with a continuous signal. Also, this external resistor is not required when the enable input is used to gate the clock signal.

FIGURE 1

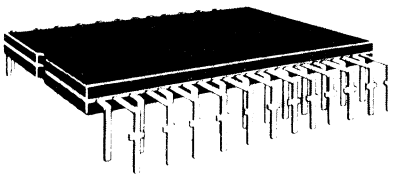


MI0800 PROCESSOR FAMILY

5

M10800

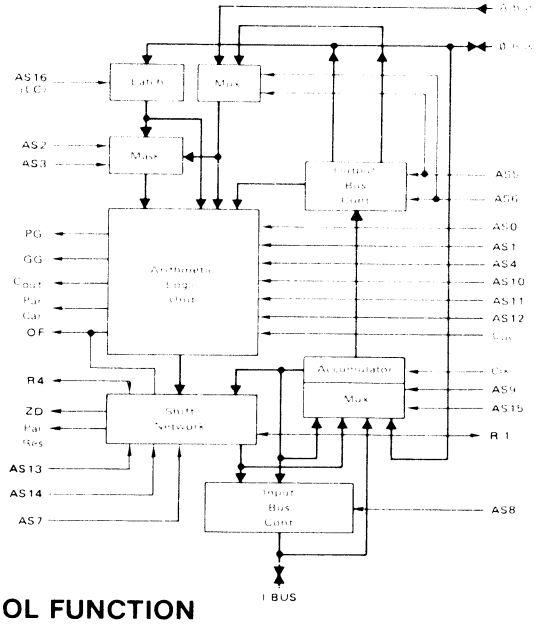
MECL LSI HIGH-PERFORMANCE PROCESSOR FAMILY



MC10800 4-BIT SLICE

The MC10800 4-Bit ALU Slice is an LSI building block for digital processors. This circuit performs the necessary logic and arithmetic functions required to execute the various machine instructions. Each part is 4 bits wide and is "sliced" parallel to data flow. The MC10800 is fully expandable to larger word lengths by connecting circuits in parallel and features three input/output data ports for maximum system flexibility.

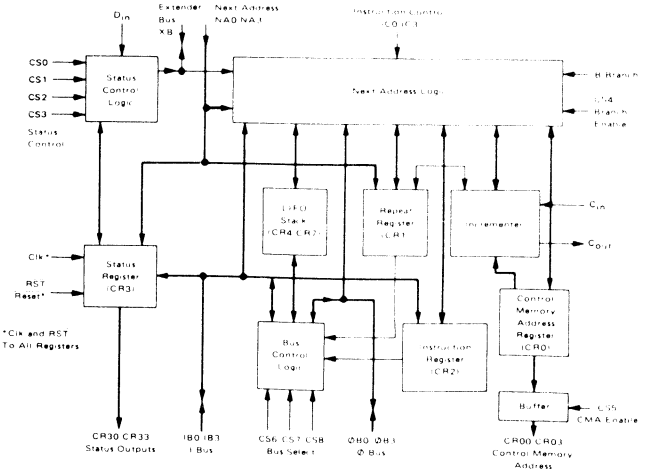
The 4-Bit ALU Slice as shown in the block diagram contains latch/mask logic, ALU, shift network, accumulator, and bus control logic in a single bipolar circuit. Seventeen select lines are used to control all operations within the part.



MC10801 MICROPROGRAM CONTROL FUNCTION

The MC10801 Microprogram Control Function is an LSI building block for digital processor systems. This circuit controls machine operations by generating the addresses and sequencing pattern for microprogram control storage. The MC10801 is compatible with a wide range of control memory sizes and organizations. Each part is 4 bits wide and can be connected in parallel for larger memory addresses. Maximum system flexibility is maintained with 5 separate data ports.

The Microprogarm Control Function as shown in the block diagram contains a control memory address register CR0, multipurpose registers CR1-CR3, an incrementer, a subroutine LIFO, and the associated next address, status, and bus control logic in a single MECL Bipolar LSI circuit. Nine select (CS) lines and four instruction inputs (IC) control all operations within the part.

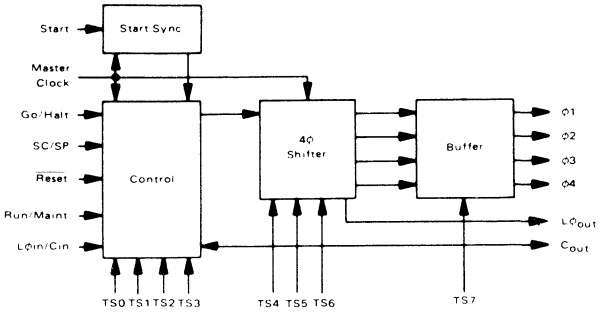


5

MC10802 TIMING FUNCTION

The MC10802 Timing Function is an LSI building block for digital processor systems. This circuit contains the logic and control lines to generate system clock phases and provides for start, stop, and diagnostic operations. Each part is 4-bits wide and can be connected in series for greater than four phase clock systems.

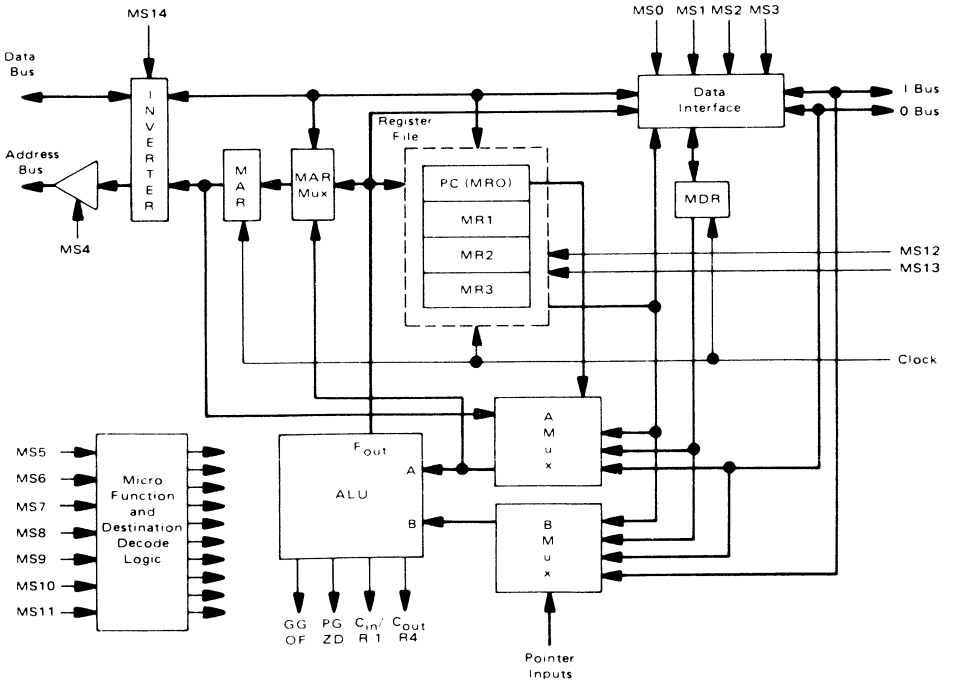
The Timing Function as shown in the block diagram is composed of a four phase shifter circuit with buffered outputs. Fifteen input lines combine with Control and Start Sync logic to control all operations within the part.



MC10803 MEMORY INTERFACE FUNCTION

The MC10803 Memory Interface Function is an LSI building block for interfacing a high-speed processor system to main memory or peripheral equipment. The circuit contains the logic and storage registers for generating memory address and routing incoming or outgoing data. Each part is 4-bits wide and can be connected in parallel to meet wider system I/O word requirements. An internal ALU allows the MC10803 to also assume processor ALU responsibility for many controller applications. Maximum system flexibility is maintained with 5 separate data ports.

The Memory Interface Function as shown in the block diagram contains six 4-bit registers, an ALU with encoded function/operand select logic, and data transfer circuitry on a single MECL bipolar LSI circuit. Fifteen select (MS) lines control register selection, 13 basic ALU functions, and 17 data transfer operations.



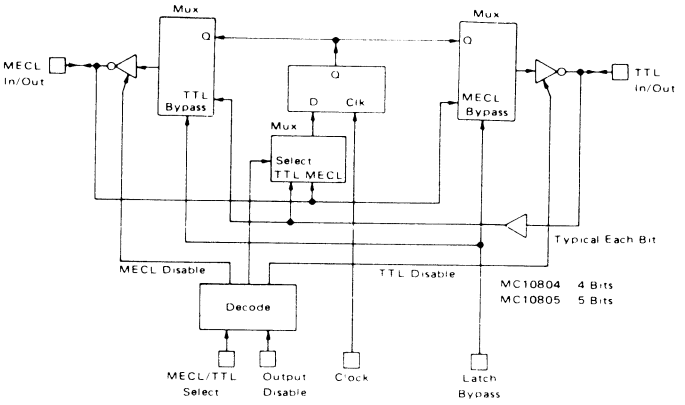
5

MC10804/5 MECL/TTL BIDIRECTIONAL TRANSLATORS WITH LATCH

The MC10804 and MC10805 are bidirectional transceivers that interface MECL logic levels with TTL logic levels. Data can be transferred directly in either direction (MECL → TTL or TTL → MECL), and an optional gated latch is also provided. Logic levels are inverted during transfers. The MC10804 is a 4-bit version in the 16-pin package, and the MC10805 is a 5-bit version in the 20-pin package.

The MC10804 and MC10805 are members of the high performance M10800 MECL/LSI processor family. They make it possible to easily interface to MOS memories, TTL compatible peripherals, or existing TTL subsystems.

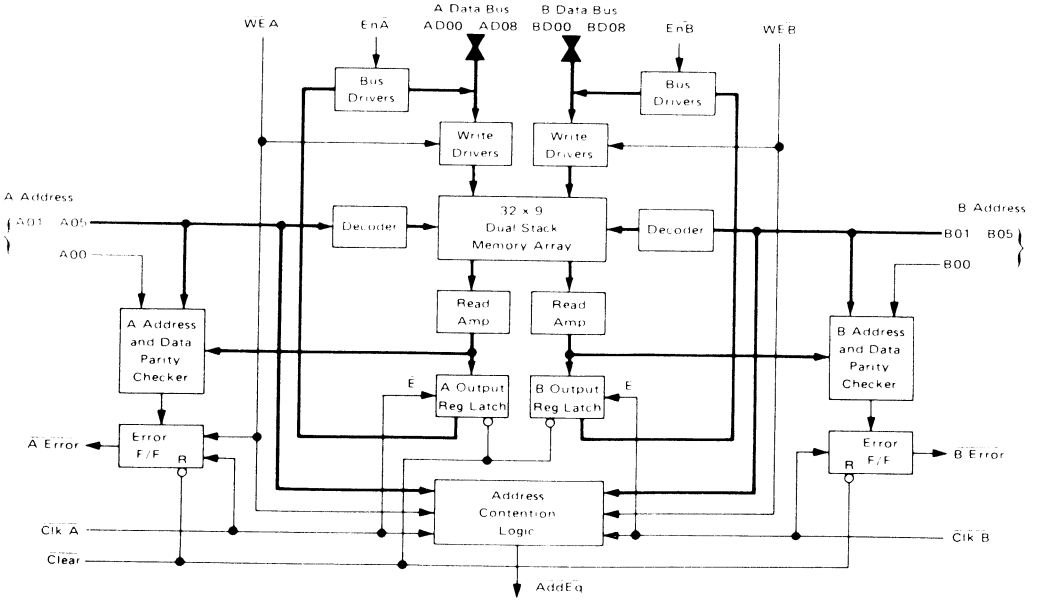
- Bidirectional Translation
- Power Supplies: +5.0 Volts and -5.2 Volts
- TTL Three-State Outputs
  Sink 50 mA Source 5 mA
- Standard MECL 50 Ohm Drive Outputs
- Latch – May Be Bypassed for High Speed
- High Capacitive MOS Drive Capability on MC10805



MC10806 DUAL ACCESS STACK

The MC10806 Dual Access Stack is an LSI building block for digital processor systems. This circuit consists of 32 words by 9 bits of memory with two independent address and data ports. The circuit is easily expandable in both the word and bit directions making it ideal in register file, scratch pad, and high-speed buffer application.

The Dual Access Stack, as shown in the block diagram, contains a 32 x 9 memory array, two address ports, two 9-bit data input/output ports, two 9-bit output registers, address and data parity checking logic, and two error flip-flops in a single MECL Bipolar LSI circuit. Separate read, write, and output enables exist for each port to control all operations within the part.

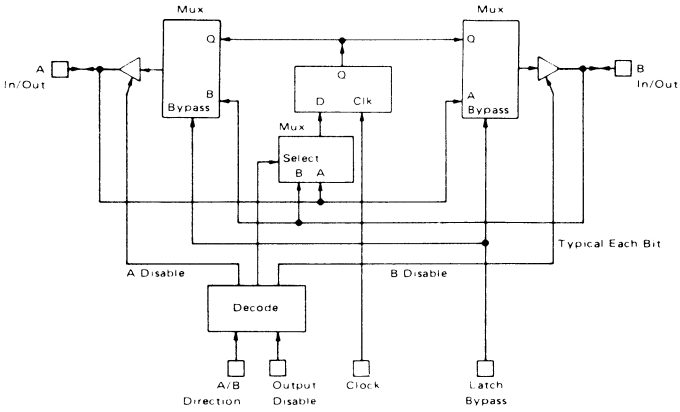


MC10807 5-BIT TRANSCEIVER WITH LATCH

The MC10807 is a 5-bit bidirectional MECL transceiver bus. Data can be transferred directly in either direction (A port → B port or B port → A port), and an optional gated latch is also provided. The MC10807 is in a 16-pin ceramic package.

The MC10807 is a member of the high performance M10800 MECL/LSI processor family. It is designed to provide bidirectional exchange of MECL level signals in multiprocessor installations, or multiplexing of buses to a single processor.

- MECL 10,000 Levels
- Bidirectional Data Transfer
- Standard MECL 50 Ohm Drive Outputs
- Latch – May Be Bypassed for High Speed
- Temperature Range – -30° to +85°C
- 16-Pin CERDIP Package

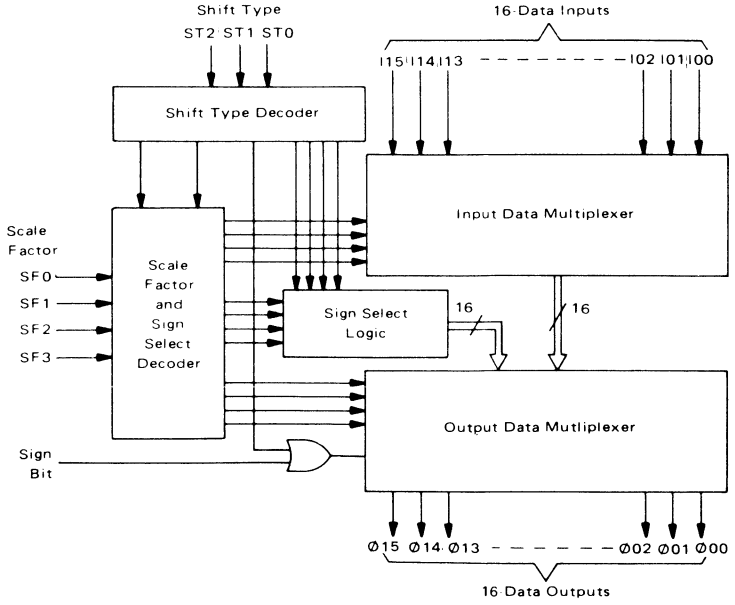


MC10808 PROGRAMMABLE MULTI-BIT SHIFTER

The MC10808 Programmable Multi-Bit Shifter is 16 bits wide and is fully expandable in a shifter array to handle any number of bits.

There are 16 data inputs and 16 data outputs for shifting the data under the control of 4 scale factor inputs that specify the number of positions the input data should be shifted or rotated. A sign bit input is used for arithmetic shift right or left and sign extend operations. There are 3 shift select inputs that are used to select the appropriate shifting function.

The data outputs of the MC10808 can be disabled for wire-ANDing (negative logic) other device outputs by selecting the sign bit at all the outputs (SBO function) and forcing the sign bit to a negative logic "1".

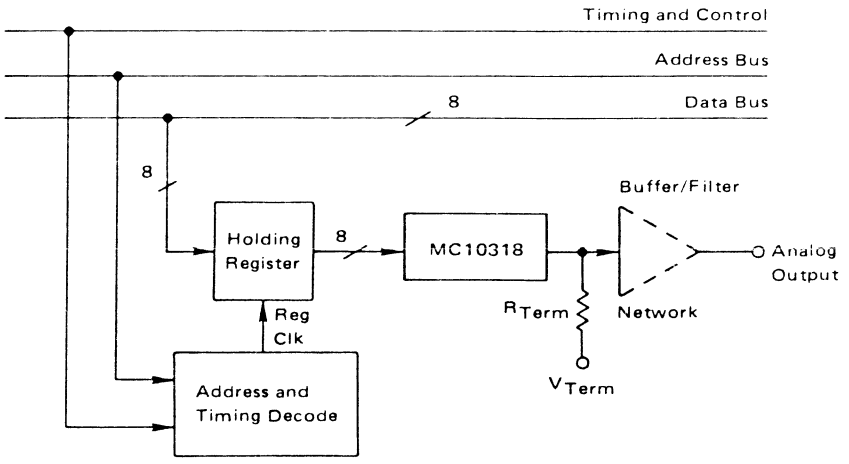


5

MC10318 HIGH-SPEED MECL DIGITAL-TO-ANALOG CONVERTER

Intended for applications in instrumentation, communication and television broadcasting, the MC10318 is an eight-bit accurate D/A converter operating at speeds above 10 MHz. The inputs are compatible with MECL 10K series logic while the complementary current sink outputs feature current of up to 50 mA. Devices are specified to be 8-bit (± 1/2 LSB) accurate, monotonic and operate over a −30° C to 85° C temperature range.

TYPICAL MC10318 TO MC10800 PROCESSOR INTERFACE



5

MOTOROLA Semiconductors

MC10800
MC10800M

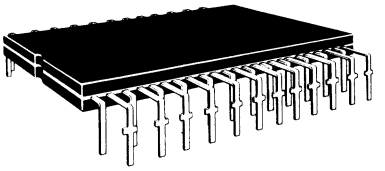
INTRODUCTION

The MC10800 4-Bit ALU Slice is an LSI building block for digital processors. This circuit performs the necessary logic and arithmetic functions required to execute the various machine instructions. Each part is 4 bits wide and is "sliced" parallel to data flow. The MC10800 is fully expandable to larger word lengths by connecting circuits in parallel and features three input/output data ports for maximum system flexibility.

The 4-Bit ALU Slice as shown in the block diagram below contains latch/mask logic, ALU, shift network, accumulator, and bus control logic in a single bipolar circuit. Seventeen select lines are used to control all operations within the part.

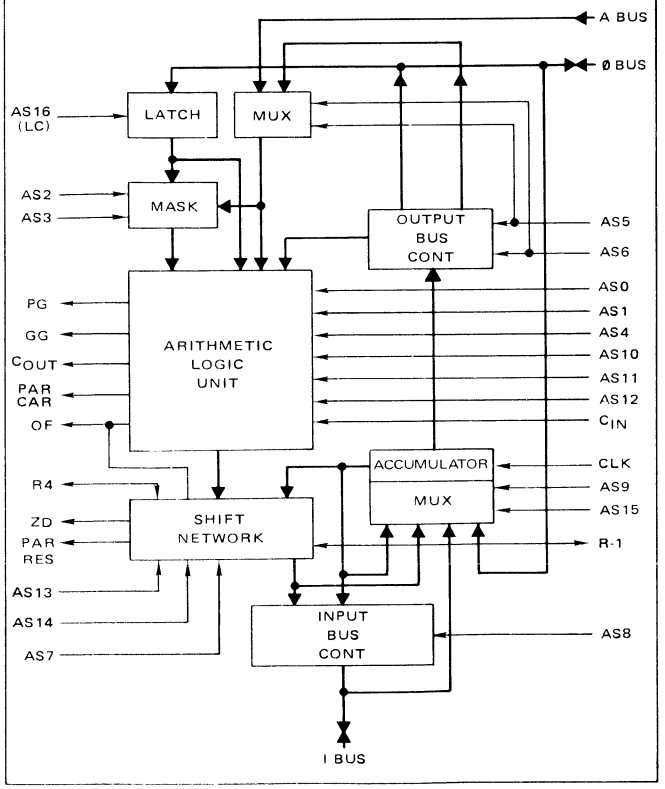
The MC10800M is intended for applications having an ambient temperature range beyond the standard -30° to +85°C. Performance data is provided for -55°C ambient and +150°C junction temperature.

MECL—LSI 4-BIT ALU SLICE

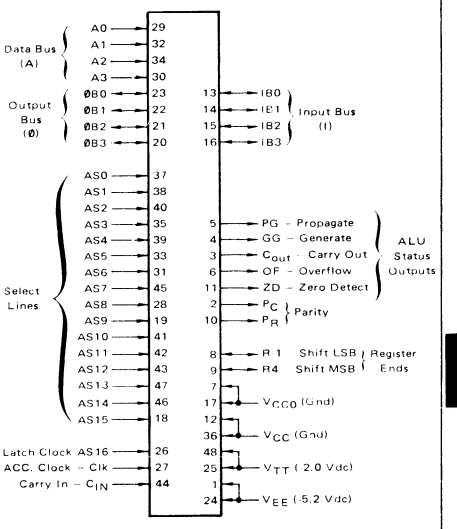


Case 725-01

4-BIT SLICE BLOCK DIAGRAM



INPUT/OUTPUT DIAGRAM



DS9437
(Replaces ADI 364)

5

TABLE OF CONTENTS

IMPORTANT FEATURES

1. Powerful ALU
   a. Full binary and BCD arithmetic.
   b. A and Ø input data words treated equal.
   c. All logic functions.
   d. Internal lookahead carry with propagate and generate outputs.
2. Internal shift network.
   a. Left and right logic shift.
   b. Sign protect for arithmetic shift.
3. Versatile bus structure.
4. Master-slave accumulator for temporary storage.
5. Interfaces with MECL 10,000 register file circuits.
6. All necessary status outputs: overflow, zero detect, carry out, and sign bit.
7. Parity outputs for binary operations.
8. Full masking of Ø bus to A bus is provided in the latch/mask network.
9. Each part is 4 bits wide and the circuits can be operated in parallel to form any word size in increments of 4 bits.

M10800 LSI FAMILY DEVICES:

P/N	Description
MC10800	4-Bit ALU Slice
MC10801	Microprogram Control Function
MC10802	Timing Function
MC10803	Memory Interface Function

COMPATIBLE MOTOROLA MECL MEMORIES:

MCM10143	8 x 2 Multiport Register File
MCM10144	256 x 1 RAM
MCM10145	16 x 4 RAM
MCM10146	1024 x 1 RAM
MCM10147	128 x 1 RAM
MCM10149	256 x 4 PROM

COMPATIBLE LOGIC:

ECL 10,000: 100 Circuits, Industry-wide

ABSOLUTE MAXIMUM RATINGS (see Note 1)

RATING		SYMBOL	VALUE	UNIT
Supply Voltage (V_{CC} = 0)		V_{EE} V_{TT}	−8 to 0 −4 to 0	Vdc Vdc
Input Voltage (V_{CC} = 0)	Std Bus	V_{in} V_{in}	0 to V_{EE} Note 2	Vdc Vdc
Output Source Current	Cont Surge	I_o I_o	< 50 <100	mAdc mAdc
Storage Temp.		$T_{stg.}$	−55 to +150	°C
Junction Temp.		T_j	165	°C

NOTE: 1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device realiability.

NOTE: 2. Input voltage limit is V_{CC} to −2 Volts when the bus is used as an input and the output drivers are disabled.

5

SYSTEM OVERVIEW

Certain basic functional building blocks, as shown in Figure 1, are characteristic of high performance processors. These building blocks can be resolved into LSI circuits which, by proper use of control memory programming and circuit function select lines, will fit a wide range of system requirements. The Motorola M10800 family of LSI processor circuits is designed to provide these functional blocks and not limit the final system to any given system size or architecture.

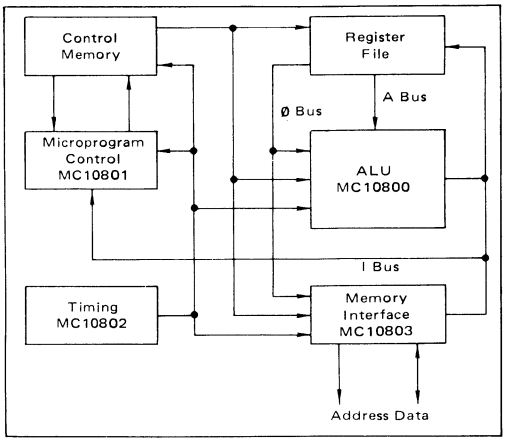
The ALU block in Figure 1 is filled by the MC10800 4-Bit ALU Slice. This circuit combines the mask logic, ALU, shift network, and accumulator to give a very powerful function set. In addition, the data routing paths and data I/0 ports allow numerous options when configuring a system. When designing with the MC10800 function set it is possible to accomplish in a single pass what would require mulitple passes with other ALU circuits.

In the M10800 Family, the register file has been made a separate block from the ALU, because modern systems use a wide range of register file sizes – varying between 4 and 256 working registers. With high speed MECL RAM and register file circuits available, the designer is permitted to specify the optimum register file size and configuration for his particular system. Storage registers are available in the MC10801 Microprogram Control Function and MC10803 Memory Interface Function for special purpose functions such as instruction register, status register, program counter, index register, and stack pointer.

Virtually all modern computers use a microprogrammed instruction set. Microprogramming permits emulating machines, updating systems by increasing capability, modifying systems to meet specific customer requirements, and designing to take advantage of existing software. The MC10801 Microprogram Control Function contains the logic needed to address and sequence through microprogram storage. Each MC10801 is 4 bits wide and can be operated in parallel for larger control memory address words. The necessary storage, logic, and I/0 is provided to generate next control memory address and handle status, branching, and interrupt functions.

One of the penalties normally paid to gain the advantages of microprogramming is system speed. Each processor instruction requires several microprogram steps. The Motorola M10800 LSI family makes use of MECL 10,000 circuit technology and interfacing to attain fast microprogram cycle times. In addition, other features of the family (such as a powerful ALU function set in the MC10800 and independent memory addressing in the MC10803), minimize the number of microprogram steps per system instruction. With the M10800 bipolar LSI family, it is possible to build fast microprogrammed systems which outperform dedicated hardwired systems using a slower technology.

FIGURE 1 – MICROPROGRAMMED PROCESSOR



The Control Memory block in Figure 1 is a separate section of the system, best selected by the designer. Any microprogram storage included on the LSI circuits results in design constraints. Microprogram storage can vary up to several thousand words, depending on system complexity, and is best built with individual MECL PROMs such as the MCM10149, or MECL RAMs such as the MCM10144 or MCM10146.

Any processor system must have access to external information from such sources as main memory, peripherals, and bulk storage. In the M10800 Family this chore is handled by the M10803 Memory Interface Function. This circuit is 4 bits wide and contains the necessary memory data and address storage. In addition, there are registers and an ALU for performing the various modes of memory addressing.

The MC10802 Timing Function ties the other function blocks together. This part provides the various clock phases as needed and makes it easy to interface to a manual test or control panel. As with other parts in the M10800 Family, the MC10802 is fully programmable for maximum system flexibility.

The Motorola M10800 circuits interface directly with all parts in the MECL 10,000 family. This provides a source for high speed ECL memories and interface circuits for MOS memories. It allows special hardware functions to be constructed for maximum system performance. MECL 10,000 MSI circuits can be used to multiplex status inputs for branch conditions, format priority interrupts, and build high speed array multipliers.

Versatility is a main point of the M10800 Family. The block diagram in Figure 1 is intended to illustrate the purpose of the various LSI functions and not restrict the designer to any particular system configuration or application.

PIN ASSIGNMENTS

Pin Designation	Pin Number	Description
A0	29	Data Bus A – LSB Input
A1	32	Data Bus A – NLSB Input
A2	34	Data Bus A – NMSB Input
A3	30	Data Bus A – MSB Input
ØB0	23	Output Bus – LSB I/O
ØB1	22	Output Bus – NLSB I/O
ØB2	21	Output Bus – NMSB I/O
ØB3	20	Output Bus – MSB I/O
IB0	13	Input Bus – LSB I/O
IB1	14	Input Bus – NLSB I/O
IB2	15	Input Bus – NMSB I/O
IB3	16	Input Bus – MSB I/O
AS0	37	Y Input Mux – Select Input
AS1	38	Y Input Mux – Select Input
AS4	39	Increment/Decrement by 2 – Select Input
AS2	40	X Input Mux – Select Input
AS3	35	X Input Mux – Select Input
AS5	33	Output Bus Control & A Input Mux – Select Input
AS6	31	Output Bus Control & A Input Mux – Select Input
AS10	41	Add/Subtract – Select Input
AS11	42	Binary/BCD – Select Input
AS12	43	Arithmetic/Logic Mode – Select Input
C_{in}	44	Carry Input
C_{out}	3	Carry Output
PG	5	Group Propagate Output
GG	4	Group Generate Output
OF	6	Overflow Output
PC	2	Parity of Carries Output
PR	10	Parity of Result Output
ZD	11	Zero Detect
AS7	45	Shift Network – Source Select Input
AS13	47	Shift Network – Function Select Input
AS14	46	Shift Network – Function Select Input
R4	9	Shift Network – MSB I/O
R-1	8	Shift Network – LSB I/O
AS9	19	Accumulator Mux & Input Bus Control – Select Input
AS15	18	Accumulator Mux & Input Bus Control – Select Input
AS8	28	Input Bus Driver – Enable Input
CLK	27	Accumulator – Clock Input
AS16 (LC)	26	Output Bus Latch – Clock Input
V_{EE}	1	–5.2 Volt Supply
V_{EE}	24	–5.2 Volt Supply
V_{TT}	25	–2.0 Volt Supply
V_{TT}	48	–2.0 Volt Supply
V_{CC}	12	Ground
V_{CC}	36	Ground
V_{CCO}	7	Ground
V_{CCO}	17	Ground

ARCHITECTURAL DESCRIPTION

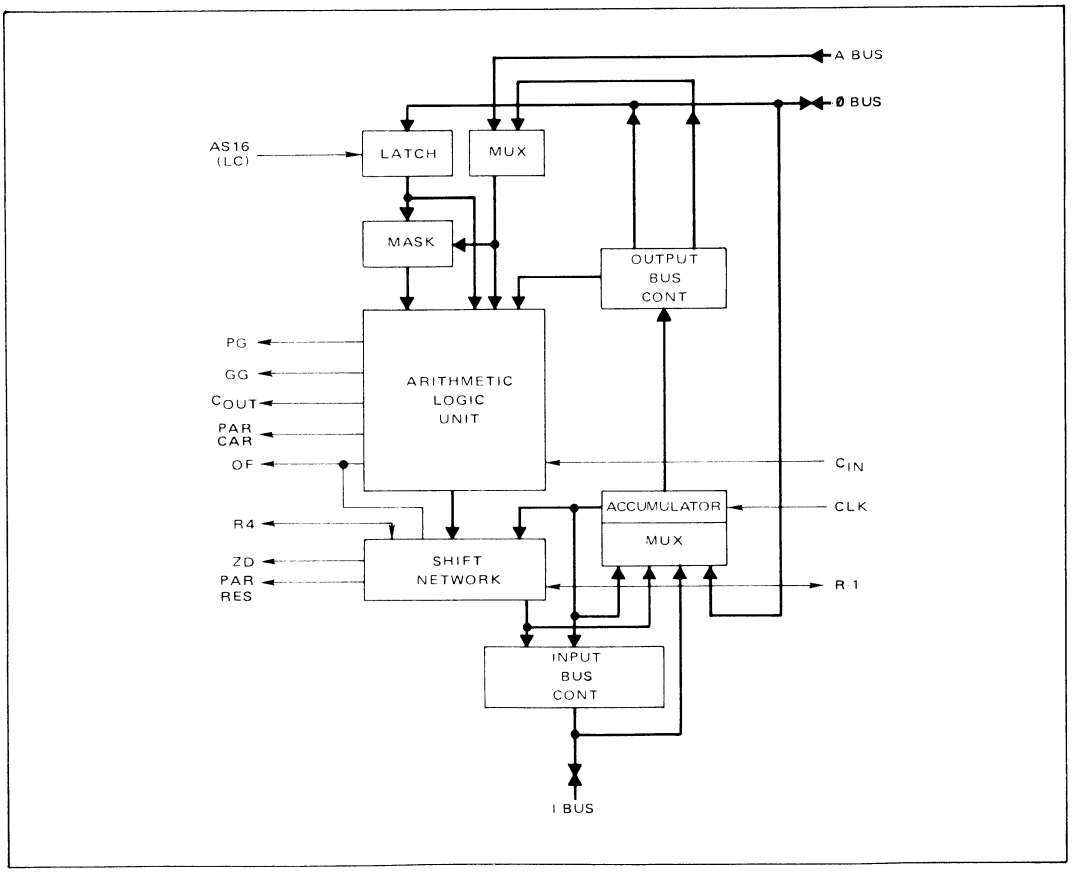
Data enters and exits the MC10800 4-Bit ALU Slice through the A bus, Output (ø bus), and Input (I bus) as shown in Figure 2. The ø bus and I bus are bidirectional, while the A bus is an input port only. These ports are each 4 bits wide requiring that MC10800s be operated in parallel for larger word lengths, single bit data paths C_{in}, C_{out}, R-1, and R4 are used to interconnect parallel MC10800s. The circuit contains two storage elements; the ø bus latch controlled by the latch clock (LC) and the accumulator controlled by the master clock (CLK). The remaining terminals in Figure 2 are status outputs and are used for second level look-ahead carry or for generation of processor condition codes. The individual blocks and I/O terminals in Figure 2 are described below.

Latch/Mask Network

The latch/mask network controls data to one input port of the Arithmetic Logic Unit. The holding latch is positioned to provide temporary storage for data entering through the Output Bus port. The latch clock input (LC) controls the latch operation. When not latched, data ripples through the latch and need not be clocked.

For microprocessor and microcontroller applications, it is desirable to be able to mask data entering a machine. The latch/mask network incorporates this feature. By using the mask select lines, it is possible to mask data on the Output Bus with the A Bus using the logic AND and logic OR functions.

FIGURE 2 – 4-BIT ALU SLICE – MC10800
DATA, STATUS AND CLOCK



Arithmetic Logic Unit

The Arithmetic Logic Unit (ALU) combined with the latch/mask network has the capability of perfoming logic operations, binary arithmetic, and BCD arithmetic on combinations of one, two, or three variables. These variables are the A bus, output bus latch, and accumulator. Variables are treated equally in both binary and BCD formats (A bus minus ø bus and ø bus minus A bus). BCD arithmetic operations are incorporated internally within the ALU and the BCD functions do not compromise system speed.

The ALU incorporates a 9's complement circuit to generate the necessary BCD complement function. The 9's complementer is used with BCD subtract and 9's complement instructions and the circuit is automatically enabled when these functions are selected.

The ALU section of the 4-Bit Slice provides the logic for overflow and carry out. Overflow provides the two's complement overflow of binary addition and subtraction. Overflow is also generated in the shift network and is the exclusive OR of the MSB and NMSB during a shift left operation. Carry out functions for both binary and BCD operations. If second level look-ahead carry is not used, the carry out of one 4-Bit Slice is connected to carry in of the following slice circuit for ripple carry.

The ALU generates the group propagate, group generate, and parity of carry outputs. Group propagate and generate are used for external look-ahead carry between 4-Bit Slice circuits. The propagate and generate outputs operate with both BCD and binary functions. Parity of carries is used for arithmetic error checking and is generated by the exclusive-ORing of C_{in}, carry from the LSB, carry from the NLSB, and carry from the NMSB.

Shift Network

The shift network following the ALU performs the data shift operations within the 4-Bit Slice. Select lines to the shift network control shift left, logic shift right, arithmetic shift right, and ripple through.

The arithmetic shift right provides sign protection for arithmetic shift operations. Only MSB is affected during an arithmetic shift right (towards the LSB), the most significant bit is repeated. R-1 and R4 input/outputs are brought out and are used for shift expansion when interconnecting 4-Bits Slice circuits. The zero detect is derived from the shift network outputs and detects the binary or BCD all zero state. Parity of results is also generated in the shift network. This output, used for parity checking, is generated by exclusive-ORing the shift outputs.

Input Bus Control

The input bus control manipulates the source of data to the Input Bus port. The input bus can receive data from either the shift network or the accumulator. In addition, this control circuit can inhibit data from being routed to the input bus. This allows the input bus to enter data into the accumulator or to be used for other system functions not related to the 4-Bit Slice.

Accumulator/Multiplexer

The master-slave accumulator provides for high speed iterative computer operations. These can include repeated add with accumulated sum, multiply, divide, and multiple shift operations. A multiplexer circuit feeds the accumulator from one of three possible sources as controlled by select lines. These sources are the results of the shift network, the input bus, or the output bus. A fourth condition inhibits the accumulator clock and stored data is retained. Data is entered on the rising (V_{OL} to V_{OH}) clock edge.

Output Bus Control

The output bus control section distributes the outputs of the accumulator to various points in the 4-Bit slice. Select lines route the accumulator to either the A input multiplexer or to the output bus. In addition, the accumulator can be routed to the ALU for mask and compare type operation. A fourth state of the output bus control inhibits the accumulator from going to any of the three above destinations.

A Input

The A input consists of four pins, A0, A1, A2, and A3 which serve as input data paths to the arithmetic logic unit. These inputs are designed to operate in a negative logic data format with a MECL V_{OL} being a logic 1. Because of the BCD functions, the 4-Bit Slice does not directly accept both positive and negative logic formats. The inputs are designated with A0 as the least significant of the 4 bits in the circuit and A3 as the most significant bit.

Output Bus

The output bus consits of four terminals, øB0 through øB3, which function as both data inputs and data outputs. As with the A input, the output bus pins are in negative logic and øB0 is the least significant bit within the part. The output bus when used as an input is routed to the holding latch, and accumulator multiplexer. As an output port, these terminals are used to connect data in the accumulator to the output bus as shown in Figure 2.

Input Bus

The input bus consists of four terminals, IB0 through IB3, which function as both data inputs and data outputs. As with the A buffer and the output bus, the input bus pins are in negative logic and IB0 is the least significant bit within the part. The input bus when used as an input is routed to the accumulator. As an output port, these terminals are used to connect data from either the accumulator or shift network results to the input bus as shown in Figure 2.

Carry In

Carry in, C_{in}, is used to interconnect 4-Bit Slice circuits in a system. For ripple carry, carry in is connected to carry out of the preceding 4-Bit Slice. When look-ahead carry is incorporated, the carry in is connected to the look-ahead carry logic.

Carry in is only used for arithmetic operations and has no effect on any logic operation. The carry in functions for both binary and BCD arithmetic operations. Carry in operates in a negative logic mode with V_{OL} being a logic 1.

Carry Out

Carry out, C_{out}, signals that the calculated value within the ALU has exceeded the maximum capacity of the four ALU output lines. Any binary total over count 15 (1111) or BCD total over count 9 (1001) results in a carry out. When ripple carry is used, carry out is connected to carry in of the following 4-Bit Slice.

Shift Interconnects R-1 and R4

R-1 and R4 are provided to interconnect 4-Bit Slice circutis for shift operations. R-1 and R4 function as both inputs and outputs depending on the shift direction. For a shift left (toward the MSB) R-1 is an input for the R0 bit and R4 is an output for the MSB. For a logic shift right R-1 is an output for the LSB and R4 is an input to R3. MSB is also connected to R4 during a no shift operation and during an arithmetic shift right. This allows R4 to be used as a status output for sign detection. When not used as outputs, the internal drivers for R-1 and R4 are held at a negative logic 1 so the shift interconnects can function as inputs using the MECL emitter dot. See Table 1.

TABLE 1

SHIFT OPERATION	I/O FUNCTION	
	R-1	R4
Shift Left	Shift Input	Shift Output
No Shift	Not Used	MSB Output
Logic Shift Right	Shift Output	Shift Input
Arithmetic Shift Right	Shift Output	MSB Output

Group Propagate and Group Generate

The group propagate, PG, and group generate, GG, outputs are used in conjunction with external look-ahead carry logic for faster system operation. Using this technique, the carry in signals to the 4-Bit Slice circuits are generated faster than with ripple carry. The propagate output goes to the logic 1 when the maximum number value occurs on the ALU outputs. This is count 15 (1111) for binary functions and count 9 (1001) for BCD functions. For binary functions, generate occurs with any value of 16 (10000) or larger and for BCD functions any number value of 10 (10000) or larger.

Group propagate and group generate outputs are used only for arithmetic operations in a system to allow faster generation of carry in signals. They serve no function for ALU logic operations.

Overflow OF

Overflow is used only with two's complement arithmetic and shows that the maximum system word or byte value has been exceeded. In a system, only the overflow output from the 4-Bit Slice operating on the most significant bits of the data word is used.

In addition to overflow caused by an ALU operation, it is possible to have overflow as a result of a shift left (toward the MSB) in the shift network. This happens when the sign bit is changed as a result of the shift left operation.

Normally the overflow of the ALU and shift network are ORed together so that either causes an overflow condition. The exception to this occurs when the accumulator is routed to the shift network inputs. At this time, the ALU overflow is inhibited from the OF output. Overflow is not used with BCD arithmetic.

Zero Detect ZD

Zero detect signals the all zero condition (0000) at the output of the shift network. Zero detect functions for logic operations, binary arithmetic, and BCD arithmetic operations within the ALU. By having the zero detect at the output of the shift network, it is possible to detect zero status after a shift has been performed. Zero detect is defined by the following equation:

$$ZD = \overline{R0} \cdot \overline{R1} \cdot \overline{R2} \cdot \overline{R3}$$

where $\overline{R0}$ through $\overline{R3}$ are the internal outputs from the shift network.

Parity Outputs PAR CAR and PAR RES

Parity bits are used to detect system errors in data handling. With a single parity bit, it is possible to detect a single bit error or any combination of an odd number of bit errors.

For parity checking binary arithmetic operations, two parity points are generated in the MECL 4-Bit Slice. These are parity of carries (PAR CAR) and parity of results (PAR RES). Parity of carries is the parity of the individual bit carries internal to the slice.

$$\text{PAR CAR} = \text{C IN} \oplus \text{C0} \oplus \text{C1} \oplus \text{C2}$$

Parity of results is the parity of the individual result bits at the output of the shift network.

$$\text{PAR RES} = \text{R0} \oplus \text{R1} \oplus \text{R2} \oplus \text{R3}$$

Accumulator Clock CLK

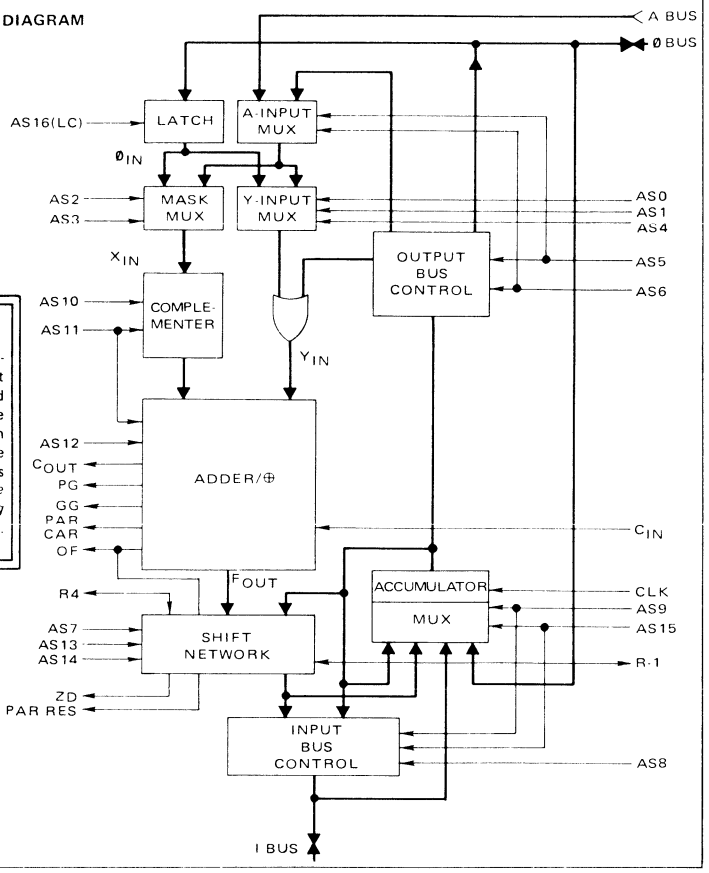
The accumulator is constructed of master-slave flip flops and must be clocked to change stored data. As is characteristic of MECL flip flops, the accumulator is clocked on the positive going (V_{OL} to V_{OH}) clock edge. At that time, data on the accumulator inputs is transferred to the accumulator outputs.

Signals on the accumulator inputs can change at any time with the clock input at either logic state and not change accumulator outputs. The only restriction on changing accumulator inputs is during the set up and hold time near the positive going clock edge.

Latch Clock AS16

Latch clock AS16 controls the storage of data in the holding latch on the output bus. When the latch clock is at V_{IH} data ripples through the latch, interconnecting the output bus with the ALU inputs. When AS16 is at V_{OL} data is stored in the latch and latch outputs are not affected by any changes in information on the output bus.

FIGURE 3 – FUNCTIONAL BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Seventeen select lines AS0 through AS16 control the flow of data within the MC10800 4-Bit Slice and determine the arithmetic, logic, and shift operations performed on the data. The following information describes the operation of these select lines, then shows how these select lines combine to perform the various MC10800 functions. *The truth tables are expressed in negative logic with V_{OL} being a logic 1 and V_{OH} a logic 0,* Figure 3 applies.

SELECT LINE OPERATION

Y Input Mux Select Inputs AS0 and AS1

AS0 and AS1 control the source of data to the Y-Input mux of the ALU. These select lines allow selection of either the A Input Mux, the output bus, all logic 0 or all logic 1 bits. Table 2 illustrates the operation of these two select lines.

The ALU Y input is also the port for entering accumulator data into the ALU. This is accomplished by setting AS0 and AS1 to a logic 0 and enabling the accumulator with AS5 and AS6 as described in Table 4 and Table 5.

TABLE 2

AS0	AS1	ALU Y INPUT
0	0	LOGIC 0
0	1	OUTPUT BUS LATCH
1	0	A INPUT MUX
1	1	LOGIC 1

Increment/Decrement by 2 Select Input AS4

Select line AS4 is used to give the MECL 4-Bit Slice an increment or decrement by 2 function capability. When this input is held at a logic 1 (V_{OL}) it has no effect on the circuit. When at a logic 0, it is used with AS0 and AS1 to force a code 0010 (plus 2) or 1110 (minus 2) on the Y input of the ALU. In a system, this input would normally be used only with the 4-Bit Slice operating on the least significant bits in a word or byte. However, other slice locations could also be used to add such constants as 2, 32, 34, 512, 544, 546, etc. AS4 operation with AS0 and AS1 is shown in Table 3.

TABLE 3

AS4	AS0	AS1	ALU Y INPUT
1	TABLE 2		DETERMINED BY AS0, AS1
0	0	0	PLUS 2 (0010)
0	1	1	MINUS 2 (1110)

The combinations AS0•$\overline{AS1}$•$\overline{AS4}$ and $\overline{AS0}$•AS1•$\overline{AS4}$ are not normally used. AS0•$\overline{AS1}$•$\overline{AS4}$ results in Y0 = logic 0, Y1 = logic 1, Y2 = A2, and Y3 = A3. $\overline{AS0}$•AS1•$\overline{AS4}$ results in Y0 = logic 0, Y1 = logic 1, Y2 = ØB2, and Y3 = ØB3.

Output Bus Control and A Input Mux Select Inputs AS5 & AS6

Select lines AS5 and AS6 control the destination of the accumulator output. The accumulator can be routed to five locations in the MECL 4-Bit Slice. Three locations, the output bus, the ALU A input, the ALU ACC input are controlled by AS5 and AS6. A fourth state of AS5 and AS6 inhibits the accumulator from any of these three destination. Other destinations for the accumulator are the input bus as described in the section on AS9 and AS15 and to the shift network inputs as controlled by AS7. (Table 9 and Table 11).

When drivers to the output bus are not enabled by AS5 and AS6, they are forced to a logic 1 (V_{OL}) so this bus can take advantage of the MECL emitter dotting. The accumulator input to the ALU requires a logic 0 when not used as a data input.

AS5•$\overline{AS6}$ enables the accumulator on the Ø Bus. The MC10800 can simultaneously output the accumulator contents onto the system Ø Bus and input the accumulator contents to the Ø Bus port of the ALU. Only external data on the Ø Bus is ANDed to the accumulator contents when AS5•$\overline{AS6}$ is selected.

The MC10800 A bus terminals are input only and AS5 and AS6 select either the A bus inputs or the accumulator to the ALU A input.

Logic State $\overline{AS5}$•AS6 operates in conjunction with AS0 and AS1 to enter data into the ALU Y input. The output of the Y-input mux is logically ORed to the accumulator ALU input. Table 5 illustrates the operation of these select lines.

TABLE 4

AS5	AS6	Ø BUS	A IN MUX	ALU
0	0	Ø BUS	A BUS	0
0	1	Ø BUS	A BUS	ACC
1	0	ACC•Ø BUS	A BUS	0
1	1	Ø BUS	ACC	0

TABLE 5

$\overline{AS5}$•AS6	AS0	AS1	ALU Y INPUT
0	TABLE 2		Determined by AS0, AS1
1	0	0	ACCUMULATOR
1	0	1	ACC OR Ø BUS
1	1	0	ACC OR A MUX
1	1	1	LOGIC 1

X Input Mux Select Inputs AS2 and AS3

Select lines AS2 and AS3 control the data path to the other ALU input (X input). These lines can select either the A bus or the output bus. In addition, AS2 and AS3 provide masking capability within the 4-Bit Slice. These select lines control the logic functions – (A bus OR Ø bus) and (A bus AND Ø bus). This allows any bit or bits to be masked to either a logic 1 or 0 with masking information on either the A bus or Ø bus terminals. The advantage of doing masking prior to the ALU is that it allows single pass mask and compare within the 4-Bit Slice. AS2 and AS3 operation is shown in Table 6.

TABLE 6

AS2	AS3	ALU X INPUT
0	0	A MUX AND Ø BUS
0	1	Ø BUS
1	0	A MUX
1	1	A MUX OR Ø BUS

Add/Subtract and Binary/BCD Select Inputs AS10 and AS11

Select line AS10 and add/subtract control enables the complementer. During the add mode the X_{in} data is passed directly through, and during the subtract mode the data is complemented. The complement function is also modified by AS11. The 9's complement is generated for BCD subtract, and data is inverted (1's complement) for binary subtract.

If the ALU is in the logic (Exclusive-OR) mode the complementer is used to selectively invert the X_{in} data. AS11 should be set to the binary mode, and AS10 is used to control inversion of the data.

TABLE 7

AS10	AS11	FUNCTION
0	0	SUBTRACT BCD (9's COMPLEMENT)
0	1	SUBTRACT BINARY (INVERT)
1	0	ADD BCD
1	1	ADD BINARY

Arithmetic/Logic Mode Select Input AS12

AS12 is the mode control for the 4-Bit adder. This input determines if the function performed in the ALU is an arithmetic or logic operation. The logic mode disables the carry between bits and the function performed is the Exclusive-OR of the two inputs to the adder.

TABLE 8

AS12	MODE
0	LOGIC (Exclusive-OR)
1	ARITHMETIC

Shift Network Source Select Input AS7

AS7 controls the information source to the shift network. The MECL 4-Bit Slice is designed to allow shifting data from the accumulator or from the ALU. The accumulator shift operation is useful in multiply and divide add/shift routines. AS7 follows the truth table shown in Table 9.

TABLE 9

AS7	SHIFT NETWORK SOURCE
0	ACCUMULATOR
1	ALU

Shift Network Function Select Inputs AS13 and AS14

AS13 and AS14 control the operation of the shift network following the ALU in the 4-Bit Slice. The four possible operations are: no shift (straight through), shift left one bit, logic shift right one bit, and arithmetic shift right one bit. The truth table for AS13 and AS14 is shown in Table 10.

TABLE 10

AS13	AS14	SHIFT OPERATION
0	0	SHIFT LEFT
1	0	NO SHIFT
0	1	LOGIC SHIFT RIGHT
1	1	ARITHMETIC SHIFT RIGHT

Shift left shifts each bit at the shift network inputs (F inputs) one bit left (toward the MSB). This operation provides the function for both arithmetic and logic shift left. Logic shift right shifts each bit at the F inputs one bit right (toward the LSB). This shift mode is used in all 4-Bit Slice circuits for logic shift right and all except the slice circuit handling the most significant bit of a word or byte for an arithmetic shift right. During an arithmetic right shift, it is necessary to have sign protection for a number expressed in 2's complement or 1's complement notation. This is accomplished by repeating the most significant bit during and arithmetic shift right.

R-1 is an input for shift left and an output for both logic and arithmetic shift right. This pin is not used for no shift. R4 is an input for logic shift right and an output for all other AS13 and AS14 operations. This feature allows R4 to function as a sign bit status output on the MC10800 having the sign bit as the MSB within the part.

Accumulator Mux & Input Bus Control Select Inputs AS9 & AS15

Select lines AS9 and AS15 perform two functions in the MECL 4-Bit Slice. One is to control the source of data to the accumulator, the other to control the source of data to the input bus drivers. The accumulator can store data from three independent points in the 4-Bit Slice. These are the input bus, the output bus, and the shift network outputs. A fourth condition on AS9 and AS15 feeds the accumulator back on itself so the accumulator clock is effectively disabled. This permits storage of data in the accumulator with a continuous system clock entering the slice circuit. The clock disable state of AS9 and AS15 is designed so that only the clock can load information into the accumulator and the accumulator status cannot be altered by the select lines alone.

AS9 and AS15 route either the accumulator or the shift network outputs to the input bus drivers. When the results of the shift network are gated to the accumulator, the accumulator is the source of data to the input bus drivers. For all other combinations AS9 and AS15, the shift network outputs are gated to the bus drivers. The accumulator clock can be disabled when reading the accumulator to the shift network and using the shift network as a feedback path. Table 11 illustrates the operation of AS9 and AS15.

TABLE 11

AS9	AS15	INPUT TO ACCUMULATOR	INPUT BUS SOURCE
0	0	SHIFT RESULTS	ACCUMULATOR
0	1	OUTPUT BUS	SHIFT RESULTS
1	0	INPUT BUS	SHIFT RESULTS
1	1	ACCUMULATOR	SHIFT RESULTS

Input Bus Driver Enable Input AS8

AS8 inhibits and enables the input bus driver circuits. When this select line is at a logic 1 (V_{OL}) the input bus drivers are enabled and data from either the shift network or the accumulator is routed to the input bus. A logic 0 on AS8 disables the input bus drivers so the input bus port can be used to input data or so the input bus can route data independent of the 4-Bit Slice in a system. When disabled the input bus drivers assume a logic 1 state (V_{OL}). Forcing the outputs low permits the use of MECL emitter dotting on the system input bus. The truth table for AS8 is shown in Table 12.

TABLE 12

AS8	INPUT BUS
0	DISABLE OUTPUTS
1	ENABLE OUTPUTS

Accumulator Clock Input CLK and Output Bus Latch Clock Input – AS16

Data is entered into the accumulator on the rising edge of the clock signal. The data source is selected by AS9 and AS15. Latch clock AS16 controls the storage of data in the holding latch on the output bus. When AS16 is a logic 0 (V_{IH}) data ripples through the latch. When AS16 is a logic 1 data is stored in the latch and the latch outputs are not affected by information changes on the output bus. Table 13 is the truth table for AS16.

TABLE 13

AS16	LATCH OPERATION
0	ENABLED
1	LATCHED

ALU LOGIC OPERATION FUNCTION SET

The output bus latch, the A input multiplexer, and the accumulator are sources of data to the ALU. Following the various truth tables of the given select lines a full set of logic operation can be performed in the ALU.

The equivalent block diagram of the ALU for logic operations is shown in Figure 4. The adder is set to the logic mode (AS12 = 0), therefore, F_{OUT} is the Exclusive-OR of selected sources X and Y. The complementer is programmed as a conditional inverter (AS11 = 1) dependent on AS10. The X source is selected by inputs AS2 and AS3. The Y source is selected by AS0 and AS1 (AS4 = 1) and OR-ed with the accumulator (selected by $\overline{AS5}$•AS6). A selected logic function set is shown in Table 14.

Other functions and select line combinations are possible with many redundant operations. Other conditions can be determined from previous truth tables.

FIGURE 4 – BLOCK DIAGRAM OF ALU LOGIC OPERATION

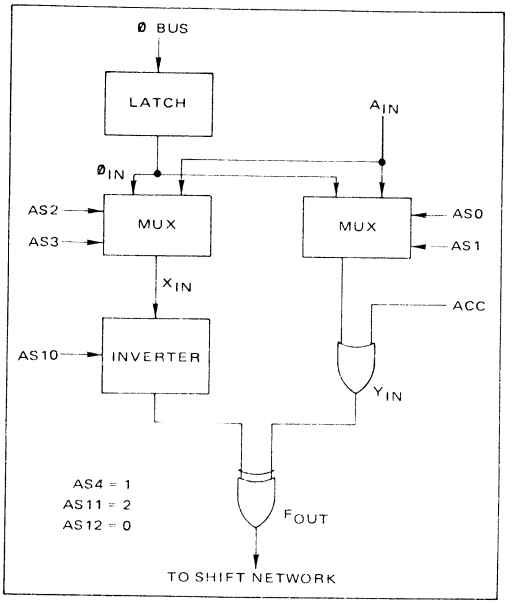
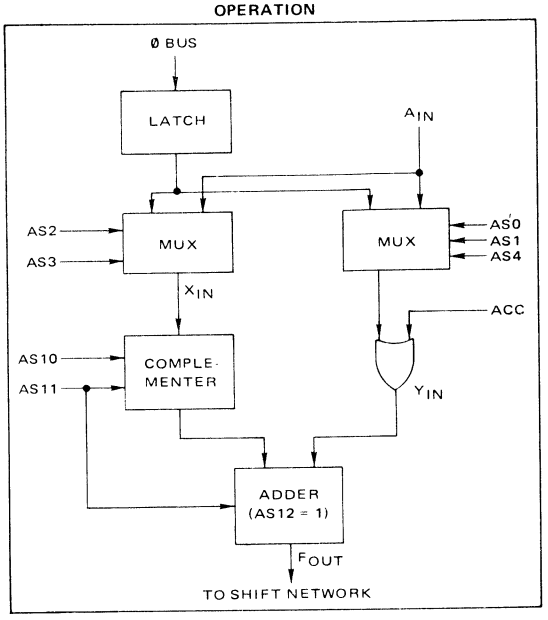


TABLE 14

Y MUX		X MUX		INV	ACC	FUNCTION
AS0	AS1	AS2	AS3	AS10	$\overline{AS5}$•AS6	
0	1	0	1	1	0	LOGIC 0
0	0	1	0	1	0	A
0	0	0	1	1	0	Ø
0	0	1	0	0	0	$\overline{A}$
0	0	0	1	0	0	$\overline{Ø}$
0	0	1	1	1	0	A + Ø
0	1	0	0	0	0	A + $\overline{Ø}$
1	0	0	0	0	0	$\overline{A}$ + Ø
0	0	0	0	1	0	A • Ø
0	1	1	1	1	0	A • $\overline{Ø}$
0	1	0	0	1	0	$\overline{A}$ • Ø
0	1	1	0	1	0	A ⊕ Ø
0	1	1	0	0	0	$\overline{A \oplus Ø}$
0	0	0	0	0	0	$\overline{A \cdot Ø}$
0	0	1	1	0	0	$\overline{A + Ø}$
0	1	0	1	0	0	LOGIC 1
1	0	1	0	1	1	ACC • $\overline{A}$
0	1	0	1	1	1	ACC • $\overline{Ø}$
1	0	1	0	0	1	$\overline{ACC}$ + A
0	1	0	1	0	1	$\overline{ACC}$ + Ø
0	0	1	0	1	1	ACC ⊕ A
0	0	1	0	0	1	ACC ⊕ $\overline{A}$
0	0	0	1	1	1	ACC ⊕ Ø
0	0	0	1	0	1	ACC ⊕ $\overline{Ø}$
0	0	0	0	1	1	ACC ⊕ A•Ø
0	0	0	0	0	1	ACC ⊕ $\overline{A}$•$\overline{Ø}$
0	0	1	1	1	1	ACC ⊕ A+Ø
0	0	1	1	0	1	ACC ⊕ $\overline{A}$+$\overline{Ø}$

+ = Logical Inclusive OR
• = Logical AND
⊕ = Logical Exclusive OR

FIGURE 5 – BLOCK DIAGRAM OF ALU ARITHMETIC OPERATION



ALU ARITHMETIC OPERATION FUNCTION SET

The block diagram for arithmetic operation is similar to logic operation, however, the complementer and adder go to arithmetic mode. Select input AS12 is set to logic 1 for adder operation, however, AS4 is now used for increment/decrement by 2 and AS11 selects the binary or BCD operation.

The various arithmetic functions in the 4-Bit Slice are determined by the choice of operands to the adder. Most binary functions have a BCD equivalent, however, operands for BCD functions should be valid BCD characters.

Table 15 shows a selected arithmetic function set. Similar to the logic function set other combinations of select lines and operations are possible. These can be generated as needed by the previous truth tables.

TABLE 15

Y MUX		X MUX		±2	COMPLE-MENT	ACC	BINARY FUNCTION (PLUS C_{IN})	BCD FUNCTION (PLUS C_{IN})
AS0	AS1	AS2	AS3	AS4	AS10	$\overline{AS5 \cdot AS6}$	AS11 = 1	AS11 = 0
1	0	0	1	1	1	0	A PLUS Ø	A PLUS Ø
1	0	0	1	1	0	0	A PLUS $\overline{Ø}$	A PLUS 9's COMP. Ø
0	1	1	0	1	0	0	Ø PLUS $\overline{A}$	Ø PLUS 9's COMP. A
0	0	1	0	1	1	0	A	A
0	0	0	1	1	1	0	Ø	Ø
0	0	1	0	1	0	0	$\overline{A}$	9's COMP. A
0	0	0	1	1	0	0	$\overline{Ø}$	9's COMP. Ø
1	1	1	0	1	1	0	–1 PLUS A	*
1	1	0	1	1	1	0	–1 PLUS Ø	*
1	1	1	0	0	1	0	–2 PLUS A	*
1	1	0	1	0	1	0	–2 PLUS Ø	*
0	0	1	0	0	1	0	+2 PLUS A	+2 PLUS A
0	0	0	1	0	1	0	+2 PLUS Ø	+2 PLUS Ø
1	0	1	0	1	1	0	A PLUS A	A PLUS A
0	1	0	1	1	1	0	Ø PLUS Ø	Ø PLUS Ø
0	0	1	0	1	1	1	ACC PLUS A	ACC PLUS A
0	0	0	1	1	1	1	ACC PLUS Ø	ACC PLUS Ø
0	0	1	0	1	0	1	ACC PLUS $\overline{A}$	ACC PLUS 9's COMP. A
0	0	0	1	1	0	1	ACC PLUS $\overline{Ø}$	ACC PLUS 9's COMP. Ø
0	0	0	0	1	1	1	ACC PLUS A·Ø	ACC PLUS A·Ø
0	0	0	0	1	0	1	ACC PLUS $\overline{A \cdot Ø}$	ACC PLUS 9's COMP. A·Ø
0	0	1	1	1	1	1	ACC PLUS A + Ø	*
0	0	1	1	1	0	1	ACC PLUS $\overline{A + Ø}$	*

*Not Defined in BCD

DATA ROUTING FUNCTION SET

Data routing in the MECL 4-Bit Slice covers the routing of data to and from both the shift network and accumulator. Data routing is controlled by select lines AS5, AS6, AS7, AS8, AS9, and AS15. AS5 and AS6 control the output destination of accumulator data, AS7 determines the source of data to the shift network, and AS8 enables and disables the input bus drivers. AS9 and AS15 control the source of data to both the accumulator and input bus drivers. Table 16 shows the truth table for AS7, AS8, AS9, and AS15.

The first four columns show all select line states. The fifth column shows the input source to the accumulator as controlled by AS9 and AS15. The possible accumulator inputs are: (1) ACC which is accumulator feedback on itself for accumulator clock disable. (2) IB which connects the input bus to the accumulator inputs, (3) ØB which connects the output bus to the accumulator inputs, and (4) RES which connects the results of shift network to the accumulator input. The sixth column shows the two possible sources of input data to the shift network. These are from the accumulator (ACC) for accumulator shift operations, and from the ALU function outputs (F). The final column in the table shows the status of the input bus drivers. A logic 0 on AS8 disables the driver circuits so this part can be used to input data or for other system functions not related to the 4-Bit Slice. When enabled, the input bus port will output information from the accumulator or from the results of the shift network.

TABLE 16

				FUNCTION		
AS7	AS8	AS9	AS15	ACC SOURCE	SHIFT SOURCE	INPUT BUS
0	0	0	0	RES	ACC	DISABLE
0	0	0	1	ØB	ACC	DISABLE
0	0	1	0	IB	ACC	DISABLE
0	0	1	1	ACC	ACC	DISABLE
0	1	0	0	RES	ACC	ACC
0	1	0	1	ØB	ACC	RES
0	1	1	0	IB	ACC	RES
0	1	1	1	ACC	ACC	RES
1	0	0	0	RES	F_{OUT}	DISABLE
1	0	0	1	ØB	F_{OUT}	DISABLE
1	0	1	0	IB	F_{OUT}	DISABLE
1	0	1	1	ACC	F_{OUT}	DISABLE
1	1	0	0	RES	F_{OUT}	ACC
1	1	0	1	ØB	F_{OUT}	RES
1	1	1	0	IB	F_{OUT}	RES
1	1	1	1	ACC	F_{OUT}	RES

RECOMMENDED OPERATING CONDITIONS – MC10800

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage (V_{CC} = 0 Volts)	V_{TT} V_{EE}	−1.9 to −2.2 −4.68 to −5.72	Vdc Vdc
Operating Temp. (Functional)	T_A	−30 to +85	°C
Output Drive	—	50Ω to −2.0 Vdc	—
Maximum Clock Input Rise and Fall Time (20% to 80%)	t_r, t_f	10	ns
Minimum Clock Pulse Width	PW	5	ns

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{TT}
−30°C	−0.890	1.890	1.205	1.500	5.2	−2.0
+25°C	−0.810	1.850	1.105	1.475	5.2	−2.0
+85°C	0.700	1.825	1.035	1.440	5.2	−2.0

Characteristic	Symbol	Pin Under Test	MC10800 TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{TT}	(V_{CC}) Gnd
Power Supply Drain Current	I_{EE} I_{TT}	1, 24 25, 48				195 180	240 199			mAdc					1, 24	25, 48	12, 36 7, 17
Input Current	I_{inH}	23 31 27					65 350 435			μAdc	23 31 27						
	I_{inL}	31			0.5					μAdc		31					
Logic "0" Output Voltage	V_{OH}	13 10	1.060 1.060	−0.890 −0.890	−0.960 −0.960		−0.810 −0.810	−0.890 −0.890	−0.700 −0.700	Vdc Vdc	8, 26, 46, 47 *						
Logic "1" ** Output Voltage	V_{OL}	13 10	−1.940 −1.890	1.675 1.675	−1.900 −1.850		−1.650 −1.650	1.875 1.825	1.615 1.615	Vdc Vdc	26, 46, 47 *, 47						
Logic "0" Threshold Voltage	V_{OHA}	13 10	−1.080 −1.080		−0.980 −0.980			−0.910 0.910		Vdc Vdc	26, 46, 47 *		8	47			
Logic "1" Threshold Voltage	V_{OLA}	13 10		1.655 1.655			−1.630 −1.630		1.595 1.595	Vdc Vdc	26, 46, 47 *		47	8			

* V_{IH} on pins 19, 26, 30, 31, 32, 33, 34, 35, 37

** The bi-directional outputs are specified at −1.90 volts for V_{OL} min

RECOMMENDED OPERATING CONDITIONS – MC10800M

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage (V_{CC} = 0 Volts)	V_{TT} V_{EE}	−1.9 to −2.2 −4.68 to −5.72	Vdc Vdc
Operating Temp. (Functional)	T_J max	+150°C	°C
Output Drive	–	100 Ω to − 2.0 Vdc	–
Maximum Clock Input Rise and Fall Time (20% to 80%)	t_r, t_f	10	ns
Minimum Clock Pulse Width	PW	5	ns

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The ciruict is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 100-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{TT}
−55°C	−0.830	−1.920	−1.255	−1.510	−5.2	−2.0
+25°C	−0.720	−1.850	−1.105	−1.475	−5.2	−2.0
T_J +150°C	−0.580	−1.820	−1.000	−1.400	−5.2	−2.0

Characteristic	Symbol	Pin Under Test	MC10800M TEST LIMITS −55°C Min	−55°C Max	+25°C Min	+25°C Typ	+25°C Max	+150°C Min	+150°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{TT}	(V_{CC}) Gnd
Power Supply Drain Current	I_{EE} I_{TT}	1, 24 25, 48				195 180	240 199			mAdc					1, 24	25, 48	12, 36 7, 17
Input Current	I_{inH}	23 31 27					65 350 435			µAdc	23 31 27						
	I_{inL}	31			0.5					µAdc		31					
Logic "0" Output Voltage	V_{OH}	13 10	−1.080 −1.080	−0.830 −0.830	−0.930 −0.930		−0.720 −0.720	−0.825 −0.825	−0.580 −0.580	Vdc Vdc	8, 26, 46, 47 *						
Logic "1" ** Output Voltage	V_{OL}	13 10	−1.970 −1.920	−1.655 −1.655	−1.900 −1.850		−1.620 −1.620	−1.870 −1.820	−1.545 −1.545	Vdc Vdc	26, 46, 47 *, 47						
Logic "0" Threshold Voltage	V_{OHA}	13 10	−1.100 −1.100		−0.950 −0.950			−0.845 −0.845		Vdc Vdc	26, 46, 47 *		8 47				
Logic "1" Threshold Voltage	V_{OLA}	13 10		−1.635 −1.635			1.600 1.600		−1.525 −1.525	Vdc Vdc	26, 46, 47 *		47	8			

* V_{IH} on pins 19, 26, 30, 31, 32, 33, 34, 35, 37

** The bi-directional outputs are specified at −1.90 volts for V_{OL} min

SETUP AND HOLD TIMES (NANOSECONDS OVER TEMPERATURE RANGE).

Input	Path	Mode	MC10800		MC10800M	
			Setup (Max)	Hold (Max)	Setup (Max)	Hold (Max)
A Bus	→ A MUX → MASK MUX → COMP → ALU → SHIFT → ACC	Arith Subtract	38.0	−15.0	40.0	−15.0
A Bus	→ A MUX → Y MUX → ALU → SHIFT → ACC	Logical	19.0	−5.0	21.0	−5.0
ϕ Bus	→ LATCH → MASK MUX → COMP → ALU → SHIFT → ACC	Arith Subtract	38.0	−15.0	40.0	−15.0
ϕ Bus	→ LATCH → Y MUX → ALU → SHIFT → ACC	Logical	20.0	−5.0	22.0	−5.0
ϕ Bus	→ ACCUMULATOR	Direct	7.0	+5.0	7.0	+5.0
I βus	→ ACCUMULATOR	Direct	7.0	+5.0	7.0	+5.0
AS0, 1	Y MUX → ALU → SHIFT → ACC	Arith Add	32.0	−15.0	35.0	−15.0
AS4	ALU → SHIFT → ACC	Logical	15.0	0.0	18.0	0.0
AS3	MASK MUX → COMP → ALU → SHIFT → ACC	Arith Subtract	36.0	−17.0	38.0	−17.0
AS2	MASK MUX → ALU → SHIFT → ACC	Logical (No Comp)	22.0	−5.0	24.0	−5.0
AS5, 6	ALU → SHIFT → ACC		20.0	−5.0	20.0	−5.0
AS7	SHIFT INPUT MUX → SHIFT → ACCUMULATOR	Direct	10.0	+5.0	10.0	+5.0
AS9, 15	ACCUMULATOR INPUT MUX → ACC	Direct	8.0	+7.0	8.0	+7.0
AS10	COMP → ALU → SHIFT → ACC	Arith	35.0	−15.0	37.0	−15.0
AS11	ALU → SHIFT → ACC	Arith	21.0	−2.0	21.0	−2.0
AS12	ALU → SHIFT → ACC		28.0	−10.0	30.0	−10.0
AS12	ALU → SHIFT → ACC		14.0	+2.0	14.0	+2.0
AS13, 14	SHIFT NETWORK → ACCUMULATOR	Direct	16.0	+5.0	16.0	+5.0
CIN	→ ALU → SHIFT → ACC	Arith	19.0	+2.0	21.0	+2.0
R-1, R4	SHIFT NETWORK → ACCUMULATOR	Direct	8.0	+5.0	8.0	+5.0
ϕ Bus	→ LATCH (AS16 – LATCH CLOCK)	Direct	5.0	+6.0	5.0	+6.0

PROPAGATION DELAYS (NANOSECONDS)

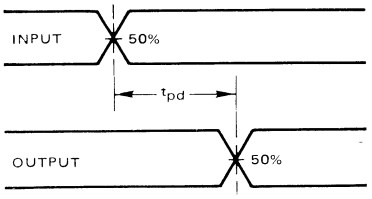
Input	Path Via	Path Mode	Path Function	Output	MC10800 -30°C T_A Typ	MC10800 -30°C T_A Max	MC10800 +25°C T_A Typ	MC10800 +25°C T_A Max	MC10800 +85°C T_A Typ	MC10800 +85°C T_A Max	MC10800M -55°C T_A Max	MC10800M +25°C T_A Typ	MC10800M +25°C T_A Max	MC10800M +150°C T_J Typ
A Bus ØBus	ALU	Arith	Subtract	I Bus	30.0	39.0	32.0	41.0	37.0	49.0	41.0	32.0	41.0	60.0
				P_G, G_G	16.0	21.0	17.5	21.0	20.0	27.0	21.0	17.5	21.0	35.0
				C_{OUT}	18.0	22.0	19.0	23.0	22.0	28.0	23.0	19.0	23.0	36.0
				OF, ZD R-1, R4	27.0	37.0	29.5	39.0	34.0	44.0	39.0	29.5	39.0	56.0
				PC, PR	27.0	34.0	29.0	36.0	34.0	41.0	36.0	29.0	36.0	53.0
C_{IN}	ALU	Arith	Addition	I Bus	15.0	18.5	16.0	19.5	19.0	24.5	19.5	16.0	19.5	33.0
				C_{OUT}	5.0	7.0	5.5	7.5	6.0	8.5	7.5	5.5	7.5	11.0
				OF, ZD R-1, R4	12.5	16.0	13.5	17.0	15.5	19.0	17.0	13.5	17.0	26.0
				PC, PR	13.5	18.0	14.5	19.0	17.0	23.0	19.0	14.5	19.0	30.0
AS0 AS1 AS2 AS3 AS4 AS5 AS6 AS10 AS11 AS12	ALU	Arith	Subtract Accumulator	I Bus	36.0	43.0	38.5	46.5	47.0	64.0	46.5	38.5	46.5	80.0
				PG, GG	23.0	30.0	24.0	30.0	30.0	38.0	30.0	24.0	30.0	48.0
				C_{OUT}	24.0	32.0	26.0	32.0	31.5	39.0	32.0	26.0	32.0	49.0
				OF, ZD R-1, R4	33.0	43.0	36.0	46.0	47.0	60.0	46.0	36.0	46.0	72.0
				PC, PR	33.0	40.0	35.0	42.0	44.0	57.0	42.0	35.0	42.0	70.0
AS16	ALU	Arith	Subtract	I Bus	33.0	40.0	35.0	43.0	41.0	51.0	43.0	35.0	43.0	62.0
				PG, GG	20.0	25.0	21.0	26.0	25.0	32.0	26.0	21.0	26.0	40.0
				C_{OUT}	21.5	26.0	23.0	27.5	26.5	33.0	27.5	23.0	27.5	41.0
				OF, ZD R-1, R4	30.5	39.0	33.0	42.0	38.0	47.0	42.0	33.0	42.0	60.0
				PC, PR	30.5	36.0	33.0	39.0	38.0	47.0	39.0	33.0	39.0	57.0
R-1 R4	Shift	Shift Left Shift Right	–	I Bus	7.0	8.5	7.5	9.0	9.0	13.0	9.0	7.5	9.0	18.0
AS7 AS13 AS14	Shift	Shift Left Shift Right	–	I Bus	10.0	16.0	10.0	16.0	12.5	18.0	16.0	10.0	16.0	27.0
AS9 AS15	Direct	Shift ACC	–	I Bus	8.0	11.0	8.5	11.5	10.0	13.5	11.5	8.5	11.5	18.0
AS8	Direct	Enable Disable	–	I Bus	5.5	8.5	6.0	8.5	7.5	10.0	8.5	6.0	8.5	25.0
AS5 AS6	Direct	Enable Disable	–	ØBus	7.0	9.5	7.5	9.5	10.0	17.0	9.5	7.5	9.5	28.0
CLK	A Bus ALU	Arith	Subtract Accumulator	I Bus	38.5	48.0	41.0	51.0	47.0	57.0	51.0	41.0	51.0	67.0
				PG, GG	26.0	36.0	27.5	38.0	31.0	43.0	38.0	27.5	38.0	52.0
				C_{OUT}	27.5	38.0	29.0	40.0	32.5	45.0	40.0	29.0	40.0	55.0
				OF, ZD R-1, R4	37.0	41.0	39.0	43.0	44.5	49.0	43.0	39.0	43.0	60.0
				PC, PR	36.5	44.0	39.0	46.0	44.0	55.0	46.0	39.0	46.0	68.0
CLK	ALU	Arith	Add Accumulator	I Bus	34.5	45.0	36.5	47.0	42.5	58.0	47.0	36.5	47.0	69.0
CLK	Shift	AS7 = 0	Multiple Shift	I Bus	13.0	17.5	14.0	18.5	16.0	21.0	18.5	14.0	18.5	27.0
				OF, ZD R-1, R4	14.0	18.0	14.5	19.0	16.0	23.0	19.0	14.5	19.0	30.0
				PC, PR	15.0	20.0	16.0	21.0	18.0	24.0	21.0	16.0	21.0	30.0
CLK	Direct	–	Acc to I Bus	I Bus	8.0	11.0	8.5	11.0	10.0	13.0	11.0	8.5	11.0	22.0

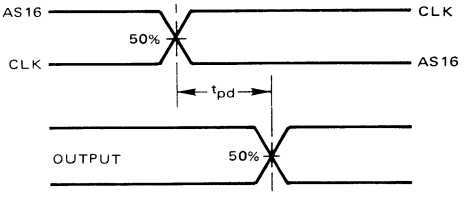
PROPAGATION DELAYS (NANOSECONDS) (continued)

Input	Path: Via	Path: Mode	Path: Function	Output	MC10800: -30°C T_A Typ	MC10800: -30°C T_A Max	MC10800: +25°C T_A Typ	MC10800: +25°C T_A Max	MC10800: +85°C T_A Typ	MC10800: +85°C T_A Max	MC10800M: -55°C T_A Max	MC10800M: +25°C T_A Typ	MC10800M: +25°C T_A Max	MC10800M: +150°C T_J Typ
CLK	Direct	–	Acc to ØBus	ØBus	8.5	12.0	9.0	12.0	10.0	13.0	12.0	9.0	12.0	22.0
ØBus	ALU (Mask)	Logic	Without Complement	I Bus	23.0	32.0	25.0	35.0	30.0	45.0	35.0	25.0	35.0	60.0
CLK	A Bus (Mask)	Logic	Without Complement	I Bus	33.0	42.0	35.0	43.0	40.0	47.0	43.0	35.0	43.0	62.0
CLK	A Bus (Mask)	Logic	With Complement	I Bus	34.5	44.0	37.0	47.0	42.0	55.0	47.0	37.0	47.0	65.0
CLK	A Bus (Y Mux)	Logic	Without Complement	I Bus	31.0	39.0	33.0	41.0	37.0	44.0	41.0	33.0	41.0	57.5
Output Rise and Fall Time (20% – 80%)				All	3.0	5.0	3.5	5.5	4.0	6.0	5.5	3.5	5.5	7.5

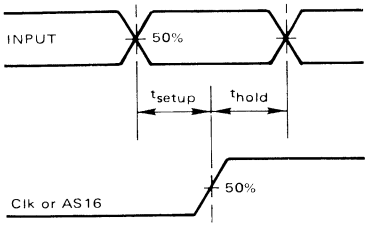
SWITCHING WAVEFORMS

PROPAGATION DELAYS





SETUP AND HOLD



TEST PROCEDURE:

a) Establish setup time with long t_{hold}.

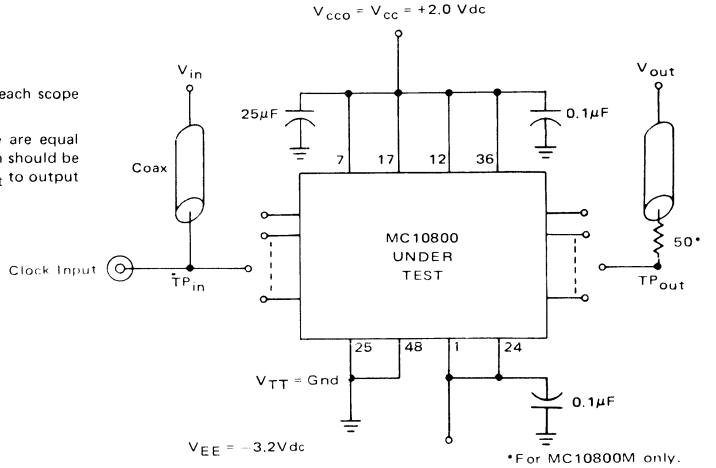
b) Keeping the leading edge of the input constant (t_{setup}) vary the trailing edge of the input to determine t_{hold}.

NOTE: t_{setup} and t_{hold} as defined are positive. Internal delays in the data path may result in a shift of the data waveform to the left, with respect to the clock, resulting in negative hold times.

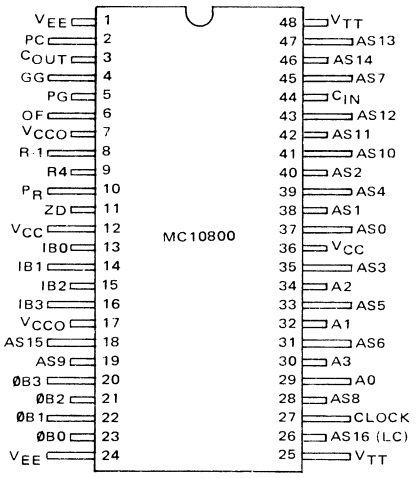
SWITCHING TIME TEST CIRCUIT

50 ohm termination to ground located in each scope channel input.

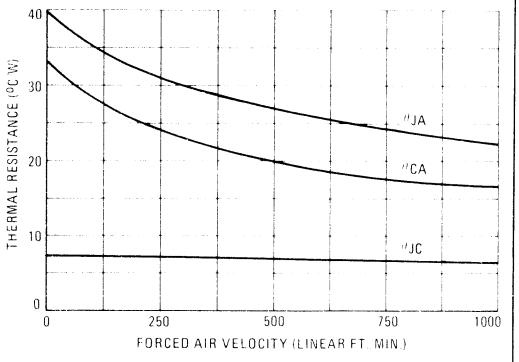
All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be ≈¼ inch from TP_{in} to input pin and TP_{out} to output pin.



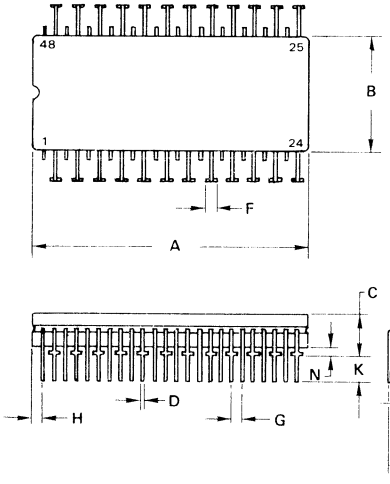
PIN ASSIGNMENT



THERMAL CHARACTERISTICS (TYPICAL)



PACKAGE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.57	5.59	0.180	0.220
D	0.38	0.53	0.015	0.021
F	1.14	1.40	0.045	0.055
G	1.27 BSC		0.050 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.54	3.30	0.100	0.130
L	15.24 BSC		0.600 BSC	
M	--	7°	--	7°
N	0.51	1.52	0.020	0.060
P	20.32 BSC		0.800 BSC	

Case 725-01

A socket for the QUIL package is available from ELECTRONIC MOLDING CORPORATION. (Part number 7178-295-5)

QUIL is a trademark of Motorola Inc.

MOTOROLA Semiconductors

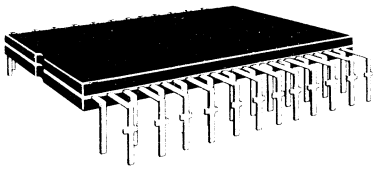
MC10801

INTRODUCTION

The MC10801 Microprogram Control Function is an LSI building block for digital processor systems. This circuit controls machine operations by generating the addresses and sequencing pattern for microprogram control storage. The MC10801 is compatible with a wide range of control memory sizes and organizations. Each part is 4 bits wide and can be connected in parallel for larger memory addresses. Maximum system flexibility is maintained with 5 separate data ports.

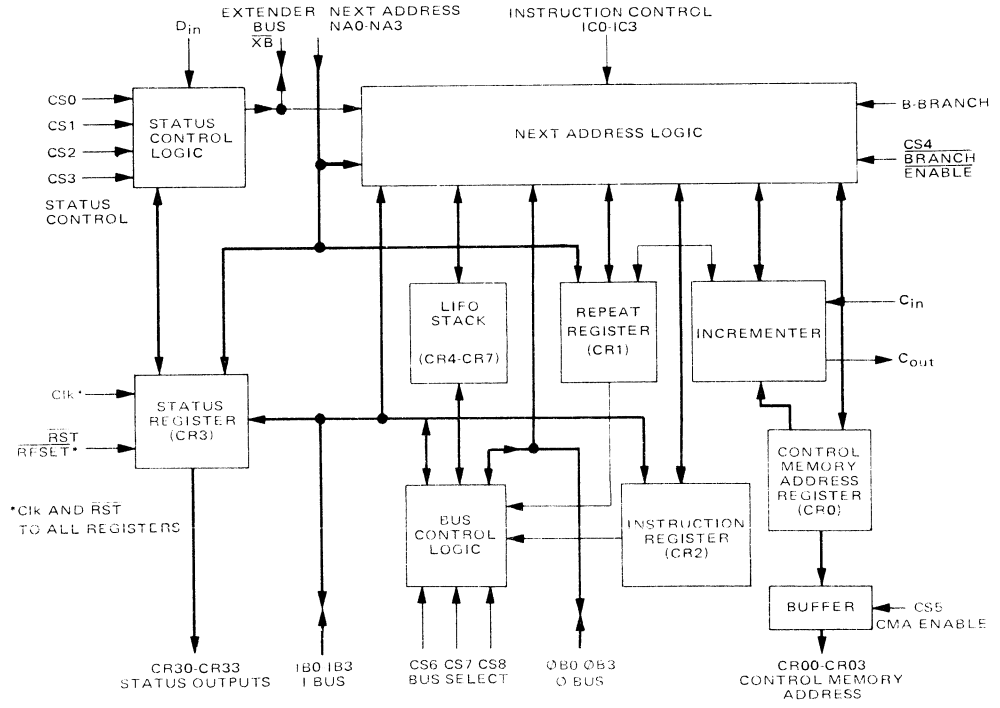
The Microprogram Control Function as shown in the block diagram below contains a control memory address register CR0, multipurpose registers CR1-CR3, an incrementer, a subroutine LIFO, and the associated next address, status, and bus control logic in a single MECL Bipolar LSI circuit. Nine select (CS) lines and four instruction inputs (IC) control all operations within the part.

MECL — LSI MICROPROGRAM CONTROL FUNCTION



CASE 725-01

Microprogram Control Function BLOCK DIAGRAM—MC10801



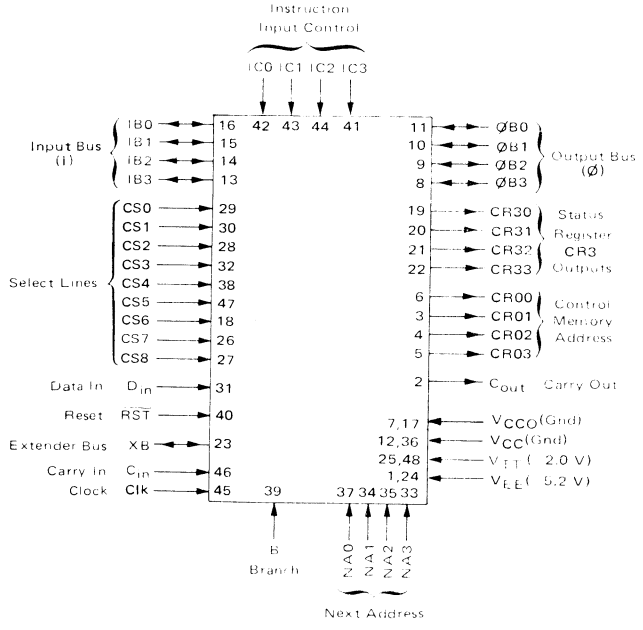
DS9497
(Formerly ADI 410)

TABLE OF CONTENTS

IMPORTANT FEATURES

1. 16 microprogram sequencing instructions including:
   a. Increment
   b. Direct jumps
   c. Conditional jumps
   d. Subroutining
   e. Conditional Subrouting
2. 4-bit registers expandable with parallel MC10801 circuits.
   a. Microprogram address register — CR0
   b. Repeat register — CR1
   c. Instruction register — CR2
   d. Status register — CR3
3. Expandable 4 X 4 push-pop stack for nesting subroutine — CR4-CR7.
4. Branch inputs for conditional operations and multiway branching
5. Address masking on special instructions.
6. Repeat logic for repeating subroutines or single instructions.
7. All registers are of edge triggered master-slave design.
8. Fully compatible with the MECL 10,000 family.

INPUT/OUTPUT DIAGRAM—MC10801



ABSOLUTE MAXIMUM RATINGS (see Note 1)

RATING		SYMBOL	VALUE	UNIT
Supply Voltage (V_{CC} = 0)		V_{EE} V_{TT}	−8 to 0 −4 to 0	Vdc Vdc
Input Voltage (V_{CC} = 0)	Std Bus	V_{in} V_{in}	0 to V_{EE} Note 2	Vdc Vdc
Output Source Current	Cont Surge	I_o I_o	< 50 <100	mAdc mAdc
Storage Temp.		$T_{stg.}$	−55 to +150	°C
Junction Temp.		T_j	165	°C

NOTE: 1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

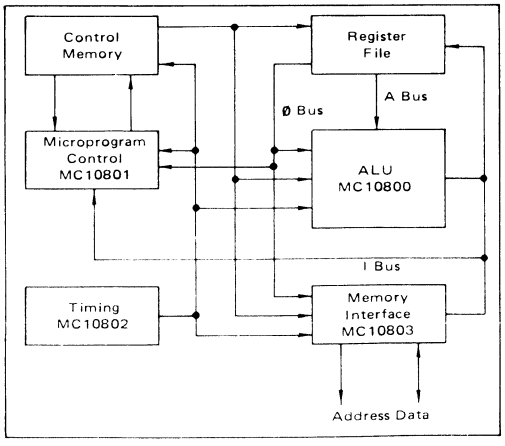
NOTE: 2. Input voltage limit is V_{CC} to −2 Volts when the bus is used as an input and the output drivers are disabled.

SYSTEM OVERVIEW

The Motorola M10800 family of LSI processor circuits has been partitioned into key building block elements as shown in Figure 1. The LSI circuits can be interconnected and programmed for a wide range of processor system applications. Combinations of the various circuits allow expansion to any required data word length or control memory size. Multiple I/O ports on each circuit provide maximum data flow flexibility. The M10800 LSI family is designed to provide functional system blocks without limiting a final system size or architecture.

The M10800 system is designed around a microprogrammed concept for greatest versatility. Microprogramming permits emulating existing machines or software, updating systems by adding more capability, or modifying systems to meet specific customer requirements. The microprogram is contained in the control memory block of Figure 1. Depending on system requirements, this memory can vary from a few hundred words to several thousand. The size and organization of this block is controlled by the system designer and is constructed with MECL PROMs such as the MCM10149, or MECL RAMs such as the MCM10144 or MCM10146.

FIGURE 1 – MICROPROGRAMMED PROCESSOR



In a microprogrammed processor the information for executing a machine function (macroinstruction) is contained within the control memory. Control memory outputs go to the Register File, ALU, and Memory Interface blocks in Figure 1 and control the specific function performed by each section of the processor. The number of control memory steps (microinstructions) required to execute a macroinstruction is determined by complexity of the instruction. For example, a simple register to register add can require only one or two microinstructions, while a more complex multiply or floating point arithmetic calculation requires several control memory words addressed in the proper sequence.

The heart of a microprogrammed system is the microprogram control logic. This block in Figure 1 holds the present control memory word address and controls the sequencing to execute processor operations. Within the Motorola M10800 family, the MC10801 Microprogram Control Function performs this important task. Each circuit is four bits wide and parallel combinations adapt to any required control memory size. A set of sixteen instructions address the MC10801 and control the sequencing of the microprogram storage. Powerful branch and subroutine instructions increase system performance and minimize the amount of control memory required to build a system. The sixteen instructions ease the burden of writing a microprogram by expressing program flow in a manner familiar to assembly language programmers.

Versatility is a key word to describe each circuit in the Motorola M10800 family. The block diagram in Figure 1 and the examples in this data sheet are intended to illustrate ways to use these LSI parts and do not restrict the designer to any particular system configuration or application.

PIN ASSIGNMENTS

Pin Designation	Pin Number	Description
IC0	42	Instruction Control Input
IC1	43	Instruction Control Input
IC2	44	Instruction Control Input
IC3	41	Instruction Control Input
IB0	16	Input Bus – LSB I/O
IB1	15	Input Bus – NLSB I/O
IB2	14	Input Bus – NMSB I/O
IB3	13	Input Bus – MSB I/O
ØB0	11	Output Bus – LSB I/O
ØB1	10	Output Bus – NLSB I/O
ØB2	9	Output Bus – NMSB I/O
ØB3	8	Output Bus – MSB I/O
NA0	37	Next Address – LSB Input
NA1	34	Next Address – NLSB Input
NA2	35	Next Address – NMSB Input
NA3	33	Next Address – MSB Input
CR00	6	Control Memory Address – LSB Output
CR01	3	Control Memory Address – NLSB Output
CR02	4	Control Memory Address – NMSB Output
CR03	5	Control Memory Address – MSB Output
CR30	19	Status Register CR3 Output
CR31	20	Status Register CR3 Output
CR32	21	Status Register CR3 Output
CR33	22	Status Register CR3 Output
CS0	29	Status Register Control – Select Input
CS1	30	Status Register Control – Select Input
CS2	28	Status Register Control – Select Input
CS3	32	Status Register Control – Select Input
CS4	38	Branch Line – Select Input
CS5	47	Control Memory Address – Enable Input
CS6	18	Ø Bus/I Bus Control – Select Input
CS7	26	Ø Bus/I Bus Control – Select Input
CS8	27	Ø Bus/I Bus Control – Select Input
C_{in}	46	Carry Input
C_{out}	2	Carry Output
D_{in}	31	Data Input to CR3
$\overline{B}$	39	Branch Input
$\overline{XB}$	23	Extender Bus
$\overline{RST}$	40	Reset Input
Clk	45	Clock Input
V_{EE}	1	–5.2 Volt Supply
V_{EE}	24	–5.2 Volt Supply
V_{TT}	25	–2.0 Volt Supply
V_{TT}	48	–2.0 Volt Supply
V_{CC}	12	Ground
V_{CC}	36	Ground
V_{CCO}	7	Ground
V_{CCO}	17	Ground

ARCHITECTURAL DESCRIPTION

The MC10801 Microprogram Control Function is composed of 8 master slave registers, CR0 through CR7, as shown in Figure 2. Additional gates, multiplexers, and a next address logic block transfer information to and from these registers. Five 4-bit data ports (CR0, CR3, NA, I Bus, and Ø Bus) are available to enter and output address information. In addition, three single line terminals (B, $\overline{XB}$, and D_{in}) provide status inputs for decisions within the part. Each of the eight registers fills an important function in the storage and generation of control memory addresses. The individual registers and data transfer paths in Figure 2 are described below.

CR0 – CONTROL MEMORY ADDRESS REGISTER

Register CR0 holds the present microprogram control memory address and its outputs are gated to package pins CR00 through CR03. In a system these outputs address the control memory storage block. The next address logic block in Figure 2 generates next address information to the CR0 register inputs. A positive clock edge loads the new control memory address into CR0 which in turn selects the next microinstruction.

NEXT ADDRESS LOGIC

The next address logic block performs 16 sequence instructions as selected by the instruction control lines IC0 through IC3 inputs. These 16 control instructions, see Table 1, determine the source of control memory address information within each MC10801. Possible sources are CR1, CR2, CR4, NA inputs, I Bus, Ø Bus, and the incrementer. During each microcycle the next address block generates a new control memory address in parallel with other processor functions, such as the ALU. Detailed information on the 16 MC10801 instructions follows in the Functional Description section of this data sheet.

FIGURE 2 – FUNCTIONAL BLOCK DIAGRAM

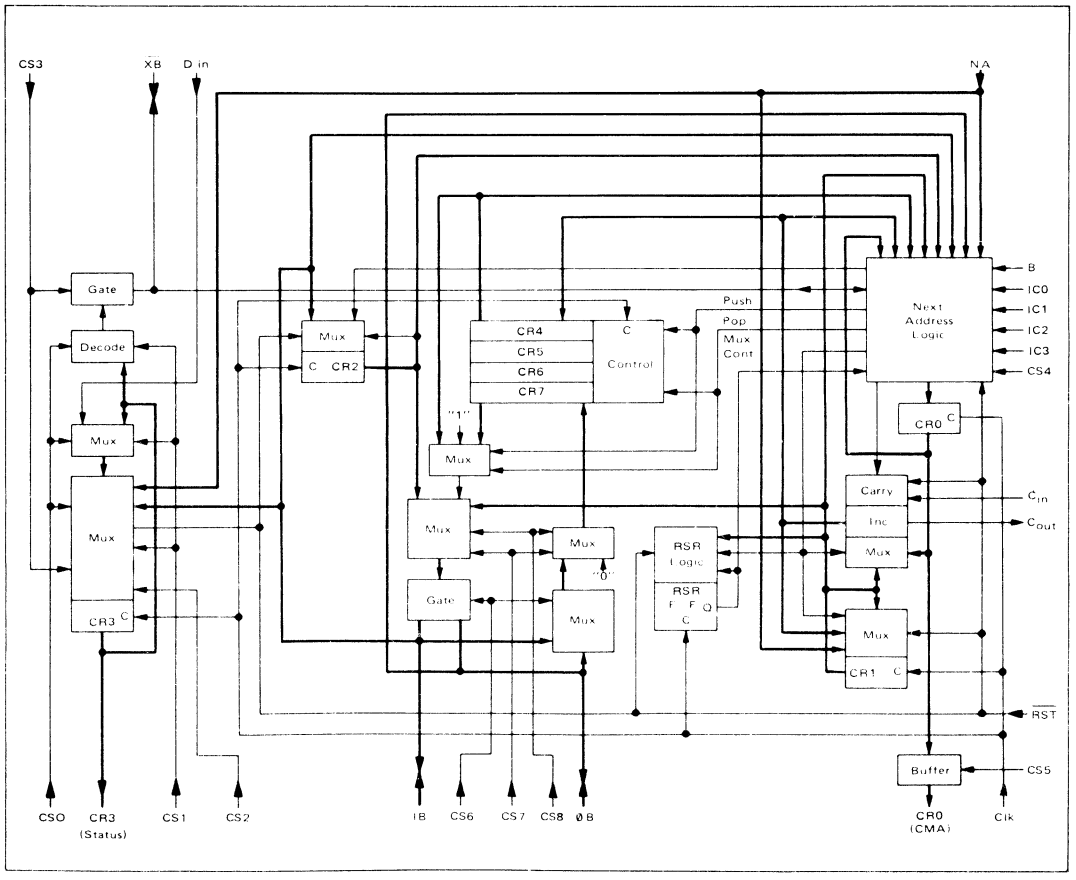


TABLE 1
MC10801 CONTROL INSTRUCTIONS

INC	– Increment
JMP	– Jump to N.A. Inputs
JIB	– Jump to I Bus
JIN	– Jump to I Bus and Load CR2
JPI	– Jump to Primary Instruction (CR2)
JEP	– Jump to External Port (Ø Bus)
JL2	– Jump to N.A. Inputs and Load CR2
JLA	– Jump to N.A. Inputs and Load Address into CR1
JSR	– Jump to Subroutine
RTN	– Return from Subroutine
RSR	– Repeat Subroutine (Load CR1 from N.A. Inputs)
RPI	– Repeat Instruction
BRC	– Branch to N.A. Inputs on Condition; otherwise Increment
BSR	– Branch to Subroutine on Condition; otherwise Increment
ROC	– Return from Subroutine on Condition; otherwise Jump to N.A. Inputs
BRM	– Branch and Modify Address with Branch Inputs (Multiway Branch)

CR1 – REPEAT REGISTER

Register CR1 is primarily designed to be an index counter for repeating single microinstructions or repeating subroutines. This repeat feature is important for multiple shift, multiply, and divide machine instructions. To perform a microprogram repeat sequence, the repeat count is first loaded into CR1 from the NA inputs with a RSR-Repeat Subroutine instruction (Table 1). Each time the selected microinstruction or subroutine is executed, CR1 is automatically incremented. Upon reaching the final repeat count the MC10801 continues to the next microprogram instruction.

A second function performed by CR1 is a control memory address save register. In this mode the present control memory address in CR0 is transferred to CR1 on a JLA-Jump and Load Address instruction (Table 1). At a later time it is possible to return to the stored address by transferring CR1 back to CR0 on a RPI-Repeat Instruction command.

The operation of CR1 is controlled by the next address logic. Possible input sources are the NA inputs, the incrementer, and CR0. CR1 outputs are routed to either CR0, to the incrementer, or to a Bus output.

CR2 – INSTRUCTION REGISTER

Register CR2 is used primarily as an instruction or op code storage register. After fetching a machine instruction, the control memory starting address can be stored in CR2. It can then be used later by transferring the contents of CR2 through the next address logic to the control memory address register CR0. As with register CR1, the operation of CR2 is controlled by the instruction inputs IC0 – IC3 and the next address logic. The I Bus is the source for CR2 and is loaded on either a JIN or JL2 instruction (Table 1). Information is transferred from CR2 to CR0 on a JPI-Jump to Primary instruction.

CR2 is not limited to an instruction register and can be used anytime it is desirable to store a control memory address location for future use. For example, CR2 can store an interrupt vector which may be loaded into CR0 as needed.

CR3 – STATUS REGISTER

Register CR3 is normally used as a status register for storing flag conditions. This 4-bit register can be parallel loaded from either the NA or I Bus inputs. In addition, any single CR3 bit can be set or cleared from the D_{in} input. The CR3 outputs are continuously available on the CR30 to CR33 package pins. The CR3 status information may be used in conjunction with other external information for generating branch conditions.

Any single CR3 bit can be selected and gated onto the $\overline{XB}$ extender bus line. $\overline{XB}$ goes to the next address logic to control branch decisions. When MC10801's are operated in parallel, the $\overline{XB}$ line is common to every part. Therefore, branch decisions can be made independent of which MC10801 circuit contains the selected status bit. The operation of CR3 with respect to the I Bus, NA inputs, D_{in}, and $\overline{XB}$ is controlled by select lines CS0, CS1, CS2, and CS3.

Another use for CR3 is to extend the control memory address. This is accomplished by organizing the control memory in a word-page format. The word address is contained in CR0 and the page address in CR3. With two MC10801's each page can be 256 words (8 CR0 bits) and 16 pages may be addressed with 4 CR3 bits or 256 possible pages using all 8 CR3 bits.

A third use for CR3 is to store all or part of the instruction operation code. In this manner, individual op code bits could be selected onto the $\overline{XB}$ line and tested for secondary decode decisions.

CR4 – CR7 LIFO STACK

Registers CR4 through CR7 are connected as a last-in-first-out (LIFO) stack for nesting subroutines within microprogram. When jumping to a subroutine, the return destination is automatically pushed onto the top of the LIFO (CR4). When returning from subroutine, CR4 is loaded into the control memory address register CR0.

With 4 registers it is possible to nest subroutines up to 4 deep within the LIFO. If additional stack depth is required CR1 can be used as a fifth location or CR7 can be expanded to any length through the I Bus or O Bus ports to additional MECL MSI circuits.

Reading CR7 via the I Bus or Ø Bus during a push of the LIFO stack provides a means for testing when the stack is full. Logic "0" bits are normally stuffed into the bottom of the stack on a "pop" or read operation. Therefore, any information in CR7 would indicate the stack is full.

Push and pop stack operations are controlled by the IC0 – IC3 inputs and the next address logic. In addition, select lines CS6, CS7, and CS8 route information to and from the LIFO via the I Bus and Ø Bus ports.

INCREMENTER

The 4-bit incrementer is used in several of the Table 1 microprogram control instructions. One is the INC-Increment command which linearly steps through a microprogram. A second function is to increment CR1 when it is used as an index counter for repeating microinstructions or subroutines as described in the earlier CR1 section. Increment is also used with the JSR-Jump to Subroutine, BSR-Branch to Subroutine, and JLA-Jump and Load Address commands to generate the proper return address. Operation of the incrementer is controlled by the IC0 – IC3 code and the C_{in} input.

The incrementer is expanded with the carry in (C_{in}) and carry out (C_{out}) terminals when MC10801 circuits are operated in parallel. The carry out of one MC10801 is connected directly to carry in of the circuit handling the next most significant control memory address bits. Carry out of the most significant bit is not required for count operation, but it can be used to signify maximum count value at the incrementer inputs.
Carry in to the least significant MC10801 is connected to a logic "1" for the increment operation. This input is normally hard wired, but in some applications can be system controlled to override the incrementer.

RSR LOGIC AND RSR FLIP FLOP

The repeat subroutine (RSR) logic and flip flop blocks in Figure 2 provide a means for setting the MC10801 in an instruction repeat sequence as described in the previous CR1 section. The RSR flip flop is automatically set when a repeat constant is loaded into CR1 with a RSR-Repeat Subroutine instruction. It is cleared when CR1 reaches the final repeat count. By monitoring the RSR flip flop status, the MC10801 can decide when to perform microinstruction repeats. Additional details of the RSR flip flop operation are explained in the following Functional Description section.

CLK – CLOCK

All registers in the MC10801 Microprogram Control Function are composed of master-slave flip flops and must be clocked to change stored data. A common clock is routed directly to all eight registers. As is characteristic of MECL flip flops, the registers are clocked on the positive going (V_{OL} to V_{OH}) clock edge. At that time data present on the register inputs is stored in the register and is available at the register outputs. Signals on the register inputs can change at any time, with the clock input at either logic state, and not change the register outputs. The only restriction on changing register inputs is during the set up and hold time near the positive going clock edge.

$\overline{RST}$ – RESET

The $\overline{RST}$ input is held at MECL V_{OL} during normal system operation. However, by forcing this input to the MECL V_{OH} level, it is possible to reset all registers in the MC10801. Reset operates in conjunction with the clock and therefore is a synchronous reset. Reset is accomplished in the following sequence. CR0, CR1, CR2, and CR3 are reset on the first clock pulse. The LIFO is connected to the incrementer to which carry-in is inhibited. The LIFO is also forced to a push mode during reset. Therefore, a maximum of five clock pulses reset all MC10801 registers in the following sequence: CR0/CR1/CR2/CR3, CR4, CR5, CR6, CR7.

FUNCTIONAL DESCRIPTION

MICROPROGRAM SEQUENCE CONTROL INSTRUCTIONS IC0-IC3

The MC10801 generates the microprogram address sequencing from 16 control instructions which are encoded on the IC0 – IC3 inputs. Each control instruction determines the data source for the next microprogram control memory address. This next address information is then stored in register CR0 on a positive going clock signal.
The 16 sequence control instructions are each described in Table 2. Table 2 lists these instructions and shows the associated mnemonics, binary select codes, and register transfers. Several instructions require making decisions on the status of the branch (B), extender bus ($\overline{XB}$), RSR flip flop output (RSQ), or select line CS4. Both decision alternatives are given for these instructions.

INC – Increment

The increment command routes the present contents of CR0 through the incrementer, adds C_{in}, and multiplexes the result (CR0 plus C_{in}) to the CR0 register inputs. As with all control instructions, the new address is loaded on a positive clock transition. This instruction is used to linearly step through the microprogram memory. When MC10801s are operated in parallel, C_{in} of a more significant device is connected to C_{out} of the previous MC10801. The least significant C_{in} is normally left floating at a logic "1".

JMP – Jump to Next Address

The JMP command provides for an unconditional jump to another control memory address. The jump destination is directly supplied on the NA inputs, which are normally feedback from control memory. A clock transition transfers address data from the NA inputs to register CR0.

FUNCTIONAL DESCRIPTION

Four instruction control inputs, IC0 – IC3, and nine select lines, CS0 – CS8, control the flow of data within the MC10801 Microprogram Control Function. The following information describes programming these inputs to perform the various circuit functions. *All truth tables are expressed in negative logic with V_{OL} being a logic 1 and V_{OH} a logic 0.*

TABLE 2[5]

MNEM	CODE IC3	IC2	IC1	IC0	DESCRIPTION	RESET $\overline{RST}$	BRANCH OR REPEAT CONDITION[2]	REGISTER AND FLIP FLOP OUTPUTS [4] V_{OL} → V_{OH} CR0[7]	CR1	CR2	LIFO STACK CR4 – CR7[6]	RSQ[3]
X	X	X	X	X	RESET CONDITION	0	X	0	0	0	"PUSH" CR0 TO STACK	0
INC	1	1	0	0	INCREMENT	1	X	CR0 plus C_{in}	–	–	–	–
JMP	0	0	1	0	JUMP TO NEXT ADDRESS	1	X	NA	–	–	–	–
JIB	1	0	0	0	JUMP TO I BUS	1	X	IB·NA	–	–	–	–
JIN	1	0	0	1	JUMP TO I BUS & LOAD CR2	1	X	IB·NA	–	IB	–	–
JPI	1	0	1	0	JUMP TO PRIMARY INST.	1	X	CR2·NA	–	–	–	–
JEP	1	1	1	0	JUMP TO EXTERNAL PORT	1	X	ØB·NA	–	–	–	–
JL2	0	0	0	1	JUMP & LOAD CR2	1	X	NA	–	IB	–	–
JLA	0	0	1	1	JUMP & LOAD ADDRESS	1	X	NA	CR0 plus C_{in}	–	–	–
JSR	0	0	0	0	JUMP TO SUBROUTINE	1	$\overline{RSQ}$+RIN·$\overline{XB}$=0	NA	–	–	"PUSH" CR0 TO STACK	–
						1	$\overline{RSQ}$+RIN·$\overline{XB}$=1	NA	–	–	"PUSH" CR0 plus C_{in}	–
RTN	1	1	1	1	RETURN FROM SUBROUTINE	1	$\overline{RSQ}$+RIN·$\overline{XB}$=0	CR4	CR1 plus C_{in}	–	"POP" STACK TO CR0	–
						1	$\overline{RSQ}$+RIN·$\overline{XB}$=1	CR4	–	–	"POP" STACK TO CR0	0
RSR	1	1	0	1	REPEAT SUBROUTINE	1	X	CR0 plus C_{in}	NA	–	–	1
RPI	1	0	1	1	REPEAT INSTRUCTION	1	$\overline{RSQ}$+RIN·$\overline{XB}$=0	–	CR1 plus C_{in}	–	–	–
						1	$\overline{RSQ}$+RIN·$\overline{XB}$=1	CR1·NA	–	–	–	0
BRC	0	1	0	1	BRANCH ON CONDITION	1	$\overline{XB}$·(CS4+$\overline{B}$)=0	NA	–	–	–	–
						1	$\overline{XB}$·(CS4+$\overline{B}$)=1	CR0 plus C_{in}	–	–	–	–
BSR	0	1	0	0	BRANCH TO SUBROUTINE	1	$\overline{XB}$·(CS4+$\overline{B}$)=0	NA	–	–	"PUSH" CR0 plus C_{in}	–
						1	$\overline{XB}$·(CS4+$\overline{B}$)=1	CR0 plus C_{in}	–	–	–	–
ROC	0	1	1	1	RETURN ON CONDITION	1	$\overline{XB}$·(CS4+$\overline{B}$)=0	CR4	–	–	"POP" STACK TO CR0	–
						1	$\overline{XB}$·(CS4+$\overline{B}$)=1	NA	–	–	–	–
BRM	0	1	1	0	BRANCH & MODIFY	1	CS4=1	NA	–	–	–	–
						1	CS4=0	CR00=NA0·B CR01=NA1·XB CR02=NA2 CR03=NA3	–	–	–	–

NOTES.
1. X = DON'T CARE STATE
   – = NO CHANGE
2. EQUATIONS APPLY AS SHOWN, WHERE:
   RIN = (CR13·CR12·CR11·CR10)
   $\overline{XB}$ = EXTERNAL EXTENDER BUS NODE (see Table 3)
   $\overline{B}$ = COMPLEMENT OF BRANCH INPUT
3. RSQ = OUTPUT OF RSR FLIP FLOP
4. ALL REGISTERS AND RSR FLIP FLOP CHANGE STATE ON V_{OL} TO V_{OH} (POSITIVE GOING) CLOCK TRANSITION
5. NEGATIVE LOGIC USED THROUGHOUT
6. TABLE 8 SHOWS LIFO STACK TRUTH TABLE
7. CR0 CHIP OUTPUTS ENABLED WHEN CS5=1

JIB – Jump to I Bus

The JIB instruction is a direct jump to address information on the I Bus port. The I Bus is normally an internal data bus in the processor and can be used to input the starting address of a microprogram instruction routine. The I Bus data is modified or "masked" with control memory feedback on the NA inputs. The next address is therefore determined by I Bus ANDed with NA inputs.

JIN – Jump to I Bus and Load CR2

The JIN command routes the I Bus ANDed with NA input to CR0 as does JIB. In addition, JIN loads unmodified I Bus data into register CR2 on the same clock edge. This information in CR2 can be used at a later point in microprogram for primary and secondary program flow modification.

JPI – Jump to Primary Instruction

The JPI command is a jump to the contents of CR2 ANDed with the NA inputs. Register CR2 is loaded with a previous JIN or JL2 instruction. The code stored in CR2 is used to start a new sequence of microinstructions or modify the present microinstruction sequence.

JEP – Jump to External Port

The JEP instruction is a direct jump to information on the Ø Bus port. The Ø Bus data is ANDed with the NA inputs (Ø Bus•NA) prior to entering register CR0. This instruction offers an additional port to enter a starting address or modify information to microprogram flow.

JL2 – Jump to NA Inputs and Load CR2

The JL2 command is a direct jump to the NA inputs and a parallel load of CR2 from the I Bus. This instruction allows CR2 to be loaded during the execution of another microinstruction. This is useful for storing an interrupt vector or a new operation address while finishing a previous microinstruction sequence.

JLA – Jump to NA Inputs and Load CR1

The JLA command is a direct jump to the NA inputs and a parallel load of CR1. CR1 is loaded with the incremented value of CR0 (CR0 plus C_{in}). The JLA instruction can be used to service an interrupt or as an additional form of subroutining.

JSR – Jump to Subroutine

The JSR instruction is an unconditional jump to subroutine. The jump address is provided by the NA inputs which are loaded into register CR0. At the same time, the present CR0 address is routed through the incrementer and "pushed" onto the LIFO stack to CR4.

The JSR command operates in two modes depending upon the status of the RSR flip flop (see Table 2).

1. Non-Repeat mode is used for normal subroutining. The RSR flip flop is clear (RSQ = 0) which causes the present CR0 address to be incremented and pushed onto the stack. That is, CR0 plus $C_{in} \rightarrow$ CR4 and the contents in registers CR4 through CR7 are "pushed down" one location. Upon a return from subroutine, the incremented address puts the control into the main program flow one location below the JSR address.

2. Repeat mode is used for multiple executions of a single subroutine. The RSR flip-flop has been previously set (RSQ = 1) by an RSR instruction.

   The incrementer is disabled and CR0 is loaded into CR4. The stack registers CR4–CR7 are pushed down as before. Upon a return from subroutine, the original JSR address is then returned to CR0 and the JSR is executed again. This repeat cycle will continue until $\overline{XB}$ signifies the final repeat count has been reached.

   For multiple MC10801 configurations, the $\overline{XB}$ line is a common connection between parallel circuits. The RSR flip-flop significes the repeat mode and $\overline{XB}$ combines with CR1 registers to determine the final repeat count. During a JSR instruction the incrementer is controlled by the following equation:

   $$\text{INTERNAL CARRY\_IN} = C_{in} \cdot (\overline{RSQ} + (CR13 \cdot CR12 \cdot CR11 \cdot CR10) \cdot \overline{XB})$$

Additional information on the $\overline{XB}$ line is found in the following Branch Control and Applications sections.

RTN – Return from Subroutine

The RTN is an unconditional return from subroutine in which the LIFO stack is "popped" and the contents of CR4 are transferred to CR0. Up to 4 levels of nesting are possible with the on-chip stack.

The RTN instruction is used with the JSR instruction for normal subroutining or multiple executions, again dependent on the RSR flip-flop (see Table 2).

1. If RSQ = 0, a normal return is executed. The stack is "popped" and the contents of CR4 are loaded into CR0.

2. If RSQ = 1, the stack is "popped" to CR0 and CR1 is incremented. The RTN will continue in the repeat mode until CR1 is filled with all ones. The RSR flip-flop is reset when all CR1 registers reach full count. As with the JSR command $\overline{XB}$ interconnects parallel MC10801's to determine full count.

RSR – Repeat Subroutine

The RSR command initializes the RSR flip-flop and CR1 for repeating microinstructions or subroutines. During the RSR, CR0 is incremented to the next address location (CR0 plus $C_{in} \rightarrow$ CR0), CR1 is loaded from the N.A. inputs, and the RSR flip-flop is set to a logic "1".

Register CR1 determines the number of times a microinstruction or subroutine will be repeated. Used as a cycle counter, CR1 is incremented until the register contains all ones (final count). For this reason, the repeat count originally loaded into CR1 must be the *2's complement* of the desired count number.

Setting the RSR flip-flop to a logic "1" causes JSR and RTN to repeat subroutines and RPI to repeat single microinstructions.

RPI — Repeat Instruction

The RPI command is used to repeat single microinstructions. In a repeat mode (RSR flip flop set to logic 1 by an RSR instruction), RPI holds the CR0 control memory address constant and increments the CR1 repeat counter. At the final repeat count, all "1"s in CR1, the RSR flip-flop is reset to logic "0" and RPI loads the contents of CR1 ANDed with the N.A. inputs into CR0.

The RPI therefore directly jumps to the new address on the N.A. inputs after the microinstruction repeat sequence is complete. (Note that CR1 remains at all "1"s after completing the repeat sequence.)

$\overline{XB}$ is common to all parallel MC10801s to insure CR1 is full on all circuits.

When not in a repeat mode (RSR flip-flop at logic "0"), the RPI instruction becomes a direct jump to register CR1. CR1 is ANDed with the N.A. inputs and loaded into CR0. In this mode RPI is used with JLA for a single level subroutine, where the return address is: (the starting address plus C_{in}) ANDed with N.A.

BRC — Branch on Condition

The BRC instruction is a conditional jump to the N.A. inputs. The branch decision is determined by the equation:

$$\overline{XB} \cdot (CS4 + \overline{B})$$

where $\overline{XB}$ is the external Extender Bus common to all parallel circuitry and B is the branch input to any MC10801. If the branch equation equals "0", BRC executes a direct jump to N.A. inputs. If the branch equation equals a logic "1", the present control memory address in CR0 is incremented (CR0 plus $C_{in} \rightarrow$ CR0) and the program goes to the next sequential location.

Normally the test bit is applied to an MC10801 branch, B, input. For multiple chip configurations, the $\overline{XB}$ line is connected common so all MC10801 respond to the same branch signal. Select line CS4 is an enable for the B input and selects which MC10801 B input is tested for the branch decision. A selected CR3 bit may also be used for branching as described in Table 4.

BSR — Branch to Subroutine

The BSR is a conditional jump to subroutine. The branch condition is determined by the $\overline{XB}$ line and the B input as with BRC. If $\overline{XB} \cdot (CS4 + \overline{B})$ = logic "0" the BSR jumps to subroutine. The subroutine destination on the N.A. inputs is loaded into CR0, and the present address in CR0 is incremented and pushed into the LIFO stack (CR0 plus $C_{in} \rightarrow$ CR4). If the branch equation equals logic "1", the present control memory address is incremented (CR0 plus $C_{in} \rightarrow$ CR0).

Unlike JSR, the BSR command is unaffected by the RSR flip flop status. Therefore, a BSR subroutine can be nested within a JSR/RTN repeat subroutine sequence without incrementing the CR1 cycle count register. A ROC is then used to return from the BSR jump.

ROC — Return on Condition

The ROC is a conditional return from subroutine. If the branch equation $\overline{XB} \cdot (CS4 + \overline{B}) = 0$, the return is executed by popping the LIFO stack and loading CR4 into CR0. If the equation equals a logic "1", the MC10801 performs a direct jump in the subroutine by loading the N.A. inputs into CR0. ROC operates independent of the RSR flip flop and can be used with BSR to nest subroutines within a repeat sequence.

BRM — Branch and Modify

The BRM instruction is a jump to the N.A. inputs with an address modification by the B and $\overline{XB}$ inputs. The following information is loaded into CR0 with CR03 being the most significant bit in the part.

CR03 = NA3
CR02 = NA2
CR01 = NA1•XB
CR00 = NA0•B

Note that $\overline{XB}$ is inverted as a modifier. This address modification allows multiway branching where the branches are sequential locations.

CS4 overrides the branch modifiers as shown in Table 2. When multiple MC10801s are operated in parallel, CS4 can be used to disable B and $\overline{XB}$ on all but the two least significant address bits.

REPEAT AND BRANCH CONTROL B, $\overline{XB}$, CS4

The Branch (B), Extender Bus ($\overline{XB}$) and Select line CS4 control certain MC10801 instructions to make repeat or conditional jump decisions.

Branch-B and Select line—CS4:

Branch operations BRC, BSR, and ROC use the B input as a source of decision information. Parallel MC10801 circuits determine the branch status from any B input enabled by select line CS4. The selected B input is routed to the $\overline{XB}$ line which is common to all MC10801s and allows parallel circuits to operate as a unit.

A branch decision depends on the following equation: $\overline{XB} \cdot (CS4 + \overline{B})$. Select line CS4 enables the B input when held at a negative logic "0" (MECL V_{OH}). Branch then occurs if B = logic "1", and the $\overline{XB}$ line extends this branch condition to all parallel circuits. $\overline{XB}$ is a complemented signal to operate properly when wired

together using the emitter dot (negative logic AND function).

The BRM instruction is a special type of branch where the B and $\overline{XB}$ lines determine register CR0 bits as follows:

CR03 = NA3
CR02 = NA2
CR01 = NA1•XB
CR00 = NA0•B

Select line CS4 overrides this use of the branch inputs. The above CR0 inputs are maintained with CS4 = logic "0" and the 4 NA inputs are routed directly to CR0 when CS4 = logic "1". This feature is used with parallel MC10801 circuits to perform a 4-way branch with the two least significant address bits. CS4 disables branch on the more significant circuits. If two MC10801s are used with CS4 = "0" on both chips, 8 way branching is possible with the next microprogram address being NA7 NA6 NA5•$\overline{XB}$ NA4•B2 NA3 NA2 NA1•$\overline{XB}$ NA0•B1 where B1 is the branch input on the lower order chip and B2 is the branch input on the upper order chip.

Repeat operations JSR, RTN, and RPI respond to $\overline{XB}$, but not to B. The functional equation for a repeat decision is $\overline{RSQ}$ + RIN•$\overline{XB}$. Repeat operation is discussed in the preceding MC10801 instruction descriptions and the following applications section.

Extender Bus – $\overline{XB}$:

The $\overline{XB}$ line operates in several modes and can be driven from various parts of the MC10801 or from external circuitry.

The $\overline{XB}$ line is controlled by the B input to insure branch coupling between parallel circuits as described above. Status register CR3 bits can be multiplexed onto $\overline{XB}$ with select lines CS0 through CS3. To make branch decisions, the selected CR3 bit goes to all parallel MC10801s on the $\overline{XB}$ interconnection. Select lines CS0 through CS3 operate independently of the selected MC10801 IC0-IC3 control instruction and must be programmed for the branch.

Repeat register CR1 and the RSR flip-flop control $\overline{XB}$ during a JSR, RTN, or RPI instruction. If RSQ = logic "1" (the MC10801 in a repeat mode) and CR1 signifies a repeat count, $\overline{XB}$ is forced to a logic "0". $\overline{XB}$ going to all parallel MC10801 circuits, couples the cycle count information in CR1 to control the repeat sequence. During a repeat sequence CR3 status bits should be disabled from $\overline{XB}$ to avoid overriding the CR1 cycle count. In a nonrepeat mode, RSQ = logic "0", the $\overline{XB}$ line has no affect on JSR, RTN or RPI instructions.

It is possible to control or modify the $\overline{XB}$ line from an external signal. The $\overline{XB}$ pins of parallel MC10801s are emitter dotted and an external signal can be tied into this connection. The external signal would override internal MC10801 control by forcing a negative logic "0" (MECL V_{OH}) on the $\overline{XB}$ line. This feature is not required for normal MC10801 operation and would be used to produce special branch functions.

Table 3 is a listing of the $\overline{XB}$ status as controlled by the various MC10801 control sequence instructions and select lines CS0, CS1, CS3 and CS4.

TABLE 3

TRUTH TABLE FOR THE $\overline{XB}$ (EXTENDER BUS) LINE

COMMENTS	1 REPEAT FUNCTION	BRANCH DISABLE CS4	INSTRUCTION CONTROL IC3-IC0 MNEMONIC CODE	2 CS3	CS1	CS0	3 $\overline{XB}$
Branch input or repeat function can not affect the $\overline{XB}$ line on these instructions.	X	X	$\overline{JSR+RPI+RTN+\ldots}$ $\overline{BRC+BSR+ROC}$	1	X	X	1
				0	0	0	$\overline{CR30}$
				0	0	1	$\overline{CR31}$
				0	1	0	$\overline{CR32}$
				0	1	1	$\overline{CR33}$
Branch input can not affect the $\overline{XB}$ line when CS4 = 1.	X	1	BRC+BSR+ROC	1	X	X	1
				0	0	0	$\overline{CR30}$
				0	0	1	$\overline{CR31}$
				0	1	0	$\overline{CR32}$
				0	1	1	$\overline{CR33}$
The Branch input is selected onto the $\overline{XB}$ line when CS4 = 0 and the instruction is a BRC, BSR or ROC	X	0	BRC+BSR+ROC	1	X	X	$\overline{B}$
				0	0	0	$\overline{B \cdot CR30}$
				0	0	1	$\overline{B \cdot CR31}$
				0	1	0	$\overline{B \cdot CR32}$
				0	1	1	$\overline{B \cdot CR33}$
If the repeat function = 0, the $\overline{XB}$ line is unaffected by JSR, RPI, or RTN	0	X	JSR+RPI+RTN	1	X	X	1
				0	0	0	$\overline{CR30}$
				0	0	1	$\overline{CR31}$
				0	1	0	$\overline{CR32}$
				0	1	1	$\overline{CR33}$
If the repeat function = 1, $\overline{XB}$ is forced to 0 on a JSR, RPI or RTN	1	X	JSR+RPI+RTN	X	X	X	0

"X" represents a Don't Care Condition

NOTES 1. (RSQ)•($\overline{CR13 \cdot CR12 \cdot CR11 \cdot CR10}$) Repeat Function
2. CS3 enables a bit from CR3 to be placed on $\overline{XB}$; CS0 and CS1 select the bit from CR3.
3. The $\overline{XB}$ line can be forced to a "0" from an external chip using the negative logic "AND"

STATUS REGISTER CR3 CONTROL
CS0, CS1, CS2, CS3

Register CR3 is primarily used as a storage area for microprogram status information. The contents of this register are continuously available on MC10801 package pins CR30 through CR33. Information can be loaded from the I Bus port, NA inputs, or from the single line input, D_{in}. Select lines CS0 through CS3 and the reset, $\overline{RST}$, input control all CR3 load operations. In addition, CS0, CS1, and CS3 enable CR3 bits onto the $\overline{XB}$ line as described in the preceeding section and Table 3.

CS0 and CS1 select one of the four CR3 bits to be loaded from information on the D_{in} input. This occurs with CS2 = logic "0". CS0 and CS1 also select the I Bus or NA inputs for parallel loading CR3. Table 4 shows the truth table for entering information into CR3. As with all MC10801 registers, CR3 is a master-slave design which loads information on a positive going (V_{OL} to V_{OH}) clock edge.

TABLE 4

TRUTH TABLE FOR
STATUS REGISTER CR3 AND $\overline{XB}$ AS A FUNCTION OF CS0-CS3

	SELECT LINE INPUTS				REGISTER CR3 OUTPUTS				
$\overline{RST}$	CS3	CS2	CS1	CS0	CR33	CR32	CR31	CR30	$\overline{XB}$
0	X	X	X	X	0	0	0	0	
1	0	0	0	0	-	-	-	DIN	$\overline{CR30}$
1	0	0	0	1			DIN		$\overline{CR31}$
1	0	0	1	0		DIN			$\overline{CR32}$
1	0	0	1	1	DIN	-	-		$\overline{CR33}$
1	0	1	0	0					$\overline{CR30}$
1	0	1	0	1					$\overline{CR31}$
1	0	1	1	0					$\overline{CR32}$
1	0	1	1	1					$\overline{CR33}$
1	1	0	0	0				DIN	1
1	1	0	0	1			DIN		1
1	1	0	1	0		DIN			1
1	1	0	1	1	DIN				1
1	1	1	0	0	0	0	0	0	1
1	1	1	0	1	IB3	IB2	IB1	IB0	1
1	1	1	1	0	NA3	NA2	NA1	NA0	1
1	1	1	1	1					1

"X" represents a Don't Care Condition; " " represents a NO CHANGE Condition

NOTES: 1. Register CR3 changes state on a V_{OL} to V_{OH} transition at the clock input.
2. The $\overline{XB}$ line can be forced to a "0" due to a branch or repeat condition. Table 3 fully describes $\overline{XB}$.

CR0 OUTPUT BUFFER ENABLE CS5

Select line CS5 provides a gating function on the CR0 control memory address outputs. A logic "1" on CS5 enables CR0 to package pins CR00 through CR03. A logic "0" on CS5 forces the buffer outputs to a logic "1" state. This negative logic 1 (MECL V_{OL}) frees the CR0 output pins and allows for an external source of control memory address information. Note that when the CR0 buffers are disabled, the CR0 information is still available for internal operation. This alternate addressing feature can be used to load writable control storage on power up or for forcing interrupt vectors and overriding normal MC10801 operation. Table 5 shows the truth table for the CS5 input.

TABLE 5

TRUTH TABLE FOR CR0 OUTPUT BUFFER

CS5	OUTPUTS CR00 – CR03
1	ENABLED
0	DISABLED

BUS CONTROL CS6, CS7, CS8

The I Bus and Ø Bus function as I/0 ports for information stored within the MC10801 internal registers. For data output, CS6, CS7, and CS8 select the proper register and enable the bus output drivers. When not used to output data the MC10801 internal bus drivers are forced to a negative logic 1 (MECL V_{OL}) to provide for I Bus and Ø Bus data input operations.

Lines CS6, CS7, and CS8 select data from registers CR1, CR2, or either end of the LIFO stack CR4 and CR7. CS6 selects either the I Bus or the Ø Bus while CS7 and CS8 control the source of output data. Registers CR1 and CR2 are directly selected. However, CR4 and CR7 selection is dependent upon IC0-IC3 control instructions involving the LIFO. CR7 can be read only during a JSR or BSR with branch LIFO push operation. Reset, $\overline{RST}$, results in a LIFO push and also enables CR7 as an output.

LIFO pop operations, as caused by a RTN or ROC with branch, forces a logic 1 state on the I Bus and Ø Bus drivers. Either port can then input information to CR7 as required to extend the stack depth with external circuits. All MC10801 control instructions not involving the LIFO enable CR4 as a possible I Bus or Ø Bus data source. Table 6 shows registers available to the I Bus and Ø Bus as output ports.

TABLE 6

SELECTING THE I BUS AND Ø BUS AS DATA OUTPUTS

INSTRUCTION CONTROL IC0 – IC3 MNEMONIC CODE	RST	CS7	CS8	CS6 0 ØB	CS6 0 IB	CS6 1 ØB	CS6 1 IB
X	X	0	0	1	CR1	CR1	1
JSR•BSR•$\overline{XB}$	X	0	1	1	CR7	CR7	1
X	0	0	1	1	CR7	CR7	1
RTN•ROC•$\overline{XB}$	1	0	1	1	1	1	1
$\overline{JSR•RTN•(BSR•ROC)•XB}$	1	0	1	1	CR4	CR4	1
X	X	1	0	1	CR2	CR2	1
X	X	1	1	1	1	1	1

X = Don't care

The bus control inputs also select either the I Bus or Ø Bus as input ports to load information into the bottom of the LIFO (CR7). Select line CS6 selects either the I Bus or Ø Bus while CS7 and CS8 in conjunction with a LIFO pop function, RTN or ROC with branch, enables these ports as inputs to CR7. Table 7 shows complete LIFO operation and selection of I Bus and Ø Bus as controlled by the IC0-IC3 control instructions and the CS6-CS8 bus control inputs.

The I Bus automatically becomes an input port to CR0 or CR2 during a JIB, JIN, or JL2 instruction. When using these instructions a logic "1" is normally selected on the I Bus drivers, see Table 6, to avoid a conflict between internal register data and the incoming I Bus information.

CARRY OUT C_{OUT}

The C_{out} line is a direct function of the C_{in} input and the CR1 or CR0 registers as shown in Table 8. Note that when RSQ = 0, C_{out} always monitors the CR0 register independent of the IC0--IC3 instruction inputs.

TABLE 7

TRUTH TABLE FOR THE 4 X 4 LIFO STACK (REGISTERS CR4-CR7)

INSTRUCTION CONTROL IC0 – IC3 MNENONIC CODE	RST	$\overline{XB}$	RSQ	CS6	CS7	CS8	NEXT STATE CR4	CR5	CR6	CR7
RTN + RPI	0	X	1	X	X	X	CR1	CR4	CR5	CR6
RTN + $\overline{RPI}$	0	X	0	X	X	X	CR0	CR4	CR5	CR6
$\overline{RTN}$ + $\overline{RPI}$	0	X	X	X	X	X	CR0	CR4	CR5	CR6
JSR	1	X	0	X	X	X	CR0 Plus C_{IN}	CR4	CR5	CR6
JSR	1	1	1	X	X	X	CR0 Plus C_{IN}	CR4	CR5	CR6
JSR	1	0	1	X	X	X	CR0	CR4	CR5	CR6
BSR	1	1	X	X	X	X	-	-	-	-
BSR	1	0	X	X	X	X	CR0 Plus C_{IN}	CR4	CR5	CR6
RTN	1	X	X	X	0	0	CR5	CR6	CR7	0
RTN	1	X	X	X	1	X	CR5	CR6	CR7	0
RTN	1	X	X	0	0	1	CR5	CR6	CR7	IB
RTN	1	X	X	1	0	1	CR5	CR6	CR7	OB
ROC	1	1	X	X	X	X	-	-	-	-
ROC	1	0	X	X	0	0	CR5	CR6	CR7	0
ROC	1	0	X	X	1	X	CR5	CR6	CR7	0
ROC	1	0	X	0	0	1	CR5	CR6	CR7	IB
ROC	1	0	X	1	0	1	CR5	CR6	CR7	OB
$\overline{JSR}$ + $\overline{BSR}$ + $\overline{RTN}$ + $\overline{ROC}$	1	X	X	X	X	X	-	-	-	-

"X" represents a Don't Care Condition, "-" represents a NO CHANGE Condition

TABLE 8

TRUTH TABLE FOR C_{out}

INSTRUCTION CONTROL IC0 – IC3	RSQ	C_{out}
RPI + RTN	0	C_{in}·CR03·CR02·CR01·CR00
RPI + RTN	1	C_{in}·CR13·CR12·CR11·CR10
$\overline{RPI}$ + $\overline{RTN}$	X	C_{in}·CR03·CR02·CR01·CR00

APPLICATIONS INFORMATION

The MC10801 fits a wide range of system sizes and applications, and therefore, has no fixed interconnection configuration. The specific system design goals will determine the control memory size, the number of MC10801s, and the interconnection pattern. A typical small processor control section can, however, illustrate use of the MC10801. Figure 3 shows two MC10801s plus microprogram control storage for the processor. Various features are described below:

MEMORY ADDRESSING

Two MC10801s provide increment, direct jump, branch, and subroutine capability for up to 256 words of control memory. Three devices can extend this to 4K words. Control register CR0 outputs are the control memory address.

A second technique to extend memory addressing beyond 256 words is two MC10801s and word-page memory mapping. Status Register CR3 of device B extends the memory size to 16 pages of 256 words each. Increment, direct jump, branch, and subrouting are restricted to within a given page, however, the third MC10801 and Next Address feedback bits from control storage are eliminated. The page address is loaded from the I Bus or NA inputs and controlled via the Status Field.

CONTROL STORAGE

Control storage can be as large as 4K words (16 pages x 256 words) for the example shown. If writable control storage is desired, MECL RAM's (MCM 10144 or MCM 10146) are used. For PROM the MCM 10149 is used.

The word length is the sum of the various control fields existing in the control storage. The Instruction Field equals 4 bits, the Next Address Field equals 8 bits, the Status Field is up to 10 bits, etc. It is not unusual for the word size to be 40 to 80 bits or more including the RF, ALU condition code, and other processor fields.

If system cycle times permit, the word size can be decreased by control field decoding. Small PROMs such as the MCM10139 or discrete logic are used to decode the select line signals. The number of microprogram bits can be reduced, but additional delay in the feedback path is introduced.

MICROPROCESSOR SEQUENCE CONTROL

The control fields feedback from storage to the MC10801s determine the microprogram sequence. The 4-bit Instruction Field selects one of 16 control instructions to generate the next microprogram address. Instruction lines IC0 through IC3 are respectively tied in parallel so that devices A and B perform the same instruction.

The Next Address Field is 8 bits wide – four bits to the most significant device B and the other four bits to device A. The NA inputs are the source of constants, starting addresses, jump and branch vectors, subroutine vectors, and masking information. The data at the NA inputs is used by the MC 10801 and controlled by the Instruction Field and/or the Status Field.

The Status Field can be up to 10 bits wide. The number of bits can be decreased with decoding or with selective functions used in the MC10801.

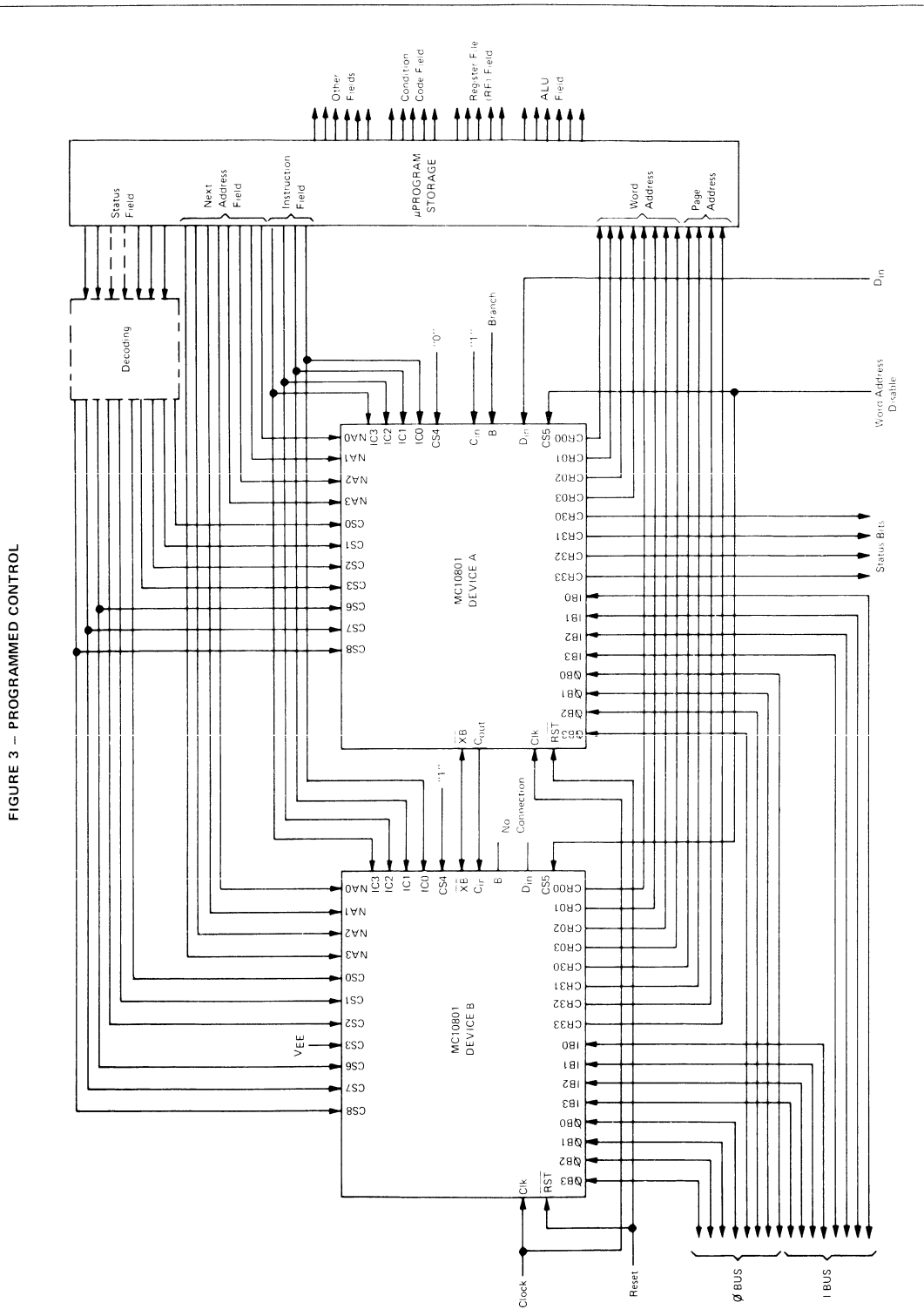


FIGURE 3 — PROGRAMMED CONTROL

Control lines CS0 through CS3 are driven independently because they manipulate register CR3 on each MC10801. Register CR3 is the Page Address register on device B, and is a status bit register on device A. Each CR3 register on the two MC10801's must be controlled independently.

Other connections to the MC10801s include:

1. C_{in} of the least significant device A is a logic "1" for increment functions. C_{out} of device A ripples to C_{in} of device B.

2. The $\overline{XB}$ lines are tied common for parallel branch functions.

3. Branch information is tested on the B input of device A. As a result, CS4 = 1 for device B to disable its branch input because the input is not used.

4. Clock and reset are tied in parallel on both devices.

5. CS5 is the CR0 output disable or the Word Address Disable. This line can be used for writable control storage functions or for interrupt functions.

6. Data can be entered into the CR3 register on a single bit basis using the D_{in} input.

I BUS AND Ø BUS

The data buses are tied to other ports of the processor. Starting addresses, interrupt vectors, and extension of the internal LIFO stack are common uses of these buses. Both the I Bus and Ø Bus are bidirectional, and are controlled by the Status Field and the Instruction Field.

SUBROUTINE & REPEAT FUNCTIONS

Subroutine and repeat operations are important functions of the MC 10801. These can each be illustrated simply.

1. Non-repeat subroutine – an example is illustrated in Figure 4. The address is limited to the word address and is listed in hexadecimal. At address 06, a JSR is executed in which address 17 → CR0, the present address plus 1 → CR4, and the stack is pushed. The subroutine begins at address 17 and ends at address 19 with an RTN. When the RTN is executed, (CR4) → CR0, the stack is popped, and the program jumps to location 07 to continue the program.

FIGURE 4 – NON-REPEAT SUBROUTINE LISTING

ADDRESS	I FIELD	NA FIELD	DESCRIPTION
06	JSR	17	06 + 1 → CR4, Push Stack, 17 → CR0
07	INC	X	Continue Program
17	INC	X	Beginning of Subroutine
18	INC	X	
19	RTN	X	(CR4) → CR0, Pop Stack

2. Repeat subroutine – Figure 5 shows this example. The instruction flow is similar to the above example except that an RSR must be executed. During the RSR, CR1 is loaded with the 2's complement of 4 which is the number of times the subroutine is to be repeated. In hexadecimal notation, this is FC for 4 cycles. Also RSQ is set to 1 for repeat (in the non-repeat mode RSQ = 0).

The JSR is executed to begin the subroutine operation. During the JSR, the subroutine address 17 → CR0, the present address 06 plus C_{in} internal → CR4 and the stack is pushed. If RSQ = 0 or CR1 = FF, C_{in} internal = 1. Thus for the first 3 cycles when the JSR is executed, the present address 06 is loaded into CR4.

At the end of each subroutine cycle, an RTN is executed or (CR4) → CR0; the stack is pushed; and if RSQ = 1 and CR1 ≠ FF, then CR1 is incremented and if CR1 = FF, 0 → RSQ. In this example for the first 3 cycles, the RTN jumps to 06 (the JSR) and CR1 is incremented finally to FF.

On the final cycle, the JSR is executed with CR1 = FF and address 07 is loaded into CR4. Then, the RTN resets RSQ and jumps to location 07 to end the operation.

For this example with an 8-bit word address, the maximum number of subroutine cycles is 256.

FIGURE 5 – REPEAT SUBROUTINE LISTING

ADDRESS	I FIELD	NA FIELD	DESCRIPTION
05	RSR	FC	1111 1100 → CR1; 1 → RSQ
06	JSR	17	06 + C_{IN} Internal → CR4, Push Stack; 17 → CR0. If RSQ = 0 or CR1 = FF, then C_{IN} Internal = 1.
07	INC	X	Continue Program
17	INC	X	Beginning of Subroutine
18	INC	X	
19	RTN	X	(CR4) → CR0, Pop Stack. If RSQ = 1 and CR1 ≠ FF, then (CR1) +1 → CR1, if CR1 = FF, then 0 → RSQ

3. Repeat Instruction is shown in Figure 6. As in the repeat subroutine, an RSR is executed loading CR1 with = FC and RSQ is set. This sets the number of instruction cycles at 4.

   An RPI then is executed. If RSQ = 1 and CR1 ≠ FF, then (CR1) plus 1 → CR1 and CR0 → CR0. If CR1 = FF, RSQ is reset and (11)·(FF) → CR0.

   Thus for the first 3 cycles, CR1 is incremented and CR0 stays at the present address.

   During the fourth and final cycle (CR1 = FF from the third cycle) RSQ is reset and CR0 jumps to the Next Address value (11) AND'ed with the value of CR1 (FF) which is all logic 1s. The location 11 now continues the program.

   The maximum repeat cycle is again 256.

FIGURE 6 – REPEAT INSTRUCTION LISTING

ADDRESS	I FIELD	NA FIELD	DESCRIPTION
09	RSR	FC	1111 1100 → CR1; 1 → RSQ
0A	RPI	11	If RSQ = 1 and CR1 ≠ FF, then (CR1) + 1 → CR1, (CR0) → CR0. If CR1 = FF, then 0 → RSQ (11·FF) → CR0
11	INC		Continue Program

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage (V_{CC} = 0 Volts)	V_{TT} V_{EE}	−1.9 to −2.2 −4.68 to −5.72	Vdc Vdc
Operating Temp. (Functional)	T_A	−30 to +85	°C
Output Drive	—	50Ω to −2.0 Vdc	—
Maximum Clock Input Rise and Fall Time (20% to 80%)	t_r, t_f	10	ns
Minimum Clock Pulse Width	PW	5	ns

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@Test Temperature	TEST VOLTAGE VALUES (Volts)					
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{TT}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2	−2.0
+25°C	−0.810	1.85	1.105	−1.475	5.2	−2.0
+85°C	0.700	−1.825	1.035	−1.440	−5.2	−2.0

Characteristic	Symbol	Pin Under Test	TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{TT}	(V_{CC}) Gnd
Power Supply Drain Current	I_{EE}	1, 24				200				mAdc					1, 24	25, 48	7,12,17,36
	I_{TT}	25, 48				270									1, 24	25, 48	7,12,17,36
Input Current	I_{inH}	23					45			μAdc	23				1, 24	25, 48	7,12,17,36
		42					370				42						
		40					470				40						
	I_{inL}	18			0.5							18					
Logic "0" Output Voltage	V_{OH}	16	−1.060	−0.890	−0.960		−0.810	−0.890	−0.700	Vdc	*18,26,27,45				1, 24	25, 48	7,12,17,36
		2	−1.060	−0.890	−0.960		−0.810	−0.890	−0.700	Vdc	41,44,46	40,42,43			1, 24	25, 48	7,12,17,36
Logic "1"† Output Voltage	V_{OL}	16	−1.940	−1.675	−1.900		−1.650	−1.875	−1.615	Vdc	45	26,27,40			1, 24	25, 48	7,12,17,36
		2	−1.890	−1.675	−1.850		−1.650	−1.825	−1.615	Vdc	**42,43,45	40,41,44,46,47			1, 24	25, 48	7,12,17,36
Logic "0" Threshold Voltage	V_{OHA}	2	−1.080		−0.980			−0.910		Vdc	**42,43,45	40,41,44,47	46		1, 24	25, 48	7,12,17,36
Logic "1" Threshold Voltage	V_{OLA}	2		−1.655			−1.630		−1.595	Vdc	**42,43,45	40,41,44,47		46	1, 24	25, 48	7,12,17,36

†The bi-directional outputs are specified at −1.90 volts for V_{OL} min.

Preset Conditions

*PS1 Apply V_{IH} at 37, 43; V_{IL} at 40, 41, 42, 44; then clock once (⊓⊔).

**PS2 Apply V_{IH} at 41, 42, 43, 44; V_{IL} at 33, 34, 35, 37, 40, 47; then clock once (⊓⊔).

SETUP AND HOLD TIMES
(NANOSECONDS AT 25°C)

Input	Setup Min	Hold Min
IC0–IC2 (1)	27	–2.0
IC0–IC3 (2, 3)	44	–8.0
NA0–NA3	28	+2.0
I Bus, Ø Bus	25	+1.0
CS0–CS3	35	–2.0
CS4 (4)	23	–2.0
B (4)	21	–1.0
C_{in}	15	+2.0
D_{in}	20	+2.0
$\overline{RST}$	20	+5.0
$\overline{XB}$	28	–4.0
$\overline{XB}$ (4)	20	–2.0

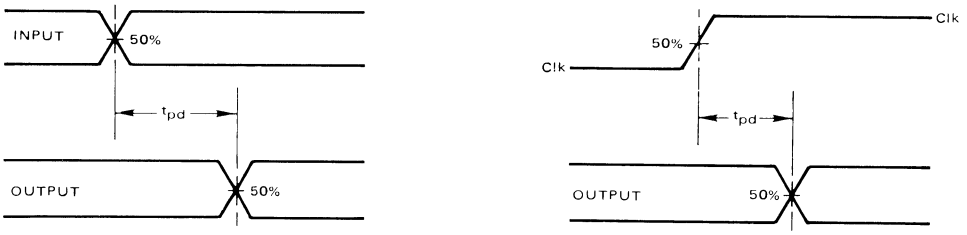
NOTES: (1) All instructions except 2 and 3 below.
(2) BSR, BRC, BRM, or ROC instruction when B · $\overline{CS4}$ = 1.
(3) BSR, BRC, BRM, ROC, JSR, RPI, or RTN instruction when RSQ = 1.
(4) BRM instruction only.

PROPAGATION DELAY TIMES (NANOSECONDS)

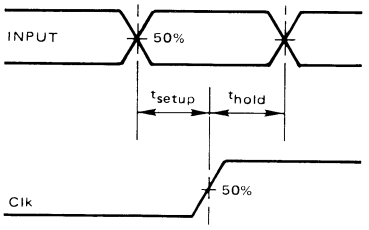
Input	Output	–30°C Typ	–30°C Max	+25°C Typ	+25°C Max	+85°C Typ	+85°C Max
Clock	CR0, CR3	11.1	16.0	11.2	16.0	12.0	17.0
Clock	IB, ØB	16.3	30.0	16.8	30.0	21.2	32.0
Clock	$\overline{XB}$	15.7	20.0	16.1	21.0	18.2	23.0
Clock	C_{out}	13.5	22.0	14.6	23.0	16.3	24.0
C_{in}	C_{out}	3.10	9.00	2.80	7.00	3.40	8.00
IC0–IC3	$\overline{ØB}$	22.7	32.0	23.4	33.0	28.9	38.0
IC0–IC3	$\overline{XB}$	14.9	20.0	15.9	21.0	19.1	24.0
IC0–IC3	C_{out}	17.4	26.0	17.4	26.0	20.9	27.0
CS7, CS8	IB, ØB	14.8	22.0	16.0	24.0	17.6	26.0
CS0–CS4, B	$\overline{XB}$	11.8	17.0	12.4	18.0	15.3	20.0
CS6	IB, ØB	7.00	11.0	6.80	11.0	7.70	12.0
CS5	CR0	5.20	10.0	5.30	10.0	6.10	11.0
$\overline{XB}$	IB, ØB	21.3	29.0	22.2	31.0	24.6	36.0
$\overline{RST}$	IB, ØB	18.8	26.0	19.6	28.0	22.9	31.0
TR, TF	All	6.00	11.0	6.50	11.0	8.30	12.0

SWITCHING WAVEFORMS

PROPAGATION DELAYS



SETUP AND HOLD



TEST PROCEDURE:

a) Establish setup time with long t_{hold}.

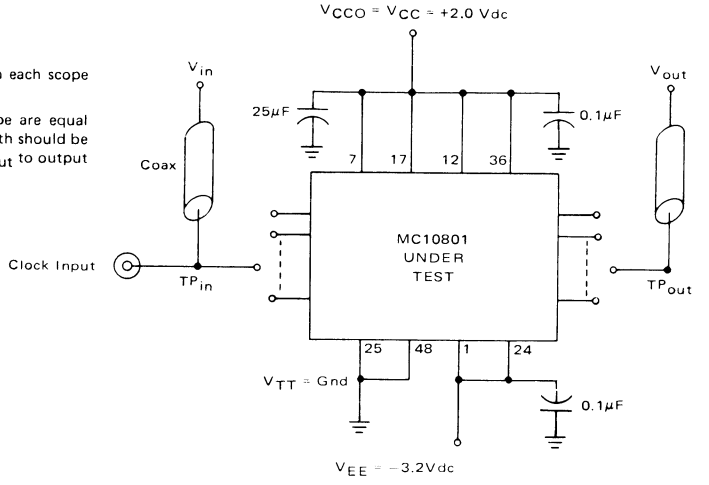
b) Keeping the leading edge of the input constant (t_{setup}) vary the trailing edge of the input to determine t_{hold}.

NOTE: t_{setup} and t_{hold} as defined are positive. Internal delays in the data path may result in a shift of the data waveform to the left, with respect to the clock, resulting in negative hold times.

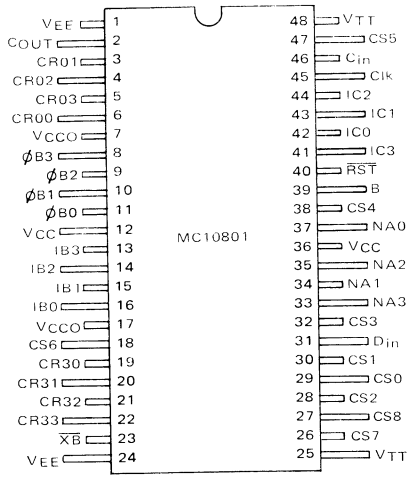
SWITCHING TIME TEST CIRCUIT

50 ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin.



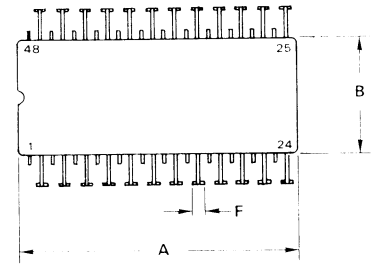
PIN ASSIGNMENT

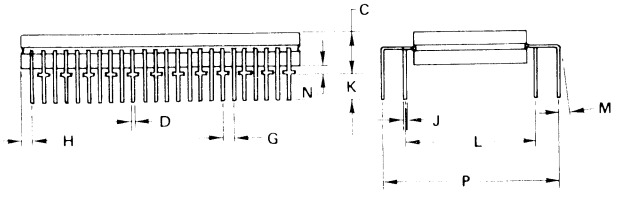


THERMAL CHARACTERISTICS
(TYPICAL)
@ 500 Linear Ft. Air Flow

$\theta_{JA} = 26.5^{o}$ C/W
$\theta_{JC} = 7^{o}$ C/W

PACKAGE DIMENSIONS





DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.57	5.59	0.180	0.220
D	0.38	0.53	0.015	0.021
F	1.14	1.40	0.045	0.055
G	1.27 BSC		0.050 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.54	3.30	0.100	0.130
L	15.24 BSC		0.600 BSC	
M	–	7^{o}	–	7^{o}
N	0.51	1.52	0.020	0.060
P	20.32 BSC		0.800 BSC	

Case 725-01

A socket for the QUIL package is available from ELECTRONIC MOLDING CORPORATION. (Part number 7178-295-5)

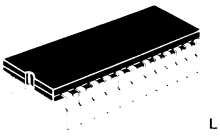
QUIL is a trademark of Motorola Inc.

MOTOROLA Semiconductors

MC10802

Advance Information

MECL – LSI
TIMING
FUNCTION



L SUFFIX
CERAMIC PACKAGE
CASE 623

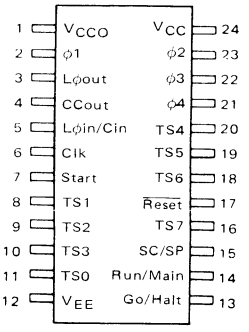
INTRODUCTION

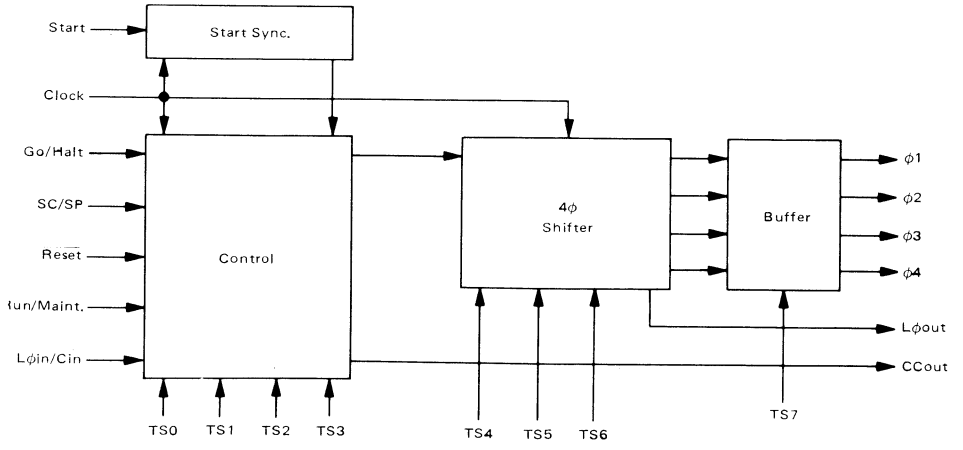
The MC10802 Timing Function is an LSI building block for digital processor systems. This circuit contains the logic and control lines to generate system clock phases and provides for start, stop, and diagnostic operations. Each part is four bits wide and can be connected in series for greater than four phase clock systems.

The Timing Function as shown in the block diagram below is composed of a four phase shifter circuit with buffered outputs. Fifteen input lines combine with Control and Start Sync logic to control all operations within the part.

FEATURES

- Programmable Number of Phases
- Selectable Double-Width Phases Duration
- Start Signal Synchronizer
- Single Cycle Stepping
- Single Phase Stepping
- Asychronous Master Reset
- Cascadable
- Fully Compatible with the MECL 10,000 Family





ADI-507

FUNCTIONAL DESCRIPTION

The MC10802 is a clock phase generator operating from a single clock source. The number of clock phases (up to four), phase duration, and operation modes are all programmable. Additionally, multiple devices can be cascaded for more than four clock phases. The following description details device operation.

CLOCK PHASE OUTPUTS

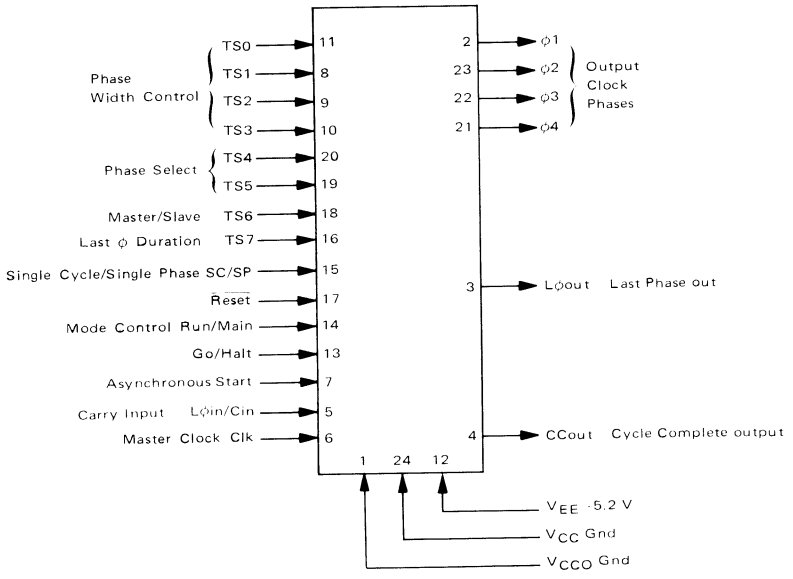
Up to four clock phases are available per circuit. The phase number is programmed by select lines TS4 and TS5 (Table 1). Clock phase outputs **are normally high** (V_{OH}) **and go low while active** (See Figures 5 and 6). The end of each phase is a low to high transition as required to clock MECL master-slave storage devices.

TABLE 1 – PHASE SELECTION

TS4	TS5	Phase Number
H	H	One Phase
L	H	Two Phases
H	L	Three Phases
L	L	Four Phases

The "One Phase" selection is used only with cascaded circuits, for example, five phases with two parts or nine phases with three parts. If used with a single circuit, the MC10802 stops with $\phi 1$ held at a low logic level (V_{OL}). A single phase clock is generated by programming the circuit to two phases, giving the desired clock and its complement on the $\phi 1$ and $\phi 2$ outputs.

INPUT/OUTPUT DIAGRAM-MC10802



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating		Symbol	Value	Unit
Supply Voltage (V_{CC} = 0)		V_{EE}	-8 to 0	Vdc
Input Voltage (V_{CC} = 0)		V_{in}	0 to V_{EE}	Vdc
Output Source Current	Cont	I_o	< 50	mAdc
	Surge	I_o	<100	mAdc
Storage Temp.		$T_{stg.}$	-55 to +150	°C
Junction Temp.		T_j	165	°C

NOTE: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Phase select lines TS4 and TS5 are fixed programmed for most systems; however, the number of selected phases can be dynamically changed if desired. The programming change of TS4 and TS5 must occur on or before the last phase of the smallest of the two selected numbers; that is, changing $\phi_n \rightarrow \phi_n + x$ or $\phi_n + x \rightarrow \phi_n$ must be done during or before ϕ_n and meet circuit setup and hold times. For example, changing from a four phase selection to a two phase selection must occur on or before $\phi 2$.

PULSE WIDTH DURATION

Each clock phase is normally one master clock period in duration. However, any or all selected phases can be extended to double duration. Select lines TS0 through TS3 independently control phase duration of the corresponding output (Table 2).

Similar to phase number selection, phase duration can be dynamically programmed. The associated select line must be stable for the positive going master clock edge that triggers the desired phase. Figure 1 shows an example of stretching $\phi 2$ with associated signals.

OPERATIONAL CONTROL

Control line inputs determine the MC10802 operating mode. System start, stop, and diagnostics can all be controlled via these MC10802 inputs as shown in Table 3.

1. $\overline{\text{RESET}}$ – is an asynchronous input overriding other control inputs. $\overline{\text{Reset}}$ drives all phase outputs to a high logic state. It also resets the circuit so $\phi 1$ will be the first phase after the circuit is initialized. $\overline{\text{Reset}}$ is active with a high logic level on the input. **$\overline{\text{Reset}}$ must be supplied on power up.**

TABLE 2 - PHASE DURATION

Select Line		Phase	Duration
TS0	H	1	Single
	L	1	Double
TS1	H	2	Single
	L	2	Double
TS2	H	3	Single
	L	3	Double
TS3	H	4	Single
	L	4	Double

2. MAINTENANCE MODE – is selected with the R/M input in the high logic state. The maintenance mode has four operating patterns as controlled by the G/H and SC/SP inputs (see Table 3). Each maintenance mode operation is initialized by a low, V_L, to high V_H, transition on the START input. This requirement for a start signal is normally used for diagnostic purposes or "front panel" interface. A special synchronizer circuit internal to the MC10802 allows the start signal to be asynchronous to the master clock.

   a. STOP AT END OF CYCLE – is a continuous cycle operation controlled by G/H=L and SC/SP=L. Initialized by a start signal, the MC10802 continues cycling until halted with the G/H input.

FIGURE 1 – STRETCHING PHASE TWO WITH ASSOCIATED SIGNALS

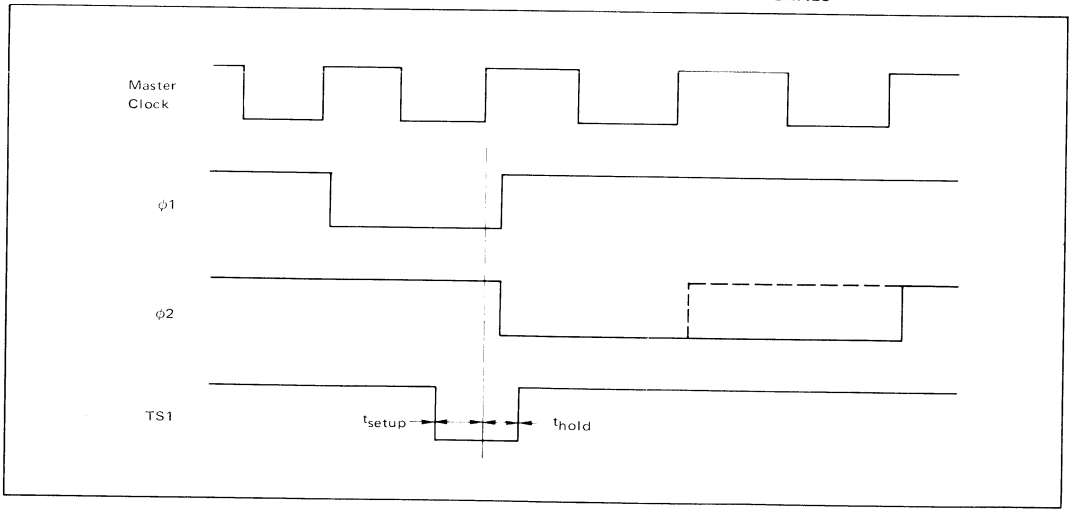


TABLE 3 – OPERATIONAL CONTROL

$\overline{\text{Reset}}$	R/M	G/H	SC/SP	Mode	Operation		Source
H	X	X	X	Reset	X		X
L	H	H	H	Maintenance	Halt	Single Phase	Start ⌐
		H	L			Single Cycle	Start ⌐
		L	H		Go	Stop on Phase	Initiate-Start ⌐ End-G/H ⌐
		L	L			Stop at End of Cycle	Initiate-Start ⌐ End-G/H ⌐
L	L	H	H	Run	Halt	Single Phase	Start ⌐
		H	L			Single Cycle	Start ⌐
		L	H		Go	Stop on Phase	Initiate-G/H ⌐ End-G/H ⌐
		L	L			Stop at End of Cycle	Initiate-G/H ⌐ End-G/H ⌐

X = don't care

When halted, the circuit will complete the programmed phase count and stop. The G/H can go high to stop the part any time during the last set of output phase signals until the minimum setup time before the master clock rising edge that terminates the last phase. The circuit is initialized afterward in this mode by returning G/H to a low state and supplying another start input signal.

b. STOP ON PHASE – is also a continous cycle operation. It is controlled by G/H = L and SC/SP = H. As with the previous Stop at End of Cycle, the MC10802 is initialized with a start signal and continues cycling until halted by taking the G/H input high. However, in this operating mode the circuit stops on the phase during which G/H goes high, again observing minimum set up times.

c. SINGLE CYCLE – is a diagnostic function selected by G/H = H and SC/SP = L. Initially all phase outputs are stationary at a high state. Upon receiving a start signal, the MC10802 goes through one complete cycle of phases, terminating after the last programmed phase (see Figure 5). Each following start signal sequences the circuit through one complete cycle.

d. SINGLE PHASE – is also a diagnostic function and is selected by G/H = H and SC/SP = H. A start input signal advances the MC10802 one output phase from its present position. Several start signals cause the circuit to cycle through the programmed number of phases, moving forward one phase for each start.

If a Single Phase or Stop on Phase operation stops the MC10802 on a phase other than the final selected phase, future operations begin from that point. For example, if a four phase pattern is stopped on $\phi 2$, any new operation other than reset starts with ϕ 3.

3. RUN MODE – is selected by the R/M input in the low state. The four operations in the run mode differ from the maintenance mode only in the initiation source for Stop on Phase and Stop at End of Cycle (see Table 3). These operations are initiated with the G/H input going to a low state and do not require a start input signal. Stop on Phase and Stop at End of Cycle are terminated by the G/H line going high as with the maintenance mode. Select line changes should be synchronized with the master clock to maintain proper set-up and hold time. Single Cycle and Single Phase operations are exactly the same as in the maintenance mode and require a start signal to initialize the operation.

TS7 controls the output phase duration during a Single Phase or a Stop on Phase Operation. If TS7 is at a logic low state, the phase output returns to a high state after its normal pulse width low. If TS7 is a logic high, the final phase of Stop on Phase or the Single Phase output remains low (Figure 6). Keeping an output low is used for diagnostics during partial computer cycle to trace data, delay clocking of registers, enable buses, etc. If a phase output has been held low, returning TS7 to a logic low causes the phase output to be clocked high with the Master Clock. Table 4 gives the Truth Table for TS7.

The CYCLE COMPLETE OUTPUT (CC) shows the operational status of the MC10802. This output indicates when the circuit is not running and is in the initial condition. Cycle complete goes high as a result of (1) a reset, (2) a completed Stop at End of Cycle operation, or (3) a completed Single Cycle operation. Cycle complete is not given during a running condition as one cycle immediately follows another. Table 5 shows Cycle Complete output status with Figures 5 and 6 giving timing examples.

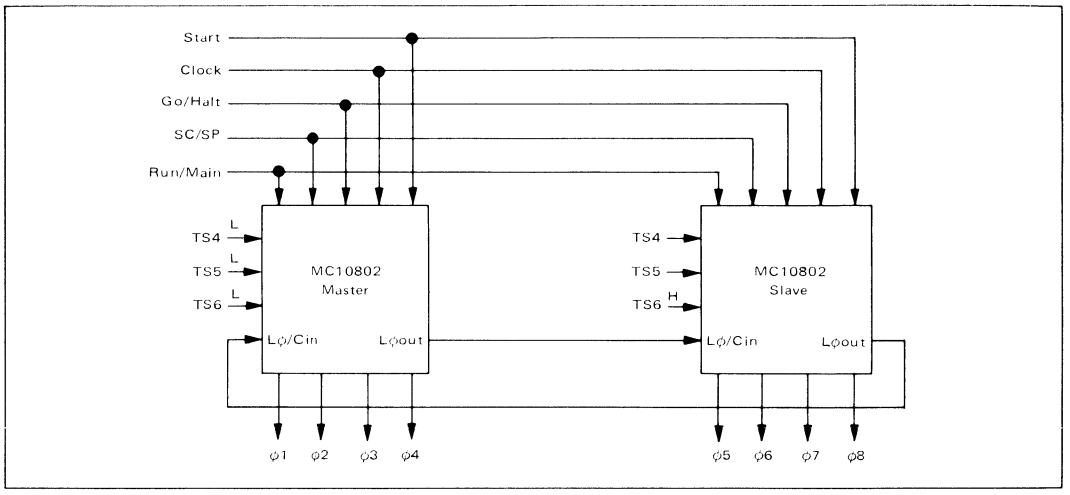
TABLE 4 – TS7 TRUTH TABLE

TS7	Function
L	Normal Phase duration
H	Wide phase duration

TABLE 5 – CYCLE COMPLETE

CC Output	Status
H	Complete
L	Running

FIGURE 2 – CASCADING CIRCUITS



CASCADING DEVICES

Two or more MC10802's can be cascaded for greater than four (4) phases. Figure 2 shows an example of two devices.

Select line TS6 is used to establish a "master-slave" relationship between the cascaded circuits. Only the first device is related as the master stage, all others are programmed as slave stages. A single device is treated as a master stage.

Additionally, the Last Phase Out (Lϕout) and Carry In (Lϕ/Cin) lines are connected for coupling between devices. In the Figure 2 example, the master stage Lϕout is connected to the slave stage Lϕ/Cin, and similarly, the slave stage Lϕout is returned to the master stage Lϕ/Cin. This daisy chain technique can be extended to multiple devices in which the Lϕout of the last device is always returned to the master. **Single device operation requires that Lϕout be returned to Lϕ/Cin of the same circuit.**

Last Phase Out is coincidental with the last programmed phase as selected by TS4 and TS5, Table 1.

TABLE 6 – SELECT LINE TS6

TS6	Function
L	Master Stage (1st)
H	Slave Stage (Other)

If the last phase is double width as selected by TS0 through TS3, Lϕout is present during the last full phase time independent of TS7 (See Figure 6), only for the second half and is one clock period in duration. When using SINGLE PHASE operation, Lϕout is present.

For normal system operation, clock phase programmability should be limited to the last MC10802 in a chain. The Figure 2 example shows a range of 5 to 8 phases. Programming the first stage results in missing phase outputs; such as ϕ1, ϕ2, ϕ5, ϕ6, etc., if the master device is programmed as a 2ϕ example. This feature can be used for programmable time delay applications (Figure 2 has a total range of 2 through 8).

CIRCUIT OPERATION WAVEFORMS

MC10802 operation can be illustrated by waveforms showing the various timing modes. The following waveforms are based on the circuit being connected as in Figure 3. These examples are designed to show circuit operation and do not represent any particular system clocking patterns.

The Start input goes directly to a start synchronizer circuit built from two master slave flip-flops. This gives the MC10802 an internal start signal one clock period wide that is synchronized to the main clock as shown in Figure 4. Internal start normally occurs on the first positive going clock edge after the start input, but will occasionally fall on the second positive edge due to set up times required for the internal flip flops.

An asynchronous start signal must be high for at least one master clock period to insure the start input is present during a positive going master clock edge. There is no maximum duration for the start input. A start signal synchronized to the master clock must follow the set up and hold times around the positive going master clock edge.

FIGURE 3 – INTERCONNECTIONS

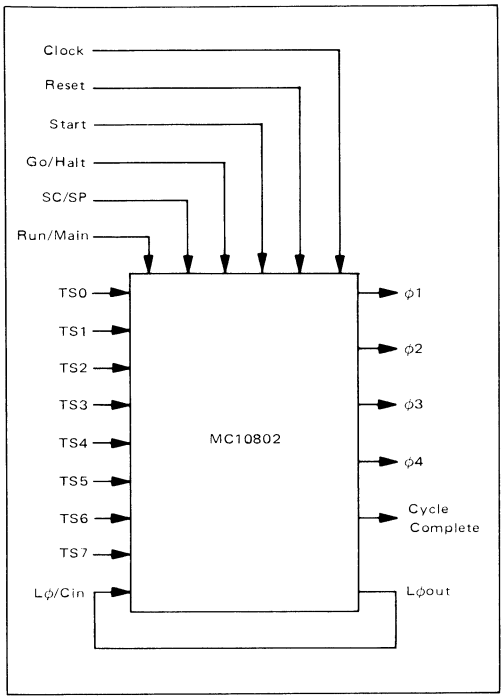


Figure 5 shows operation in the MAINTENANCE mode requiring a start signal to initialize any operation. The circuit has been reset at the start of the sequence, insuring phase one occurs first. With G/H in the GO mode a start input causes the MC10802 to begin continuous operation generating all four phases in this example. A HALT condition on the G/H input causes the circuit to complete the present cycle, SC/SP in the SINGLE CYCLE position, and stop as signified by Cycle Complete. With G/H remaining in the HALT position a start signal causes the MC10802 to go through one complete cycle of four phases and then stop. Both the continuous run or single cycle step can be repeated in any sequence.

Figure 6 shows operation in the **Run** mode which starts operation on the first positive going clock edge after G/H is in the **Go** position. The Circuit will continue to cycle with three phases and a double duration on the third phase as programmed in this example. When G/H is moved to **Halt** the circuit will stop on phase, $\phi 2$ in this illustration, because SC/SP is in the **Single Phase** position. A **Go** input would cause the MC10802 to being operation on the next positive going clock with phase two changing to phase three, etc.

With the circuit at **Halt** and in **Single Phase**, a start signal caused the part to advance one phase as shown in the Figure. When stepping phase-to-phase, it is possible to have either a wide phase pulse or a normal width pulse as controlled by TS7 and shown by the dotted line in Figure 6. Last phase out is present during the second half of a double width last phase and is present continually when halted on the last phase as discussed in the earlier Cascading Circuits section. Finally, in the **Single Phase** mode there is no Cycle Complete signal. The MC10802 operates as if it were continually running with **Halt** being an extended duration of the halted phase.

Examples given in Figures 5 and 6 are only two of the various operating modes. It is possible to have any combination of **Run/Maintenance, Single Cycle/Single Phase,** number of phases and phase durations to meet system requirements.

FIGURE 4 – START SYNCHRONIZER

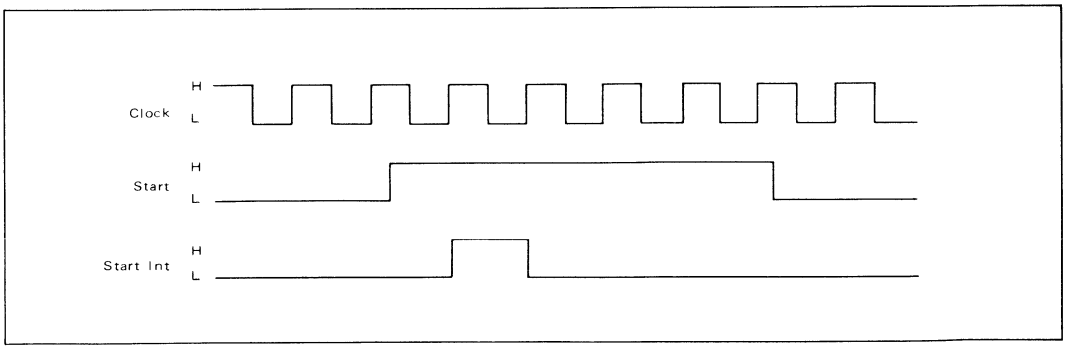


FIGURE 5 – MAINTENANCE MODE WAVEFORMS

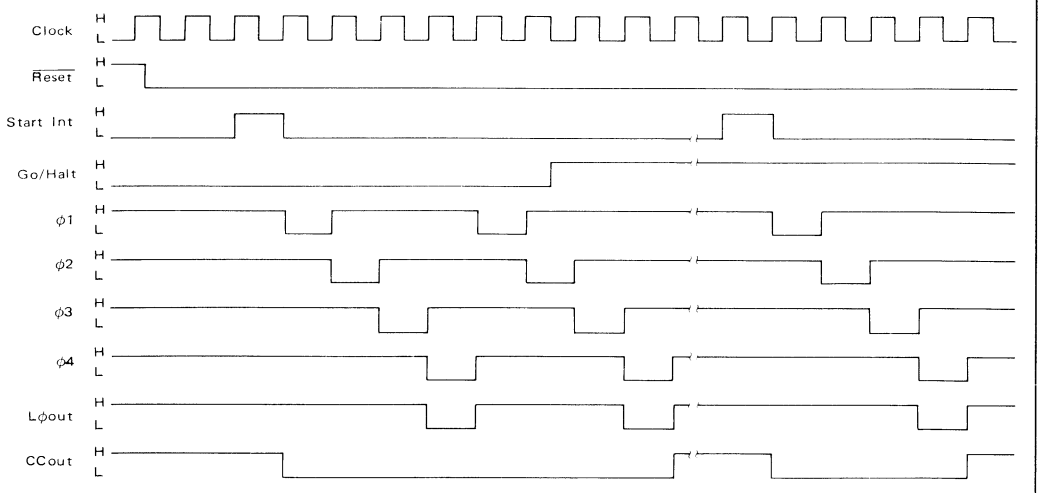
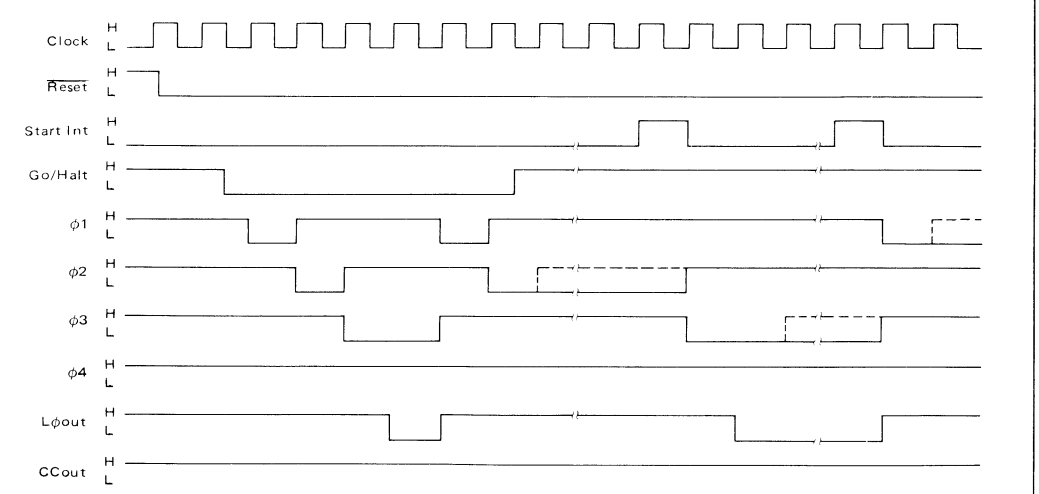


FIGURE 6 – RUN MODE WAVEFORMS



PROPAGATION DELAYS (Nanoseconds at 25°C)

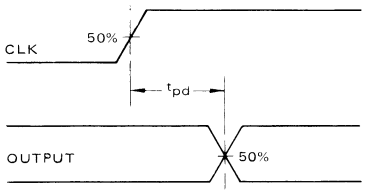
Path	Typ
Master Clock to Phase Outputs	7.5
Master Clock to Lϕout	9.0
Master Clock to CCout	6.4
$\overline{\text{Reset}}$ to Phase Outputs	6.8
$\overline{\text{Reset}}$ to Lϕout	7.5
Maximum Master Clock Frequency	36 MHz

TYPICAL SETUP AND HOLD TIMES (Nanoseconds at 25°C)

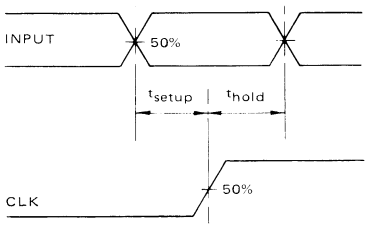
	t_{setup}	t_{hold}
TS4 to Master Clock	8.0	-6.0
TS5 to Master Clock	8.0	-6.0
Go/Halt to Master Clock	-1.5	0.5
Start to Master Clock	-5.0	5.8
Lϕ/Cin to Master Clock	3.0	10

SWITCHING WAVEFORMS

PROPAGATION DELAYS



SETUP AND HOLD



TEST PROCEDURE:

a) Establish setup time with long t_{hold}.

b) Keeping the leading edge of the input constant (t_{setup}) vary the trailing edge of the input to determine t_{hold}.

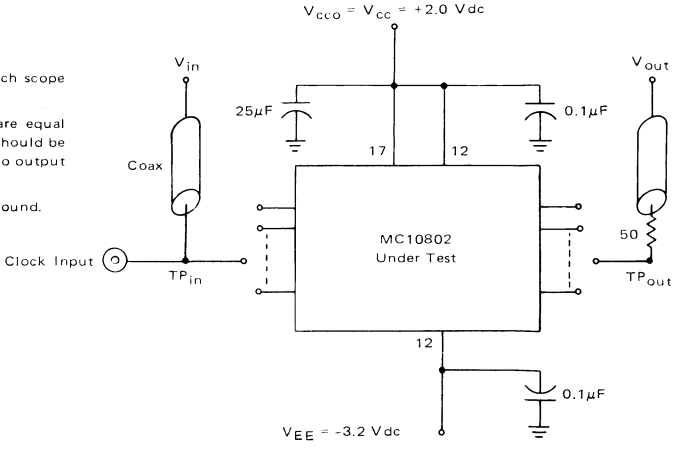
NOTE: t_{setup} and t_{hold} as defined are positive. Internal delays in the data path may result in a shift of the data waveform to the left, with respect to the clock, resulting in negative hold times.

SWITCHING TIME TEST CIRCUIT

50 ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be $\leq$¼ inch from TP_{in} to input pin and TP_{out} to output pin.

All unused outputs loaded with 50 ohms to ground.



RECOMMENDED OPERATING CONDITIONS – MC10802

Parameter	Symbol	Value	Unit
Supply Voltage (V_{CC} = 0 Volts)	V_{EE}	−4.68 to −5.72	Vdc
Operating Temp. (Functional)	T_A	−30 to +85	°C
Max Output Drive	–	50Ω to −2.0 Vdc	–
Maximum Clock Input Rise and Fall Time (20% to 80%)	t_r, t_f	10	ns
Minimum Clock Pulse Width	PW	5	ns

ELECTRICAL CHARACTERISTICS

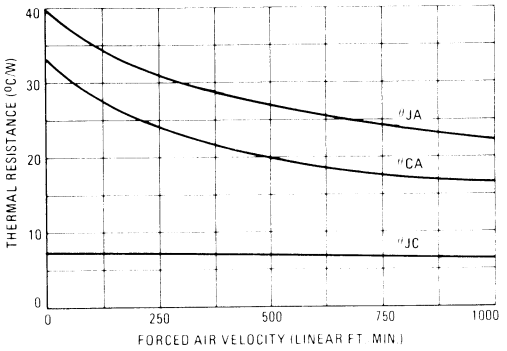
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
−30°C	−.890	−1.890	−1.205	−1.500	−5.2
+25°C	−.810	−1.85	−1.105	−1.475	−5.2
+85°C	−.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_{EE}	12	–	–	–	–	141	–	–	mAdc					12	1, 24
Input Current	I_{inH}	5	–	–	–	–	320	–	–	µAdc	5	–			12	1, 24
		13	–	–	–	–	310	–	–	µAdc	13		–		12	1, 24
	I_{inL}	5	–	–	0.5	–				µAdc	–	5	–	–	12	1, 24
Logic "0" Output Voltage	V_{OH}	2	−1.060	−.89	−.960	–	−.810	−.890	−.700	Vdc	*5,8,9,10, 11,18	7,13,14,15, 19,20			12	1, 24
Logic "1" Output Voltage	V_{OL}	2	−1.89	−1.675	−1.85	–	−1.65	−1.825	−1.615	Vdc	*8,9,10, 11,18	5,7,13,14, 15,19,20			12	1, 24
Logic "0" Threshold Voltage	V_{OHA}	2	−1.08	–	.980	–	–	−.910	–	Vdc	*8,9,10, 11,18	7,13,14,15, 19,20	5	–	12	1, 24
Logic "1" Threshold Voltage	V_{OLA}	2	–	−1.655	–	–	−1.63	–	−1.595	Vdc	*8,9,10, 11,18	7,13,14,15, 19,20		5	12	1, 24

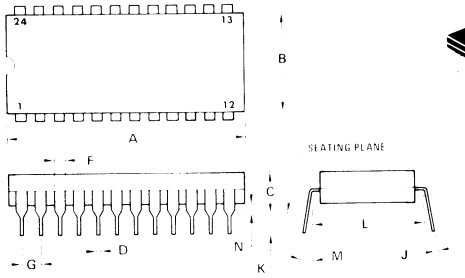
*Apply pulse ⎍ to $\overline{\text{Reset}}$ Pin 17, then
apply pulse ⎍ to CLK Pin 6, then test.

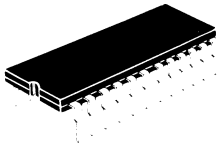
THERMAL CHARACTERISTICS (TYPICAL)



PACKAGE DEMINSIONS

CASE 623-03





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.29	4.06	0.090	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL)

MOTOROLA Semiconductors

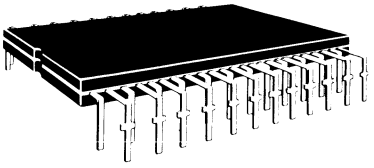
MC10803

INTRODUCTION

The MC10803 Memory Interface Function is an LSI building block for interfacing a high speed processor system to main memory or peripheral equipment. The circuit contains the logic and storage registers for generating memory address and routing incoming or outgoing data. Each part is 4-bits wide and can be connected in parallel to meet wider system I/O word requirements. An internal ALU allows the MC10803 to also assume processor ALU responsibility for many controller applications. Maximum system flexibility is maintained with 5 separate data ports.

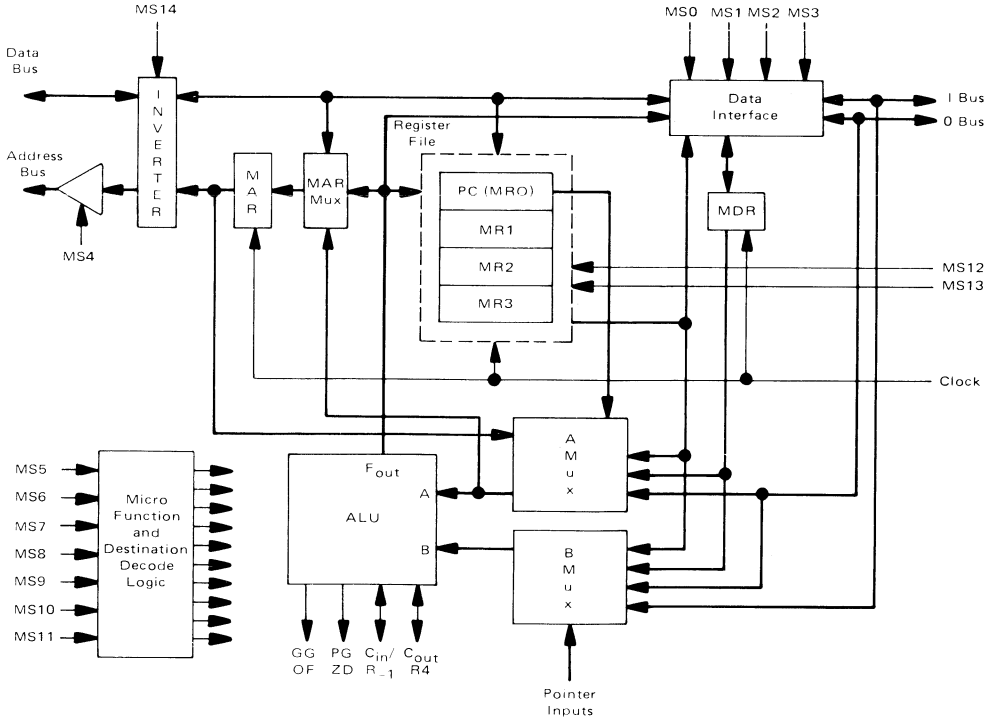
The Memory Interface Function as shown in the block diagram below contains six 4-bit registers, an ALU with encoded function/operand select logic, and data transfer circuitry on a single MECL bipolar LSI circuit. Fifteen select (MS) lines control register selection, 13 basic ALU functions, and 17 data transfer operations.

MECL — LSI MEMORY INTERFACE FUNCTION



CASE 725-01

MEMORY INTERFACE FUNCTION
BLOCK DIAGRAM – MC10803



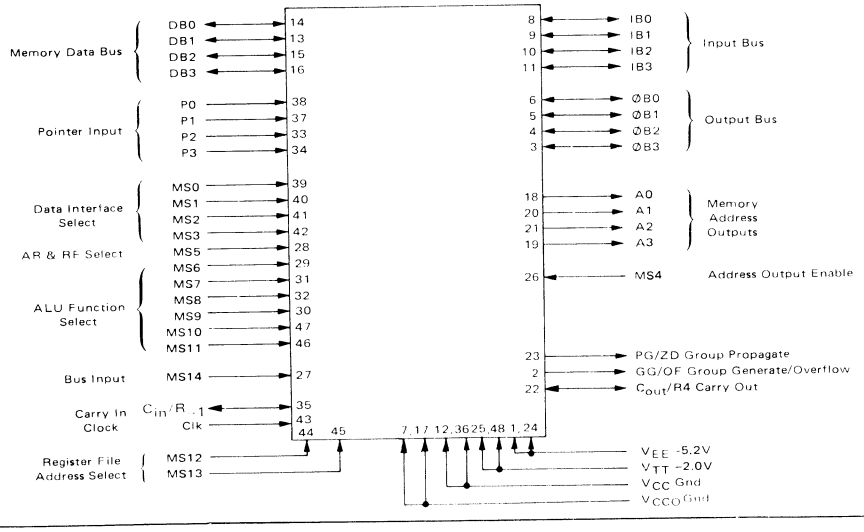
DS 9498
(Formerly ADI 435)

TABLE OF CONTENTS

IMPORTANT FEATURES

1. Internal ALU for address generation
   a. 13 arithmetic, logic and shift functions
   b. 7 separate ALU operands
2. Four word register file
   a. Program counter
   b. 3 general purpose registers for index registers, stack pointers, etc.
3. Memory data register
4. Memory address register
5. 17 data transfer and storage operations
6. 4 bits wide and fully expandable
7. 5 data ports for maximum versatility
8. Internal Register File can be expanded by using External Register File connected to the I Bus and O Bus.
9. Fully compatible with MECL 10000
   a. Power supplies
   b. Logic levels

INPUT/OUTPUT DIAGRAM-MC10803



ABSOLUTE MAXIMUM RATINGS (see Note 1)

RATING		SYMBOL	VALUE	UNIT
Supply Voltage (V_{CC} = 0)		V_{EE} V_{TT}	-8 to 0 -4 to 0	Vdc Vdc
Input Voltage (V_{CC} = 0)	Std Bus	V_{in} V_{in}	0 to V_{EE} Note 2	Vdc Vdc
Output Source Current	Cont Surge	I_O I_O	< 50 <100	mAdc mAdc
Storage Temp. Junction Temp.		$T_{stg.}$ T_J	-55 to +150 165	°C °C

NOTE: 1. Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

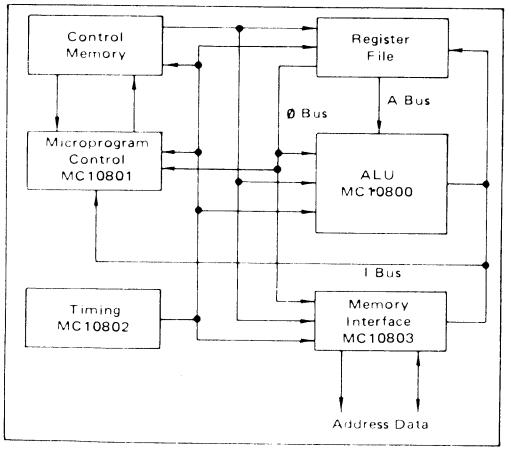
NOTE: 2. Input voltage limit is V_{CC} to −2 Volts when the bus is used as an input and the output drivers are disabled.

SYSTEM OVERVIEW

The Motorola M10800 family of LSI processor circuits combines the cost and size advantages of LSI with system design flexibility. Each family part is a major system building block which can be interconnected and programmed for a wide range of processor applications. Figure 1 illustrates a method of using the various circuits in a general purpose processor. The MC10800 4-Bit ALU Slice performs the various arithmetic, logic, and shift functions. This circuit features full BCD capability and a complete set of status outputs. The MC10801 Microprogram Control Function addresses and sequences through microprogram control memory. A set of 16 control instructions provides for direct jumps, conditional branches, and subroutines within microprogram. The MC10802 Timing Function generates clock phases and features single cycle or single phase clock increment for troubleshooting or diagnostics.

The MC10803 Memory Interface Function interfaces between the LSI processor circuits and other parts of a system. The circuit generates memory addresses and provides for the bidirectional transfer of processor data. The MC10803 represents a step forward for bipolar LSI systems by putting arithmetic capability at I/O address output port. This allows the various modes of memory addressing (relative, indexed, extended, indirect, etc.) to be performed within the MC10803 memory interface block, Figure 1, and not tie up the main ALU. It is also possible to control the program counter or do stack pointer push or pop functions inside the MC10803 again giving the register file and ALU more time for complex computations.

FIGURE 1 – MICROPROGRAMMED PROCESSOR



Within the M10800 family the MC10803 adapts to a wide variety of system functions. The Figure 1 system layout uses the MC10803 parallel with the MC10800 for maximum computational power and throughput. Besides I/O interfacing, the MC10803 ALU can be connected in parallel with the MC10800 for double precision arithmetic.

In larger systems, MC10803 blocks would be operated in parallel for multiple I/O ports and to minimize overhead burden on the processor ALU. Many peripheral controller systems perform high speed data transfer operations and do not need the computational power of the MC10800. These systems can use the MC10803 for both ALU and interface logic to minimize part count.

In some applications, the MC10803 can be used as a microprogram controller with the internal ALU for relative addressing. The circuit then generates addresses for control memory instead of main memory and uses the internal register file for storing subroutines.

The Motorola M10800 circuits interface directly to all parts in the MECL 10,000 family. This provides a source for high speed memories and a complete mix of MSI and SSI circuits. Circuits are available for special hardware functions from high speed multiply to error detection and correction.

Versatility is a main point of the M10800 Family. The block diagram in Figure 1 is intended to illustrate the purpose of the various LSI functions and not restrict the designer to any particular system configuration or application.

PIN ASSIGNMENTS

Pin Designation	Pin Number	Description
DB0	14	Data Bus-LSB I/O
DB1	13	Data Bus-NLSB I/O
DB2	15	Data Bus-NMSB I/O
DB3	16	Data Bus-MSB I/O
A0	18	Address Bus-LSB Output
A1	20	Address Bus-NLSB Output
A2	21	Address Bus-NMSB Output
A3	19	Address Bus-MSB Output
ØB0	6	Output Bus-LSB I/O
ØB1	5	Output Bus-NLSB I/O
ØB2	4	Output Bus-NMSB I/O
ØB3	3	Output Bus-MSB I/O
IB0	8	Input Bus-LSB I/O
IB1	9	Input Bus-NLSB I/O
IB2	10	Input Bus-NMSB I/O
IB3	11	Input Bus-MSB I/O
P0	38	Pointer Input-LSB
P1	37	Pointer Input-NLSB
P2	33	Pointer Input-NMSB
P3	34	Pointer Input-MSB
PG/ZD	23	Group Propagate/Zero Detect
GG/OF	2	Group Generate/Overflow
C_{in}/R_{-1}	35	Carry In/Shift LSB
$C_{out}/R4$	22	Carry Out/Shift MSB
Clk	43	Clock
MS0	39	Data Transfer Select Input
MS1	40	Data Transfer Select Input
MS2	41	Data Transfer Select Input
MS3	42	Data Transfer Select Input
MS4	26	Address Output Enable
MS5	28	AR & RF Select Input
MS6	29	Function Select Input
MS7	31	Function Select Input
MS8	32	Function Select Input
MS9	30	Function Select Input
MS10	47	Function Select Input
MS11	46	Function Select Input
MS12	44	Register File Address Select Input
MS13	45	Register File Address Select Input
MS14	27	Inverter Select Input
V_{EE}	1	-5.2 Volt Supply
V_{EE}	24	-5.2 Volt Supply
V_{TT}	25	-2.0 Volt Supply
V_{TT}	48	-2.0 Volt Supply
V_{CC}	12	Ground
V_{CC}	36	Ground
V_{CCO}	7	Ground
V_{CCO}	17	Ground

ARCHITECTURAL DESCRIPTION

The MC10803 Memory Interface Function contains 6 registers as shown in Figure 2. Three registers are given function designations; memory data register-MDR, memory address register-MAR, and program counter-PC. The other registers can be used as stack pointer, index registers, or for other memory related functions. Register assignments are not fixed and the system designer should utilize the register file as best fits the system requirements. Five 4-bit data ports (I Bus-IB, ØBus-ØB, Data Bus-DB, Address Bus-AB, and Pointer Inputs-P) are available to enter and output information. An ALU performs arithmetic, logic, and shift functions on seven possible operands (MAR, PC, RF, MDR, I BUS, ØBUS, and P). The ALU utilizes only 4 package pins for overflow, zero detect, group generate, group propagate, carry in, carry out, sign bit, shift in, and shift out. The operation of these pins is controlled by the selected ALU function. The various MC10803 sections in Figure 2 are described below.

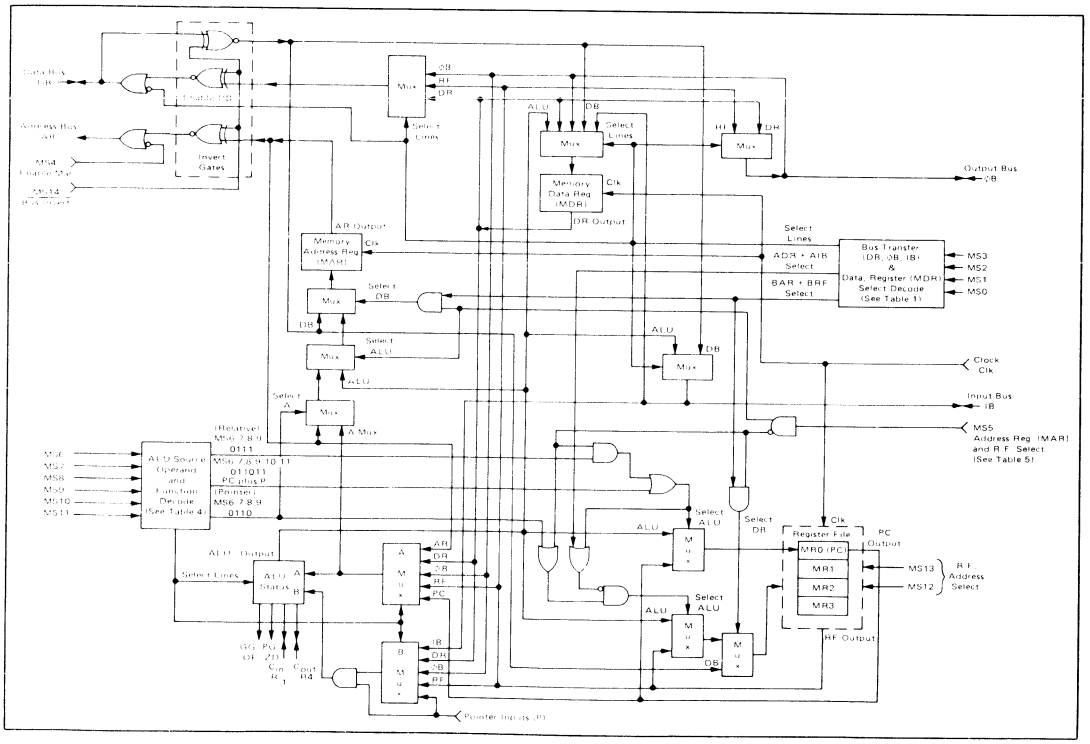
DATA INTERFACE

The data interface controls the transfer of information between various busses and registers within the MC10803.

When information is routed to a register, data is loaded on the positive going (V_{OL} to V_{OH}) clock edge. The 17 possible data transfers are listed below. Transfers numbered 12 and 13 use select line MS5 to select the Data Bus destination.

1. FØB – Register File to Ø Bus
2. RØB – Data Register to Ø Bus
3. AIB – ALU to I Bus
4. BIB – Data Bus to I Bus
5. FDB – Register File to Data Bus
6. ØDB – Ø Bus to Data Bus
7. RDB – Data Register to Data Bus
8. ADR – ALU to Data Register
9. BDR – Data Bus to Data Register
10. IDR – I Bus to Data Register
11. ØDR – Ø Bus to Data Register
12. BRF – Data Bus to Register File (MS5=0)
13. BAR – Data Bus to Address Register (MS5=1)
14. PIØ – Pipeline the I Bus to Ø Bus via the Data Register
15. PBØ – Pipeline from Data Bus to Ø Bus via the Data Register
16. PIB – Pipeline the I Bus to the Data Bus via the Data Register
17. NOP – No transfer occurs

Figure 2. Detailed MC10803 Functional Block Diagram



MR0 THROUGH MR3 – REGISTER FILE

Registers MR0 through MR3 make up a 4-word register file. Each register is 4 bits wide and expands to desired bit size with parallel MC10803 circuits. All registers are constructed from master-slave flip-flops and store information on the positive going clock edge. Register MR0 is given preferential treatment as a program counter. A separate ALU multiplexer input is used for memory addressing with the program counter. The register file can be loaded from the Data Bus or the ALU outputs. Information in the register file can be routed to the 0 Bus, Data Bus, ALU, or Address Register.

MDR – MEMORY DATA REGISTER

The Memory Data Register is the primary storage element for information going to or from the processor on the Data Bus. This register can be loaded from the Ø Bus, ALU, Data Bus, or I Bus. Destinations for information in the Data Register are Data Bus, Ø Bus, Address Register, or ALU. In addition to holding memory data, the MDR can be used as an accumulator when the MC10803 operates as the main ALU or in parallel with the MC10800 for double precision arithmetic.

MAR – MEMORY ADDRESS REGISTER

The Memory Address Register holds the outgoing memory address information. Depending on the type of memory address, this register can be loaded from the Data Bus, ALU outputs, Ø Bus, Data Register, Register File, or Program Counter. The memory address register holds information for the MC10803 address outputs and goes to the ALU for address modification.

ALU – ARITHMETIC LOGIC UNIT

The ALU features 7 basic functions: Add, Subtract, AND, OR, Exclusive OR, Shift Left, and Shift Right. These accomplish a variety of memory related tasks, including masking, bit manipulation, extended addressing, updating program counter, stack push or pop, and generating address offsets. Possible ALU operands are Ø Bus, Register File, I Bus, Data Register, Address Register, Program Counter, or the Pointer (P) inputs. Selection of the ALU function and source operands is controlled by the Microfunction Decode logic from select lines MS6 through MS11.

C_{in}/R_{-1}

During arithmetic functions this pin is the carry in to the least significant ALU bit. During shift right, R_{-1} shifts out the least significant bit. Shift left is an arithmetic operation that is accomplished by adding a word to itself.

$C_{out}/R4$

This pin is the carry out for ALU arithmetic functions. During shift operations it couples the most significant shift bit. The $C_{out}/R4$ pin contains the most significant bit for sign testing during ALU logic operations. The MSB is also brought out on arithmetic shift right because the sign bit is repeated.

PG/ZD

The PG/ZD pin serves as group propagate for fast ALU arithmetic operations and as zero detect for logic and some arithmetic functions. The selection between propagate and zero detect is controlled by the ALU function select line MS9.

GG/OF

The GG/OF pin contains group generate for all ALU arithmetic operations. In addition, the pin can be selected to display 2's complement overflow for selected arithmetic and shift left operations. A conflict between overflow and group generate is avoided by programming only the most significant slice for overflow. (See the applications section for additional information).

DATA BUS, ADDRESS BUS, AND INVERTER

The Data Bus and Address Bus are 4-bit ports. The Data Bus with bidirectional information transfer is ideal for interfacing to memory or peripheral data ports. Transfer of data on this port is controlled by the Data Interface Select lines. When not used as outputs, the data bus drivers are held at a negative logic "1", MECL V_{OL}. The Data Bus port is then available as an input using the MECL emitter-tie feature.

The Address Bus is a 4-bit port designed to output information held in the memory address register. It is placed in the MC10803 for memory and peripheral addressing, but can also be used to output ALU calculations stored in the MAR. The Address Bus is driven from an output buffer controlled by MS4. This select line (when a logic "0") forces the address outputs to a negative logic "1", MECL V_{OL}, and frees the port for other system functions.

An optional inverter controlled by MS14 is placed in series with the Data Bus and the Address Bus. In the invert mode (MS14="0"), incoming or outgoing memory data and outgoing address information is inverted. Otherwise, true data is transferred through the circuit. The invert feature allows a direct interface with any combination of positive or negative logic formats between the processor and I/O busses.

POINTER INPUTS

The P inputs are 4 input pins routed directly to the ALU. They provide a source for pointers, address modifiers, or constants as needed for memory addressing. These inputs also allow for push/pop stack operations and incrementing the program counter in byte oriented memories. When used as a main ALU, the P inputs are available for other system functions such as a register file port.

I BUS AND Ø BUS

The I Bus and Ø Bus are bidirectional data ports designed to interface between the MC10803 Memory Interface Function and other parts of the processor (Register File, ALU, Microprogram Control, etc.). Transfer of information to and from the I Bus and Ø Bus is controlled by the Data Interface select lines MS0 through MS3.

ALU SELECT AND DESTINATION DECODE

Select lines MS6 through MS11 are decoded to determine the ALU operands, the ALU function, while MS5 controls the destination for the ALU output. The ALU function select logic is designed to work in parallel with the Data Interface. This allows simultaneous data and address operations within the MC10803 for maximum system throughput. Programming information on the ALU function and Destination Decoding select lines is given in the following Functional Description tables.

Clk – CLOCK

A single clock input is common to all registers in the MC10803. Each register is built from master-slave flip-flops and loads information on the positive going (V_{OL} to V_{OH}) clock edge. Signals on the register inputs can change at any time with the clock input at either logic state and not change the register outputs. The only restriction to changing register inputs is during the set-up and hold time near the positive going clock edge. Information is held constant in any register not selected to receive a data transfer.

FUNCTIONAL DESCRIPTION

Fifteen select lines, MS0 through MS14, control the flow of information inside the MC10803 Microprogram Control Function. The following information describes programming these inputs to perform the various circuit functions. *All truth tables are expressed in negative logic with V_{OL} being a logic 1 and V_{OH} a logic 0.*

DATA TRANSFER CONTROL – MS0,MS1,MS2,MS3,MS5,MS14

Table 1 lists the 17 MC10803 data transfer functions. In addition to selecting between the BRF and BAR transfers, MS5 is used to select the memory address register data source as described later. MS14 inverts information going to and from the Data Bus. Inverting the Data Bus also inverts information between the memory address register and Address Bus.

TABLE 1. DATA TRANSFER CONTROL

MS 3	MS 2	MS 1	MS 0	MS 5	MS 14	MNEMONIC	OPERATION SOURCE	OPERATION DESTINATION	BUS OUTPUTS DB	BUS OUTPUTS IB	BUS OUTPUTS OB	NEXT STATE DR
0	0	0	0	X	X	NOP	NO OPERATION		1	1	1	—
0	0	0	1	X	X	AIB	ALU	IB	1	ALU	1	—
0	0	1	0	X	X	ØDR	ØB	DR	1	1	1	ØB
0	0	1	1	X	X	ADR	ALU	DR	1	1	1	ALU
0	1	0	0	0	0	BRF*	$\overline{DB}$	RF	1	1	1	—
				0	1		DB	RF	1	1	1	—
				1	0	BAR*	$\overline{DB}$	AR	1	1	1	—
				1	1		DB	AR	1	1	1	—
0	1	0	1	X	0	BIB	$\overline{DB}$	IB	1	$\overline{DB}$	1	—
				X	1		DB	IB	1	DB	1	—
0	1	1	0	X	0	BDR	$\overline{DB}$	DR	1	1	1	$\overline{DB}$
				X	1		DB	DR	1	1	1	DB
0	1	1	1	X	X	IDR	IB	DR	1	1	1	IB
1	0	0	0	X	0	FDB	$\overline{RF}$	DB	$\overline{RF}$	1	1	—
				X	1		RF	DB	RF	1	1	—
1	0	0	1	X	0	RDB	$\overline{DR}$	DB	$\overline{DR}$	1	1	—
				X	1		DR	DB	DR	1	1	—
1	0	1	0	X	0	ØDB	$\overline{ØB}$	DB	$\overline{ØB}$	1	1	—
				X	1		ØB	DB	ØB	1	1	—
1	0	1	1	X	0	PIB	IB	DR	$\overline{DR}$	1	1	IB
							$\overline{DR}$	DB				
				X	1		IB	DR	DR	1	1	IB
							DR	DB				
1	1	0	0	X	X	FØB	RF	ØB	1	1	RF	—
1	1	0	1	X	X	RØB	DR	ØB	1	1	DR	—
1	1	1	0	X	0	PBØ	$\overline{DB}$	DR	1	1	DR	$\overline{DB}$
							DR	ØB				
				X	1		DB	DR	1	1	DR	DB
							DR	ØB				
1	1	1	1	X	X	PIØ	IB	DR	1	1	DR	IB
							DR	ØB				

*These instructions override the ALU destination (see Table 5)

X = Don't care

— = No Change in Register State

ADDRESS OUTPUT ENABLE MS4

MS4 controls the Address Bus output drivers. The disable feature can be used for DMA operation, multiprocessors on a common memory, and other memory bus transfers. Table 2 shows the programming of MS4.

REGISTER FILE ADDRESS SELECT-MS12 AND MS13

MS12 and MS13 are used to select one of the four register file words for all register file (RF) load or read operations. The program counter (PC) operations are a special case that automatically pick MR0 and do not require MS12 or MS13. This does not inhibit selecting MR0 for any RF function. Table 3 gives the truth table for register file selection.

ALU CONTROL – MS6 THROUGH MS11

MS6 through MS11 control the ALU operand and function selection. MS6, MS7, and MS8 select the ALU function. MS9 selects the ALU function and controls the ALU status outputs. MS10 and MS11 control the ALU operand selection. Table 4 shows programming for the various ALU functions and selection of the ALU operands.

TABLE 2 – ADDRESS BUS CONTROL

MS4	MS14	ADDRESS BUS
0	–	Logic 1
1	0	$\overline{MAR}$
1	1	MAR

TABLE 3 – REGISTER FILE SELECTION

MS13	MS12	REGISTER
0	0	MR0 (PC)
0	1	MR1
1	0	MR2
1	1	MR3

TABLE 4. ALU PROGRAMMING*

	MS 6 7 8	MS 6 7 8	MS 6 7 8	MS 6 7 8	MS 6 7 8	MS 6 7 8	MS 6 7 8	MS 6 7 8
	0 0 0	0 0 1	0 1 0	0 1 1	1 0 0	1 0 1	1 1 0	1 1 1
MS 9 10 11	SUB $G_G=V\ P_G=Z_D$	ADD $G_G=V\ P_G=Z_D$	ASL $G_G=V\ P_G=Z_D$	POINTER $G_G=G\ P_G=P$	AND $C_{out}=R3\ P_G=Z_D$	OR $C_{out}=R3\ P_G=Z_D$	ASR $C_{out}=R3\ P_G=Z_D$ $G_G=1$	EOR $C_{out}=R3\ P_G=Z_D$
0 0 0	ØB Minus IB·P	ØB Plus IB·P	ØB	ØB Plus P	ØB·(IB·P)	ØB + (IB·P)	ØB	ØB ÷ (IB·P)
0 0 1	ØB Minus DR·P	ØB Plus DR·P	DR	DR Plus P	ØB·(DR·P)	ØB + (DR·P)	DR	ØB ÷ (DR·P)
0 1 0	RF Minus ØB·P	RF Plus ØB·P	RF	RF Plus P	RF·(ØB·P)	RF + (ØB·P)	RF	RF ÷ (ØB·P)
0 1 1	RF Minus DR·P	RF Plus DR·P	AR	PC Plus P	RF·(DR·P)	RF + (DR·P)	AR	RF ÷ (DR·P)
	$G_G=G_GP_G=P_G$	$G_G=G_GP_G=P_G$	LSL $G_G=G_GP_G=P_G$	RELATIVE $G_G=G_GP_G=P_G$	$C_{out}=R3\ P_G=Z_D$	EORP $C_{out}=R3\ P_G=Z_D$	LSR $G_G=1\ P_G=Z_D$	MODIFY $G_G=G_GP_G=P_G$
1 0 0	ØB Minus IB·P	ØB Plus IB·P	ØB	PC Plus IB·P	ØB · P	ØB ÷ P	ØB	AR Plus P
1 0 1	ØB Minus DR·P	ØB Plus DR·P	DR	PC Plus DR·P	DR · P	DR ÷ P	DR	AR Plus DR·P
1 1 0	RF Minus ØB·P	RF Plus ØB·P	RF	PC Plus ØB·P	RF · P	RF ÷ P	RF	AR Plus ØB·P
1 1 1	RF Minus DR·P	RF Plus DR·P	AR	PC Plus RF·P	AR · P	AR ÷ P	AR	AR Plus RF·P

*NOTE: 1. "A MUX" Operand is Left Entry, and
"B MUX" Operand is Right Entry.
2. Single Operand Instructions use "A MUX".
3. R3 = Sign Detect (MSB of ALU Output)

ALU DESTINATION CONTROL – MS5

The ALU output can be routed to several points in the MC10803. ALU to I Bus and ALU to Data Register transfers are controlled by the Data Interface, Table 1. Other MC10803 operations load the ALU output into the Memory Address Register (AR), Register File (RF), or Program Counter (PC). These transfers are determined by the selected Data Interface transfer, MS5, and the selected ALU function. Table 5 shows programming combinations for routing information to the AR, RF, and PC. Commands that transfer the selected ALU A MUX operand to the address register are designated by the letter A under the AR column.

TABLE 5 – DESTINATION PROGRAMMING

ALU OPERATION	MS 6	7	8	9	10	11	DATA INTERFACE OPERATION (SEE TABLE 1)	MS 5	DESTINATION AR	RF	PC
(POINTER)							BRF	0	A	DB	–
							BAR	1	DB	ALU	–
ØB Plus P	0	1	1	0	0	0					
DR Plus P	0	1	1	0	0	1	ADR or AIB	0	A	–	–
								1	ALU	–	–
RF Plus P	0	1	1	0	1	0	All Others	0	A	ALU	–
								1	ALU	ALU	–
(POINTER)							BRF	0	PC	DB	ALU*
							BAR	1	DB	–	ALU
PC Plus P	0	1	1	0	1	1	All Others	0	PC	–	ALU
								1	ALU	–	ALU
(RELATIVE)							BRF	0	–	DB	ALU*
PC Plus IB·P	0	1	1	1	0	0	BAR	1	DB	–	–
PC Plus DR·P	0	1	1	1	0	1					
PC Plus ØB·P	0	1	1	1	1	0	ADR or AIB	0	–	–	ALU
								1	ALU	–	–
PC Plus RF·P	0	1	1	1	1	1	All Others	0	–	–	ALU
								1	ALU	–	–
SUB	0	0	0	–	–	–	BRF	0	–	DB	–
ADD	0	0	1	–	–	–	BAR	1	DB	–	–
All ASL/LSL	0	1	0	–	–	–					
Others AND	1	0	0	–	–	–	ADR or AIB	0	–	–	–
OR/EORP	1	0	1	–	–	–		1	ALU	–	–
ASR/LSR	1	1	0	–	–	–					
EOR/MOD	1	1	1	–	–	–	All Others	0	–	ALU	–
								1	ALU	–	–

*If the PC is selected (MS12 = 0, MS13 = 0) during the indicated operation, then DB + ALU → PC

– = No change in register state.

NOTE: If MS14 = 0, replace DB with $\overline{DB}$ in Table 5.

APPLICATIONS INFORMATION

Figure 3 shows four MC10803's interconnected in a typical 16-bit configuration. A single MC10179 lookahead carry block gives second level lookahead for maximum performance. Buffers are required between carry out of the lookahead and carry out of the MC10803 so that the higher speed lookahead dominates. The buffer still permits C_{in} to C_{out} transfers required for shift right. Smaller 8 or 12-bit systems use ripple carry and do not require the MC10179 or buffers. Systems larger than 16 bits can use additional MC10179 circuits to maintain maximum performance.

The following section defines the various ALU functions and describes ways to use the part for memory addressing. Refer to Table 4 for programming and choice of operands.

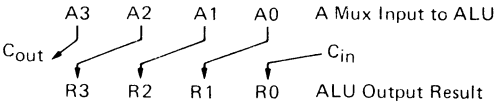
ADD-(OP A) Plus (OP B) · P Plus C_{in} = Result

SUB-(OP A) Plus $\overline{\text{(OP B)}}$ · P Plus C_{in} = Result

Add and subtract perform the logic AND using the B operand and P inputs. This is used for bit masking prior to the arithmetic operation. Lookahead carry is possible when MS9 is equal to logic 1 on the less significant MC10803's, see Figure 3. The most significant slice can have MS9 equal to logic 0 to provide 2's complement overflow without interfering with the MC10179.

ASL,LSL – SHIFT LEFT ONE BIT

The selected operand is shifted left by adding the input to itself. For an arithmetic shift left, MS9 equal logic 0, overflow is generated from a change in the sign bit. As with add and subtract lookahead carry minimizes propagation delay.



ASR,LSR – SHIFT RIGHT ONE BIT

Shift right uses the carry pins for shift coupling. MS9 is held at logic 0 for arithmetic shifting. This holds the sign bit constant and displays the sign on C_{out} of the most significant slice. Group propagate is always zero detect and group generate is held at logic 1 to disable the MC10179 in Figure 3.

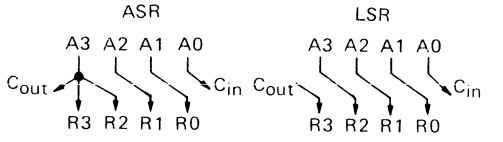
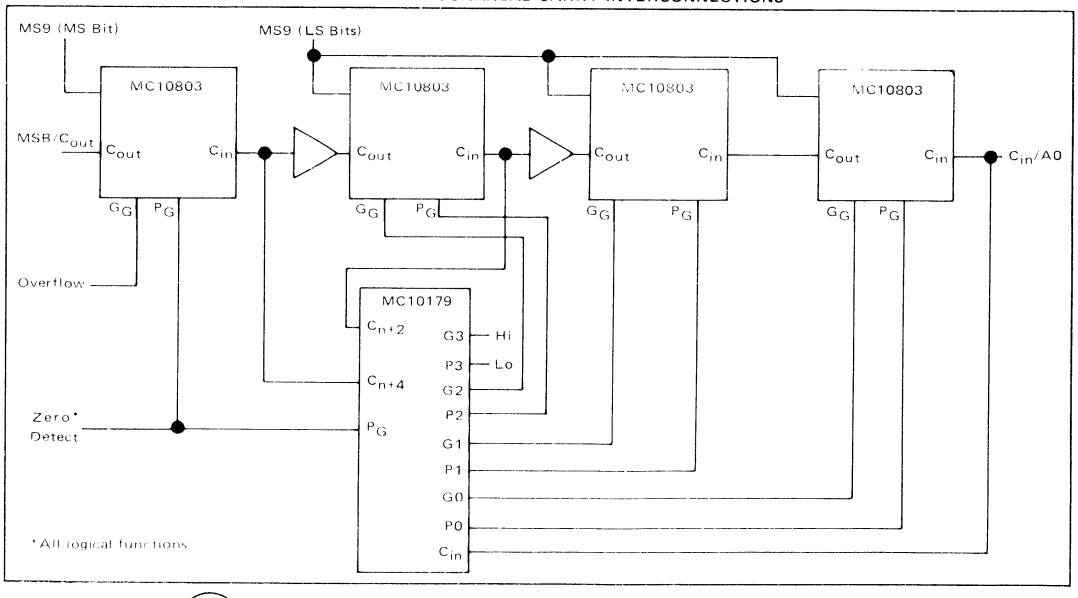


FIGURE 3. 16-BIT LOOKAHEAD CARRY INTERCONNECTIONS



MODIFY PROGRAM COUNTER-PC Plus (OP B) · P Plus C_{in} = Result

MODIFY POINTER-(OP A) Plus P Plus C_{in} = Result

MODIFY ADDRESS REGISTER-AR Plus (OP B) · P Plus C_{in} = Result

The three preceding functions are normally used with unsigned or positive numbers, and overflow is not generated. Modify Program Counter provides a means for doing a program jump from a variety of sources. The Modify Address Register gives the same jump in program capability without changing the program counter. The Modify functions are especially helpful for stack operations. The stack can directly address memory while it is simultaneously updated in the ALU. Alternately stack information can be updated, routed to the memory address register, and stored in the register file during the same clock cycle. The modify pointer format will take the P inputs and increment or decrement the program counter without disturbing other registers in the MC10803.

AND-(OP A) AND (OP B) AND P = Result

OR-(OP A) OR (OP B) AND P = Result

EOR-(OP A) EXCLUSIVE OR (OP B) AND P = Result

BIT MASK-(OP A) AND P = Result

BIT TOGGLE-(OP A) EXCLUSIVE OR P = Result

Group propagate performs zero detect and C_{out} shows the MSB for all logic functions. AND, OR, and EXOR are general purpose logic functions, allowing the MC10803 to perform compare and bit manipulation for controller applications. The Bit Mask, in addition to forcing zero bits, can be used to obtain the zero detect and sign bit status after an arithmetic function. This is accomplished when all P Inputs are a logic "1". The Bit Toggle can be used with error detection and correction circuits to correct incoming data from memory or pheripherals. Other applications include encoding or decoding for secure communications or special data formats.

STATUS AND SHIFT I/O LOGIC FUNCTION

Table 6 defines the logic equations for the status and shift conditions for each of the 16 ALU functions. The A and B inputs are selected as shown in Table 4. Table 7 defines the symbols used in the various tables.

TABLE 6 ALU OUTPUT, STATUS & SHIFT I/O

6	7	8	9	ALU FUNCTION	ALU OUTPUT $R_3\ R_2\ R_1\ R_0$	STATUS OR SHIFT I/O GG/OF	PG/ZD	C_{out}/R_4	C_{in}/R_{-1}
0	0	0	0	(SUBTRACT	A plus $\overline{B}$ plus C_{in}	OF	ZD	C_{out} (Output)	C_{in} (Input)
			1	(SEE NOTE 1)		GG	PG		
0	0	1	0	ADD	A plus B plus C_{in}	OF	ZD	C_{out} (Output)	C_{in} (Input)
			1			GG	PG		
0	1	0	0	ASL	A plus A plus C_{in}	$A_3 \oplus A_2$	ZD	C_{out} (Output)	C_{in} (Input)
			1	LSL		GG	PG		
0	1	1	0	POINTER	A plus P plus C_{in}	GG	PG	C_{out} (Output)	C_{in} (Input)
			1	RELATIVE	A plus B plus C_{in}	GG	PG		
1	0	0	0	AND	A · B	$A_3 \cdot \overline{B}_3$	ZD	R_3 (Output)	C_{in} (Input)
			1		A · P	A_3	ZD		
1	0	1	0	OR	A + B	0	ZD	R_3 (Output)	C_{in} (Input)
			1	EORP	$A \oplus P$	GG	ZD		
1	1	0	0	ASR	$A_3\ A_3\ A_2\ A_1$	1	ZD	R_3 (Output)	A_0 (Output)
			1	LSR	$R_4\ A_3\ A_2\ A_1$	1	ZD	R_4 (Input)	
1	1	1	0	EOR	$A \oplus B$	GG	ZD	R_3 (Output)	C_{in} (Input)
			1	MODIFY	AR plus B plus C_{in}	GG	PG	C_{out} (Output)	

NOTE 1: $\overline{B}_i$ is inserted for B_i in the equations below when the SUBTRACT mode is selected.

DEFINITIONS:

PG = $(A_3+B_3) \cdot (A_2+B_2) \cdot (A_1+B_1) \cdot (A_0+B_0)$

GG = $(A_3 \cdot B_3) + (A_3+B_3) \cdot (A_2 \cdot B_2) + (A_3+B_3) \cdot (A_2+B_2) \cdot (A_1 \cdot B_1) + (A_3+B_3) \cdot (A_2+B_2) \cdot (A_1+B_1) \cdot (A_0 \cdot B_0)$

$C_3 = (A_2 \cdot B_2) + (A_2+B_2) \cdot (A_1 \cdot B_1) + (A_2+B_2) \cdot (A_1+B_1) \cdot (A_0 \cdot B_0) + (A_2+B_2) \cdot (A_1+B_1) \cdot (A_0+B_0) \cdot C_{in}$

ZD = $\overline{R3} \cdot \overline{R2} \cdot \overline{R1} \cdot \overline{R0}$

$C_{out} = GG + PG \cdot C_{in}$

$OF = C_3 \oplus C_{out}$

$= C_3 (\overline{A}_3 \cdot \overline{B}_3) + \overline{C}_3 (A_3 \cdot B_3)$

Where R_i = ALU Output, Bit i; i = (LSB)0,1,2,3(MSB)
A_i = A Operand, Bit i, i = (LSB)0,1,2,3(MSB)
B_i = B Operand, Bit i, i = (LSB)0,1,2,3(MSB)
P = Pointer Inputs

PROPAGATION DELAYS (NANOSECONDS)

Path	Via	−30°C		+25°C		+85°C	
		Typ	Max	Typ	Max	Typ	Max
Cin to IB		15	21	16	22	18	24
Cin to 0F, ZD		11	18	12	19	16	25
Cin to Cout		3	8	3	8	3	9
Cout to IB		12	18	13	19	19	23
MS0, 1, 2, 3 to DB, ØB, IB		14	20	15	21	17	23
MS4, MS14 to A		6	12	7	13	9	16
MS6, 7, 8, 9, 10, 11 to PG, GG		21	28	22	29	26	37
MS6, 7, 8, 9, 10, 11 to R_{-1}		20	27	22	28	25	33
MS12, MS13 to DB, ØB		19	24	20	25	22	30
MS12, MS13 to IB	ALU	31	40	34	43	39	48
MS14 to IB		13	19	14	20	17	25
DB to IB		9	15	10	16	11	17
ØB to IB	ALU	24	31	25	32	29	38
ØB to DB		10	14	10	14	11	15
ØB, IB to 0F, ZD		19	26	20	27	22	29
ØB, IB to PG, GG		20	27	21	28	25	34
ØB, IB to R_{-1}		16	22	17	23	20	26
ØB, IB to Cout		15	21	16	22	19	25
Clk to A		10	15	10	15	11	18
Clk to DB, ØB	DR	13	18	14	19	15	20
Clk to PG, GG	RF	25	32	26	33	30	40
Clk to IB	ALU	30	37	32	39	35	42
P to PG, GG		10	16	11	17	12	18
P to 0F, ZD		11	17	12	18	13	19
P to Cout		10	16	11	17	11	18
P to IB	ALU	17	23	17	23	19	26

TABLE 7 DEFINITIONS OF SYMBOLS USED IN THE VARIOUS TABLES

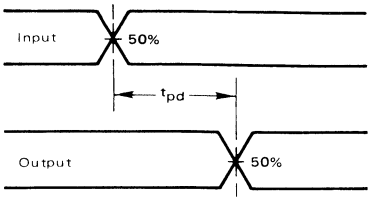
SYMBOL	MEANING
AR	Data Output of the MAR Register
DR	Data Output of the MDR Register
RF	Data Output of One of the Register File Registers as Selected by MS12 and MS13
PC	Data Output of the MRO Register Located in the Register File, PC Data Output is not Dependent on the MS12 or MS13 Select Lines
ALU or R	Data Output of the ALU
A	A Mux Output is the A Operand to the ALU
B	B Mux Output is the B Operand to the ALU (See Table 4 for the Selection of the A & B Operands)
P	Pointer Inputs to ALU
AB	Address Bus
OB	Bidirectional Ø Bus Port
IB	Bidirectional I Bus Port
DB	Bidirectional Data Bus
Plus	2's Complement Addition
Minus	2's Complement Subtraction
	Logical AND
+	Logical OR
⊕	Logical Exclusive OR

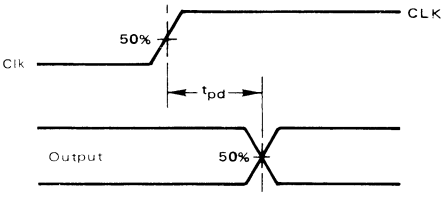
SETUP AND HOLD TIMES (NANOSECONDS OVER TEMPERATURE RANGE)

Input	Path	Setup (Min)	Hold (Min)
IB, ØB, DB to Clock	Direct	9.0	4.0
IB, ØB to Clock	via ALU	38	−7.0
C_{in} to Clock	via ALU	26	0
P to Clock	via ALU	30	−2.0
MS0, 1, 2, 3 to Clock	Direct	16	3.0
MS5 to Clock	Direct	11	4.0
MS6, 7, 8 to Clock	via ALU	20	0
MS9, 10 to Clock	via ALU	38	−6.0
MS12, 13 to Clock	Direct	11	+2.0

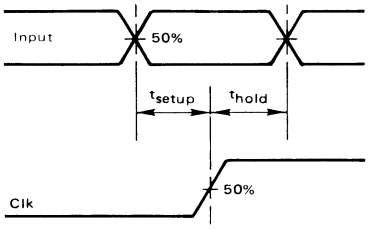
SWITCHING WAVEFORMS

PROPAGATION DELAYS





SETUP AND HOLD



TEST PROCEDURE:

a) Establish setup time with long t_{hold}.

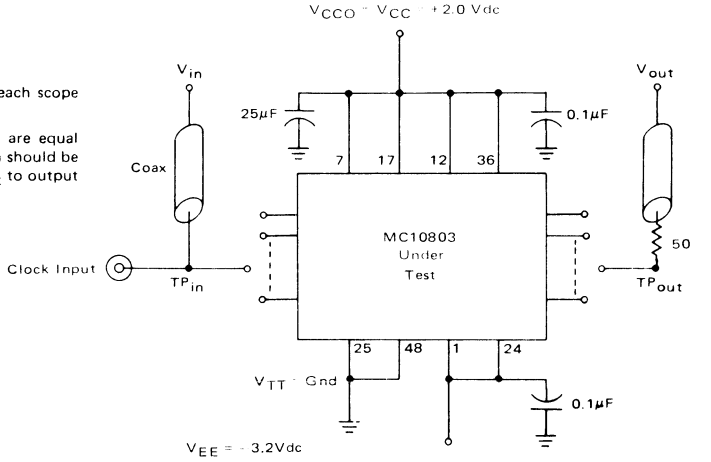
b) Keeping the leading edge of the input constant (t_{setup}) vary the trailing edge of the input to determine t_{hold}.

NOTE: t_{setup} and t_{hold} as defined are positive. Internal delays in the data path may result in a shift of the data waveform to the left, with respect to the clock, resulting in negative hold times.

SWITCHING TIME TEST CIRCUIT

50 ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin.



RECOMMENDED OPERATING CONDITIONS – MC10800

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage (V_{CC} = 0 Volts)	V_{TT} V_{EE}	−1.9 to −2.2 −4.68 to −5.72	Vdc Vdc
Operating Temp. (Functional)	T_A	−30 to +85	°C
Output Drive	—	50Ω to −2.0 Vdc	—
Maximum Clock Input Rise and Fall Time (20% to 80%)	t_r, t_f	10	ns
Minimum Clock Pulse Width	PW	5	ns

ELECTRICAL CHARACTERISTICS

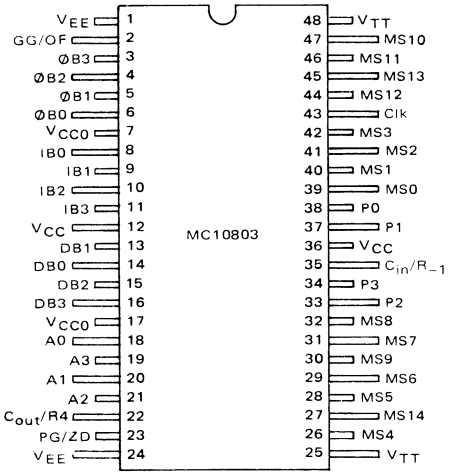
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

Characteristic	Symbol	Pin Under Test	TEST LIMITS -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE VALUES Volts: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	V_{TT}	(V_{CC}) Gnd
Power Supply Drain Current*	I_{EE}	1, 24				209				mAdc					1, 24	25, 48	7, 12, 17, 36
	I_{TT}	25, 48				256				mAdc					1, 24	25, 48	7, 12, 17, 36
Input Current	I_{inH}	33					65			μAdc	33				1, 24	25, 48	7, 12, 17, 36
		26					370			μAdc	26				1, 24	25, 48	7, 12, 17, 36
		43					545			μAdc	43				1, 24	25, 48	7, 12, 17, 36
	I_{inL}	26			0.5					μAdc		26			1, 24	25, 48	7, 12, 17, 36
Logic "0" Output Voltage	V_{OH}	8	-1.060	-.89	-.960		-.810	-.890	-.700	Vdc	14, 40, 42	27, 39, 41			1, 24	25, 48	7, 12, 17, 36
		23	-1.060	-.89	-.960		-.810	-.890	-.700	Vdc	*	30, 31, 39			1, 24	25, 48	7, 12, 17, 36
Logic "1" Output Voltage**	V_{OL}	8	-1.94	-1.675	-1.90		-1.65	-1.875	-1.615	Vdc	40, 42	16, 27, 34, 41			1, 24	25, 48	7, 12, 17, 36
		23	-1.89	-1.675	-1.85		-1.65	-1.825	-1.615	Vdc	*30	31, 39			1, 24	25, 48	7, 12, 17, 36
Logic "0" Threshold Voltage	V_{OHA}	8	-1.08		.980			-.910		Vdc	40, 42	27, 39, 41	14		1, 24	25, 48	7, 12, 17, 36
		23	-1.08		.980			-.910		Vdc	*	31, 39		30	1, 24	25, 48	7, 12, 17, 36
Logic "1" Threshold Voltage	V_{OLA}	8		-1.655			-1.63		-1.595	Vdc	40, 42	27, 39, 41		14	1, 24	25, 48	7, 12, 17, 36
		22		-1.655			-1.63		-1.595	Vdc	*	31, 39	30		1, 24	25, 48	7, 12, 17, 36

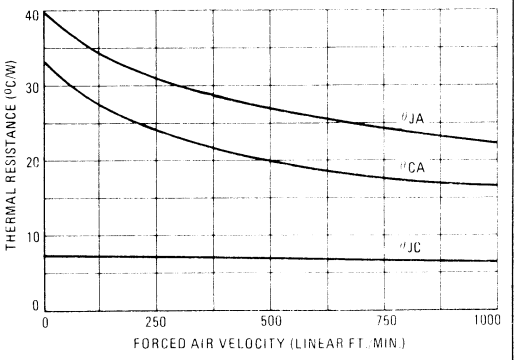
* V_{IH} on pins 3, 4, 5, 6, 29, 32, 35, 40, 41, 42, 46, 47

** The bidirectional outputs are specified at -1.90 volts for V_{OL} min

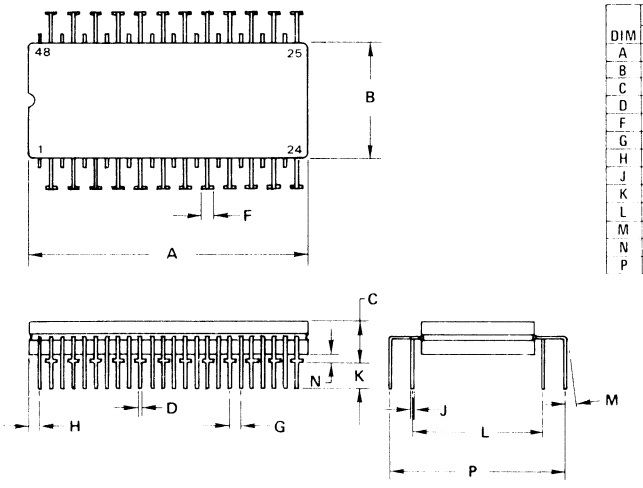
PIN ASSIGNMENT



THERMAL CHARACTERISTICS (TYPICAL)



PACKAGE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.57	5.59	0.180	0.220
D	0.38	0.53	0.015	0.021
F	1.14	1.40	0.045	0.055
G	1.27 BSC		0.050 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.54	3.30	0.100	0.130
L	15.24 BSC		0.600 BSC	
M		7°		7°
N	0.51	1.52	0.020	0.060
P	20.32 BSC		0.800 BSC	

Case 725-01

A socket for the QUIL package is available from ELECTRONIC MOLDING CORPORATION. (Part number 7178-295-5)

QUIL is a trademark of Motorola Inc.

MOTOROLA Semiconductors

MC10804
MC10805

Advance Information

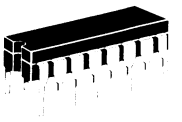
MECL – LSI
ECL/TTL INVERTING
BIDIRECTIONAL
TRANSCEIVERS WITH LATCH

INTRODUCTION

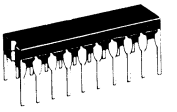
The MC10804 and MC10805 are inverting bidirectional transceivers that interface MECL logic levels with TTL logic levels. Data can be transferred directly in either direction (MECL → TTL or TTL → MECL), and an optional gated latch is also provided. Logic levels are inverted during transfers. The MC10804 is a 4-bit version in the 16-pin package, and the MC10805 is a 5-bit version in the 20-pin package.

The MC10804 and MC10805 are members of the high performance M10800 MECL/LSI processor family. They make it possible to easily interface to MOS memories, TTL compatible peripherals, or existing TTL subsystems.

- Bidirectional Translation
- Power Supplies: +5.0 Volts and 5.2 Volts
- TTL Three-State Outputs
  Sink 50 mA
  Source 5 mA
- Standard MECL 50 Ohm Drive Outputs
- Latch – Can Be Bypassed for High Speed
- High Capacitive MOS Drive Capability on MC10805

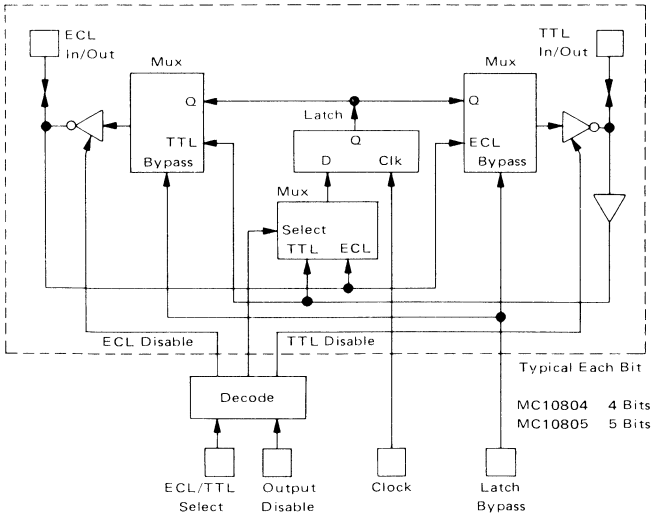


L SUFFIX
CERAMIC PACKAGE
CASE 620
MC10804

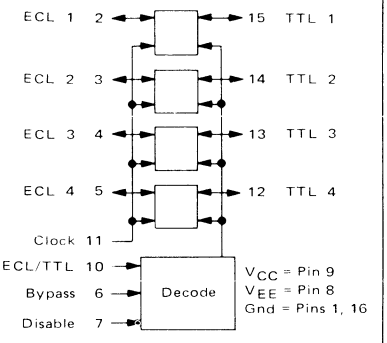


L SUFFIX
CERAMIC PACKAGE
CASE 732
MC10805

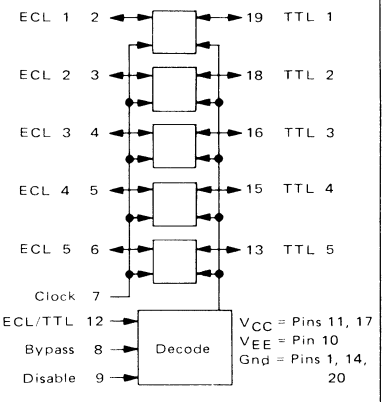
BLOCK DIAGRAM



MC10804



MC10805



This is advance information on a new introduction and specifications are subject to change without notice.

ADI-500

FUNCTIONAL DESCRIPTION

The MC10804 consists of a function decode section, a clock buffer, and four identical bit channels which perform the ECL-TTL translation. Each bit consists of a bidirectional ECL port, a bidirectional TTL port, and a latch. The MC10805 contains the same circuit blocks, but has five instead of four bits translation.

Three logic pins control the function selection. These pins, along with the clock, all operate at standard MECL levels. The block diagram and truth table define the functions. The individual pin descriptions are as follows:

Output Disable

The Output Disable, when at V_{IL}, disables both the ECL and TTL output buffers. That is, both are forced to high-impedance states. When the Output Disable is at V_{IH} the ECL/TTL translation takes place normally, and the appropriate output ports enabled by the ECL/TTL select are active. Regardless of the state of the Output Disable pin, clocked data can be loaded into the latch from the selected input port.

ECL/TTL Select

The ECL/TTL Select pin controls the direction of data transfers. When at V_{IL}, the TTL-to-ECL direction is selected. In this case, the TTL output drivers are disabled, data is input to the latch from the TTL port, and data is output onto the ECL port. When the select pin is at V_{IH}, the ECL-to-TTL direction is selected and the function is the reverse of that just described.

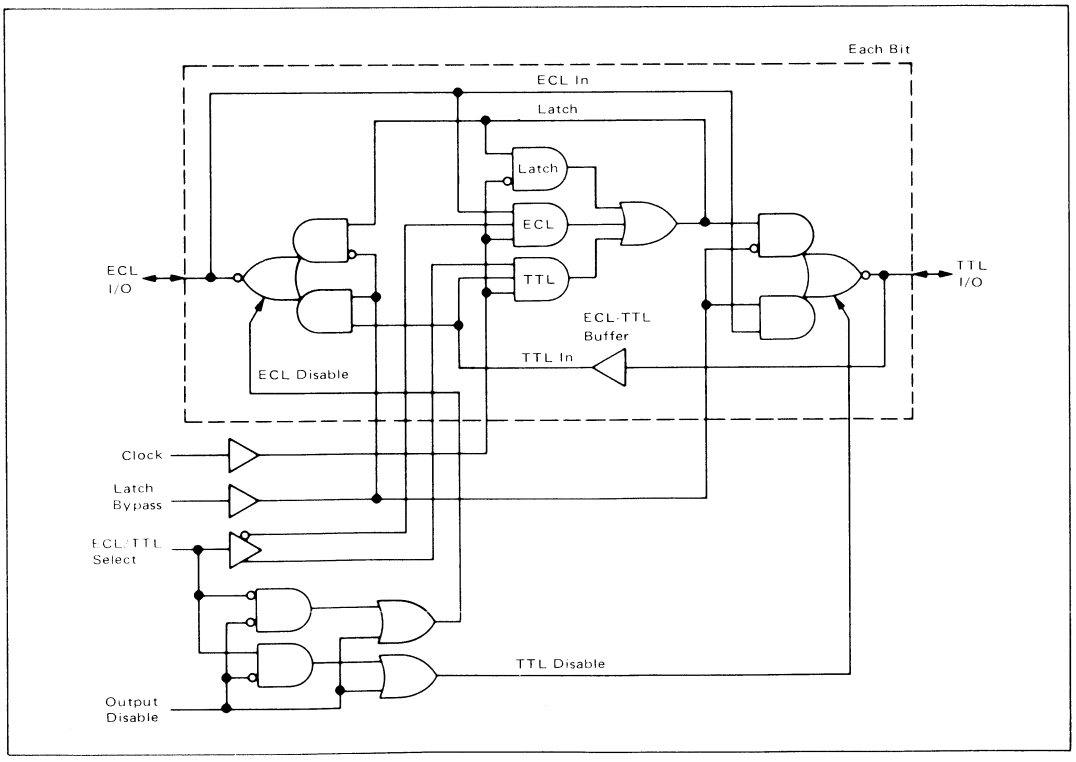
Latch Bypass

The Latch Bypass select line bypasses the latch circuitry for the fast data transfer. When the select line is at V_{IL}, the data is directed to both the latch input and the output buffer simultaneously. This feature enhances the speed of translation because the delay through the latch is bypassed. When the Latch Bypass pin is at V_{IH}, the data must first go into the latch then be sent to the output ports.

Clock

The Clock input is common to all latches and controls the storage of data. When the Clock is at V_{IL} the latch is open and data ripples through from the D input to the Q output. Data is stored or latched on the V_{IL}-to-V_{IH} transition of the Clock input.

NEGATIVE LOGIC DIAGRAM



TRUTH TABLE

SELECT INPUTS (ECL LEVELS, H = -.9V, L = -1.7V)				FUNCTION		
Output Disable	TTL/ECL Select	Latch Bypass	Clock (2)	Latch (1)	TTL I/O (H = 2.4V, L = .5V)	ECL I/O (H = -.9V, L = -1.7V)
H	H	H	H	* Q = H * Q = L	Output = $\overline{Q}$ = L = H	Off Off
H	H	H	L	Q = ECL Input = H L	Output = $\overline{Q}$ = L = H	Input = H = L
H	H	L	H	* *	Output = $\overline{ECL}$ = L = H	Input = H = L
H	H	L	L	Q = ECL Input = H L	Output = $\overline{ECL}$ = L = H	Input = H = L
H	L	H	H	* Q = H * Q = L	Off Off	Output = $\overline{Q}$ = L = H
H	L	H	L	Q = TTL Input = H = L	Input = H = L	Output = $\overline{Q}$ = L = H
H	L	L	H	* *	Input = H = L	Output = $\overline{TTL}$ = L = H
H	L	L	L	Q = TTL Input = H L	Input = H = L	Output = $\overline{TTL}$ = L = H
L	H	H	H	*	Off	Off
L	H	H	L	Q = ECL Input = H = L	Off Off	Input = H = L
L	H	L	H	*	Off	Off
L	H	L	L	Q = ECL Input = H = L	Off Off	Input = H = L
L	L	H	H	*	Off	Off
L	L	H	L	Q = TTL Input = H = L	Input = H = L	Off
L	L	L	H	*	Off	Off
L	L	L	L	Q = TTL Input = H = L	Input = H = L	Off

NOTES: (1) * Denotes "NO CHANGE" (2) Latch transfers data when clock is "L" and stores data when clock is "H".

MC10804 SETUP AND HOLD TIMES (NANOSECONDS AT 25°C)

	Setup		Hold	
	Min	Typ	Min	Typ
1. ECL1-4 to clock	--	2.0	--	4.0
2. TTL1-4 to clock	--	3.0	--	3.0
3. ECL/TTL Select to clock	--	4.5	--	1.5

MC10804 PROPAGATION DELAY TIMES (NANOSECONDS AT 25°C)

	Mode	Load	Typical	Max
1. ECL1-4 → TTL1-4	Latch Bypassed	TTL	5.0	--
2. TTL1-4 → ECL1-4	Latch Bypassed		5.5	--
3. ECL1-4 → TTL1-4	Via Latch	TTL	7.5	--
4. TTL1-4 → ECL1-4	Via Latch		8.0	--
5. Latch Bypass → TTL1-4		TTL	7.5	--
6. Latch Bypass → ECL1-4			7.0	--
7. Output Disable → TTL1-4		TTL	8.0	--
8. Output Disable → ECL1-4			7.5	--
9. ECL/TTL Select → TTL1-4		TTL	7.5	--
10. ECL/TTL Select → ECL1-4			7.0	--
11. Clock → TTL1-4		TTL	8.0	--
12. Clock → ECL1-4			7.5	--

MC10805 SETUP AND HOLD TIMES (NANOSECONDS AT 25°C)

	Setup		Hold	
	Min	Typ	Min	Typ
1. ECL1-5	—	2.0	—	4.0
2. TTL1-5	—	3.0	—	3.0
3. ECL/TTL Select	—	4.5	—	1.5

MC10805 PROPAGATION DELAYS (NANOSECONDS AT 25°C)

	Mode	Load	Typical	Max
1. ECL1-5 → TTL1-5	Latch Bypassed	TTL	5.0	
2. ECL1-5 → TTL1-5	Latch Bypassed	MOS*	14.0	
3. TTL1-5 → ECL1-5	Latch Bypassed		5.5	
4. ECL1-5 → TTL1-5	Via Latch	TTL	7.5	
5. ECL1-5 → TTL1-5	Via Latch	MOS*	16.5	
6. TTL1-5 → ECL1-5	Via Latch		8.0	
7. Latch Bypass → TTL1-5		TTL	7.5	
		MOS*	16.5	
8. Latch Bypass → ECL1-5			7.0	
9. Output Disable → TTL1-5		TTL	8.0	
		MOS*	17.0	
10. Output Disable → ECL1-5			7.5	
11. ECL/TTL Select → TTL1-5		TTL	7.5	
		MOS*	16.5	
12. ECL/TTL Select → ECL1-5			7.0	
13. Clock → TTL1-5		TTL	8.0	
		MOS*	17.0	
14. Clock → ECL1-5			7.5	

*Load = 150 pF, 413 Ω, 50% to 90%. For other load conditions, see Figure 6.

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

MC10804 RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC} V_{EE}	+4.5 to +5.5 -4.68 to -5.72	Vdc Vdc
Operating Temp (Functional)	T_A	-30 to +85	°C
Max Output Drive ECL TTL		50Ω to -2.0 Vdc V_{CC} 0.6 V @ 50 mA	
Maximum Clock Input Rise and Fall Time (20% to 80%)	t_r, t_f	10	ns
Minimum Clock Pulse Width	PW	5	ns

ELECTRICAL CHARACTERISTICS

@ Test Temperature	TEST VOLTAGE VALUES (Volts)							
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHT}	V_{ILT}	V_{CC}	V_{EE}
-30°C	-0.890	-1.890	-1.205	-1.500	+2.0	+0.8	+5.00	-5.20
+25°C	0.810	-1.850	-1.105	-1.475	+2.0	+0.8	+5.00	-5.20
+85°C	0.700	-1.825	-1.035	-1.440	+2.0	+0.8	+5.00	-5.20

Characteristic	Symbol	Pin Under Test	MC10804 TEST LIMITS -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHT}	V_{ILT}	V_{CC}	V_{EE}	Gnd	Output Condition
Negative Power Supply Drain Current	I_{EE}	8				90				mAdc							9	8	1, 16	
Positive Power Supply Drain Current	I_{CCH}	9				55				mAdc	7, 10	2,3,4,5,6								•
	I_{CCL}	9				35				mAdc		7								
Input Current	I_{inH}	15					45			µAdc	15									
		6					350			µAdc	6									
		2					485			µAdc	2									
	I_{inL}	6			0.5					µAdc		6								
ECL High Output Voltage	V_{OH}	2	-1.060	-.890	-.960		-.810	-.890	-.700	Vdc	7, 11	6, 10				15				
ECL Low Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc	7, 11	6, 10			15					
ECL High Threshold Voltage***	V_{OHA}	2	-1.080		.980			-.910		Vdc	7, 11	6		10		15				
ECL Low Threshold Voltage	V_{OLA}	2		-1.655			-1.630		-1.595	Vdc	7, 11••	10	6			15				
ECL Cutoff Voltage	V_{OLZ}	2		-1.980			-1.980		-1.980	Vdc		7								
TTL High Output Voltage	V_{OHT}	15	+2.500		+2.500			+2.500		Vdc	7, 10, 11	2, 6								-24 mA
TTL Low Output Voltage	V_{OLT1}	15		+.500			+.500		+.500	Vdc	2, 7, 10, 11	6								25 mA
	V_{OLT2}	15		+.600			+.600		+.600	Vdc	2, 7, 10, 11	6								50 mA
TTL High Threshold Voltage***	V_{OHAT}	15	+2.500		+2.500			+2.500		Vdc	7, 10	6, 11		2						-24 mA
TTL Low Threshold Voltage	V_{OLAT1}	15		+.500			+.500		+.500	Vdc	7, 10	6, 11	2							25 mA
	V_{OLAT2}	15		+.600			+.600		+.600	Vdc	7, 10	6, 11	2							50 mA
TTL Cutoff Leakage Current	I_{OHZ}	15		-100			-100		100	µAdc	2	6, 7			15					
	I_{OLZ}	15		-100			-100		-100	µAdc	2	6, 7				15				
TTL Short Circuit Current	I_{SC}	15					-170			mAdc	7, 10, 11*	2, 6							1, 15, 16	

* -5 mA sourced at output pins 12, 13, 14, 15

** Requires the following preset: V_{IH} at pin 7; V_{IL} at pins 6, 10; V_{IHT} at pin 15, then clock once (⊔).

*** TTL threshold inputs are the same as V_{IHT} and V_{ILT}

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to -2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

MC10805 RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC} V_{EE}	+4.5 to +5.5 -4.68 to -5.72	Vdc Vdc
Operating Temp (Functional)	T_A	-30 to +85	°C
Max Output Drive ECL TTL	-	50Ω to -2.0 Vdc • V_{CC} - 0.6 V @ 50 mA	-
Maximum Clock Input Rise and Fall Time (20% to 80%)	t_r, t_f	10	ns
Minimum Clock Pulse Width	PW	5	ns

*MOS drive is specified by speed vs C_L curves (MC10805 only)

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC10805 TEST LIMITS -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHT}	V_{ILT}	V_{CC}	V_{EE}	Gnd	Output Condition
Negative Power Supply Drain Current	I_{EE}	10				105				mAdc							11,17	10	1,14 20	
Positive Power Supply Drain Current	I_{CCH}	11,17				70				mAdc	9,12	2,3,4,5,6,8								•
	I_{CCL}	11,17				45				mAdc		9								
Input Current	I_{inH}	19 8 2					45 350 485			µAdc µAdc µAdc	19 8 2									
	I_{inL}	8			0.5					µAdc		8								
ECL High Output Voltage	V_{OH}	2	-1.060	-.890	-.960		-.810	-.890	-.700	Vdc	7,9	8,12				19				
ECL Low Output Voltage	V_{OL}	2	-1.890	-1.675	-1.850		-1.650	-1.825	-1.615	Vdc	7,9	8,12			19					
ECL High Threshold Voltage***	V_{OHA}	2	-1.080		-.980			-.910		Vdc	7,9	8		12		19				
ECL Low Threshold Voltage	V_{OLA}	2		-1.655			-1.630		-1.595	Vdc	7,9**	12	8			19				
ECL Cutoff Voltage	V_{OLZ}	2		-1.980			-1.980		-1.980	Vdc		9								
TTL High Output Voltage	V_{OHT}	19	+2.500		+2.500			+2.500		Vdc	7,9,12	2,8								-24 mA
TTL Low Output Voltage	V_{OLT1} V_{OLT2}	19 19		-.500 -.600			+.500 +.600		+.500 +.600	Vdc Vdc	2,7,9,12 2,7,9,12	8 8								25 mA 50 mA
TTL High Threshold Voltage***	V_{OHAT}	19	+2.500		+2.500		-	+2.500		Vdc	9,12	7,8		2						-24 mA
TTL Low Threshold Voltage	V_{OLAT1} V_{OLAT2}	19 19		-.500 -.600			+.500 +.600		+.500 +.600	Vdc Vdc	9,12 9,12	7,8 7,8	2 2							25 mA 50 mA
TTL Cutoff Leakage Current	I_{OHZ} I_{OLZ}	19 19		-100 100			-100 100		-100 100	µAdc µAdc	2 2	8,9 8,9			19	19				
TTL Short-Circuit Current	I_{SC}	19					-170			mAdc	7,9,12	2,8							1,14 19,20	

TEST VOLTAGE VALUES (Volts)

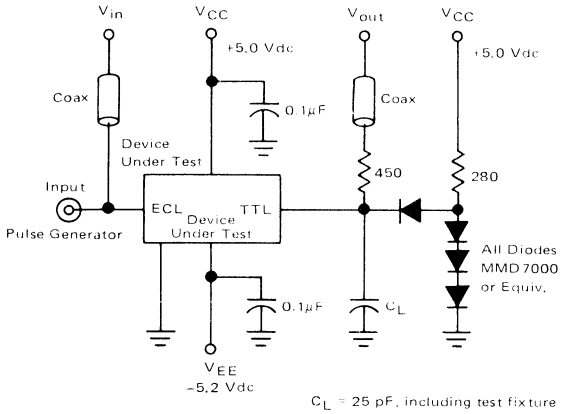
@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHT}	V_{ILT}	V_{CC}	V_{EE}
30°C	-0.890	-1.890	-1.205	-1.500	-1.20	-1.80	-5.00	-5.20
-25°C	-0.810	-1.850	-1.105	-1.475	-1.20	-1.80	-5.00	-5.20
-85°C	-0.700	-1.825	-1.035	-1.440	-1.20	-1.80	-5.00	-5.20

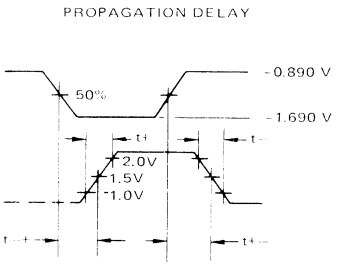
* -5 mA sourced at output pins 13, 15, 16, 18, 19

** Requires the following preset: V_{IH} at pin 9, V_{IL} at pins 8, 12, V_{IHT} at pin 19, then clock once (⊔)

*** TTL threshold inputs are the same as V_{IHT} and V_{ILT}

FIGURE 1 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C FOR PROPAGATION DELAY FROM MECL INPUT TO TTL OUTPUT WITH TTL LOAD



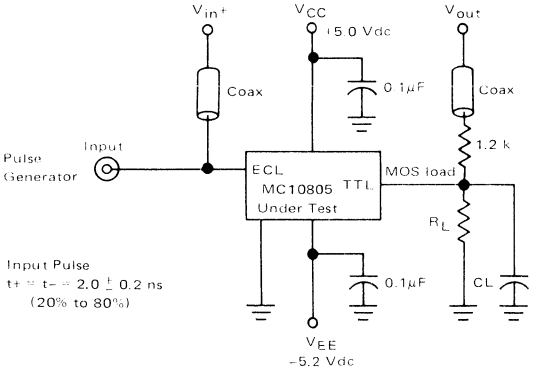


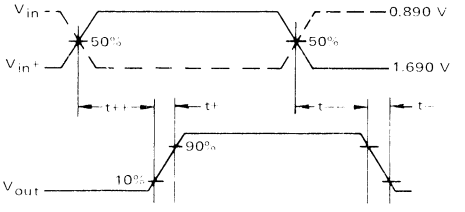
C_L = 25 pF, including test fixture

50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

FIGURE 2 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C FOR PROPAGATION DELAY FROM MECL INPUT TO TTL OUTPUT WITH MOS LOAD



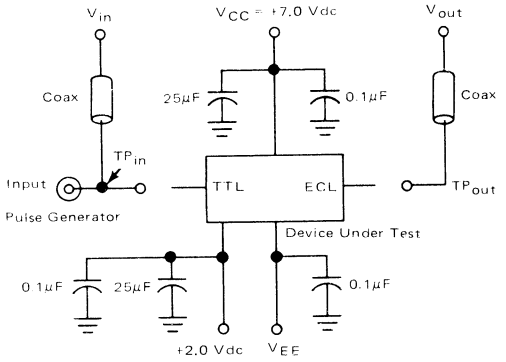


Switching times are measured after the device under test reaches a stabilized temperature (air flow ≥ 500 lfpm)

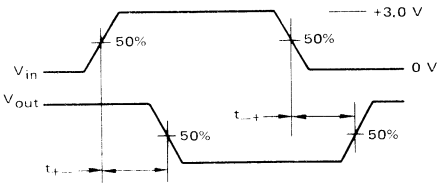
50-ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be < 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

FIGURE 3 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C FOR PROPAGATION DELAY FROM TTL INPUT TO ECL OUTPUT



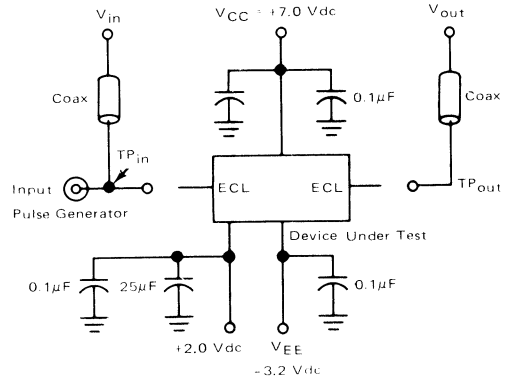
Input Pulse
$t_+ = t_- = 5.5 \pm 0.5$ ns
(10% - 90%)

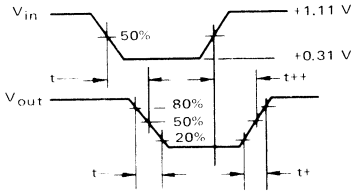


50 ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable.
Wire length should be $\leq$ 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

FIGURE 4 – SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C FOR PROPAGATION DELAY FROM ECL SELECT INPUT TO ECL OUTPUT

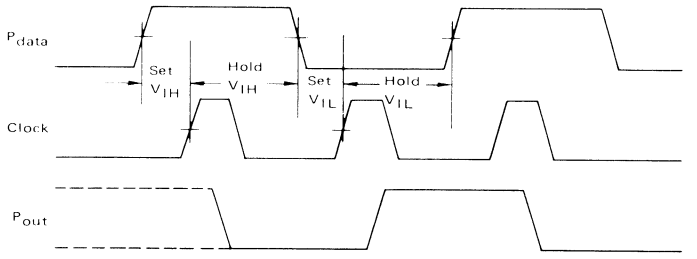




50 ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable.
Wire length should be $\leq$ 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

FIGURE 5 – SETUP AND HOLD TIME WAVEFORMS



* For These Tests, $P_{out} = \overline{P_{data}}$ in All Cases.

FIGURE 6 – MC10805 ECL → TTL DELAY (Latch Bypassed) versus CAPACITIVE LOAD (T_A = +25°C, V_{CC} = 5.0 V)

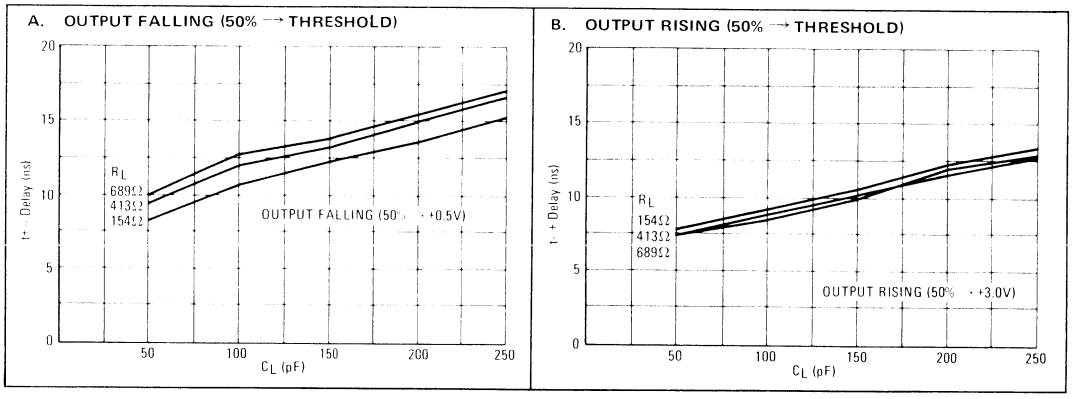
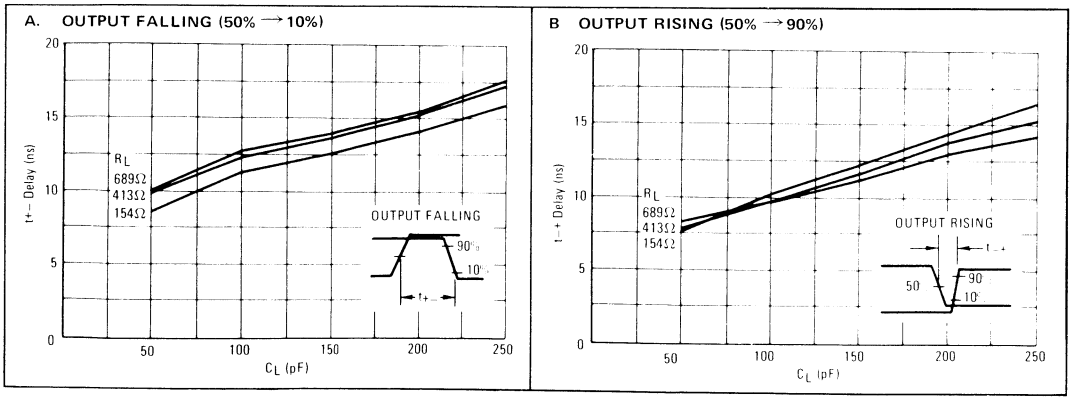
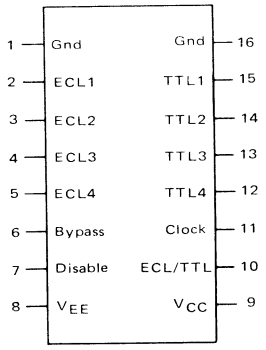


FIGURE 7 – MC10805 ECL → TTL DELAY (Latch Bypassed) versus CAPACITIVE LOAD (T_A = +25°C, V_{CC} = 5.0 V)

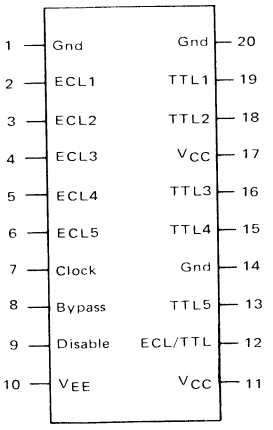


PIN ASSIGNMENTS

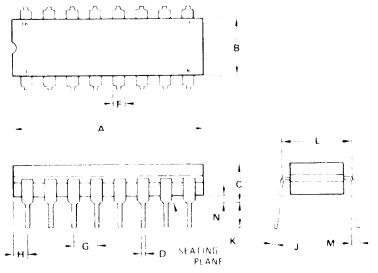
MC10804



MC10805



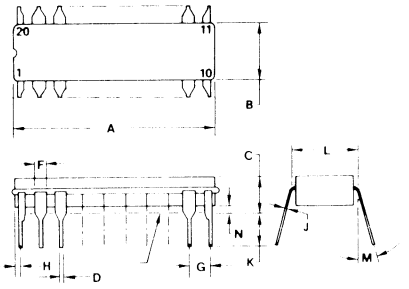
PACKAGE DIMENSIONS



NOTES
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2. PKG INDEX NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.31	0.008	0.012
K	3.18	3.30	0.125	0.160
L	7.37	7.87	0.290	0.310
M		15°	–	15°
N	0.51	1.02	0.020	0.040

CASE 620-02



NOTES
1. LEADS WITHIN 0.25 mm (0.010) DIA TRUE POSITION AT SEATING PLANE, AT MAXIMUM MATERIAL CONDITION
2. DIM L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIM A AND B INCLUDES MENISCUS

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	24.38	25.15	0.960	0.990
B	6.86	7.49	0.270	0.295
C	4.32	5.08	0.170	0.200
D	0.38	0.56	0.015	0.022
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.89	1.40	0.035	0.055
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.62 BSC		0.300 BSC	
M	5°	15°	5°	15°
N	0.51	0.76	0.020	0.030

CASE 732-02

MOTOROLA Semiconductors

MC10806

Advance Information

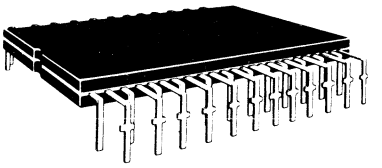
INTRODUCTION

The MC10806 Dual Access Stack is an LSI building block for digital processor systems. This circuit consists of 32 words by 9 bits of memory with two independent address and data ports. The circuit is easily expandable in both the word and bit directions making it ideal in register file, scratch pad, and high-speed buffer applications.

The Dual Access Stack, as shown in the block diagram below, contains a 32 x 9 memory array, two address ports, two 9-bit data input/output ports, two 9-bit output registers, address and data parity checking logic, and two error flip-flops in a single MECL Bipolar LSI circuit. Separate read, write, and output enables exist for each port to control all operations within the part.

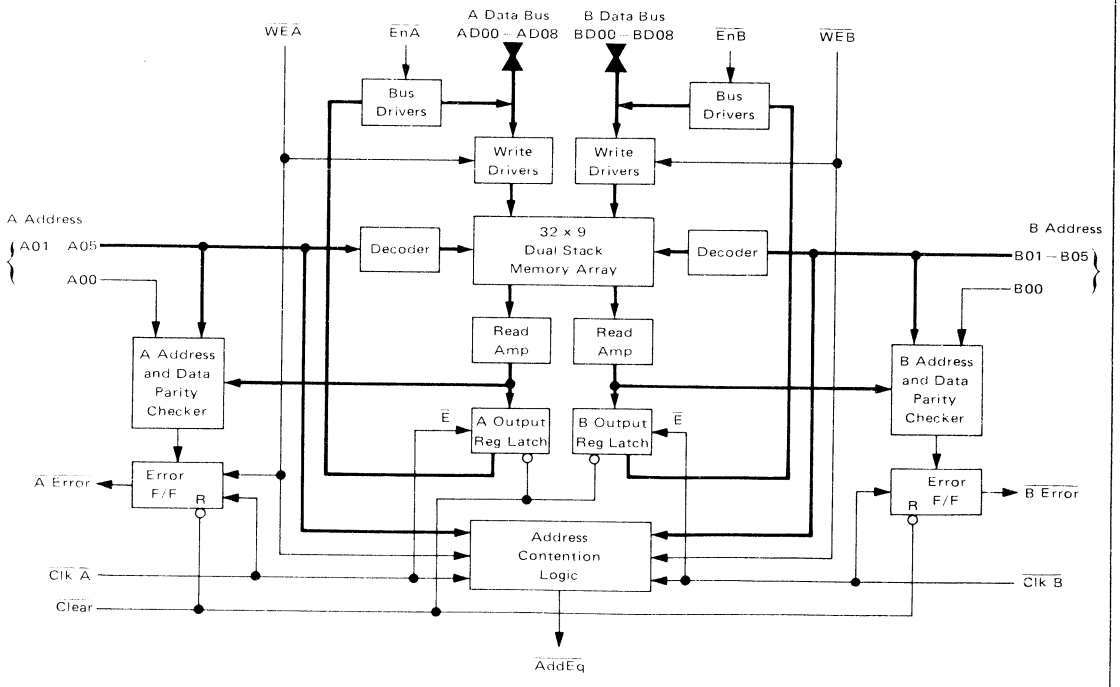
MECL — LSI

DUAL ACCESS STACK



CASE 725-01

DUAL ACCESS STACK BLOCK DIAGRAM – MC10806



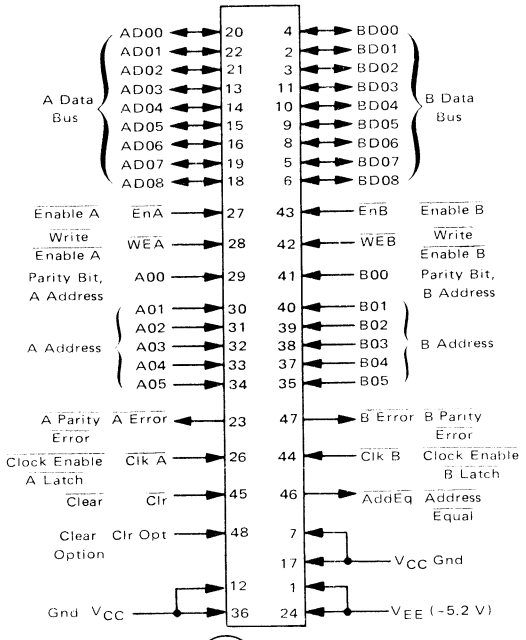
AD1-446

TABLE OF CONTENTS

IMPORTANT FEATURES

1. 32 x 9 Memory Array
2. Two 9-Bit Output Registers (Latches)
3. Two Independent Address Ports
4. Two Data I/O Ports
5. Address and Data Parity Checking Logic
6. Two Master/Slave Error Flip-Flops
7. Separate Read, Write, and Output Enables for Each Part
8. Each Part is 9-Bits Wide (One Byte) and Can Be Operated in Paralle! to Form Any Word Size in Increments of 9 Bits
9. Fully Compatible with the MECL 10,000 Family

INPUT/OUTPUT DIAGRAM



ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating		Symbol	Value	Unit
Supply Voltage (V_{CC} = 0)		V_{EE}	-8 to 0	Vdc
Input Voltage (V_{CC} = 0)	Std	V_{in}	0 to V_{EE}	Vdc
	Bus	V_{in}	Note 2	Vdc
Output Source Current	Cont	I_{out}	≤ 50	mAdc
	Surge	I_{out}	≤ 100	mAdc
Storage Temperature		T_{stg}	-55 to +150	°C
Junction Temperature		T_J	165	°C

NOTES: 1. Permanent device damage may occur, if absolute maximum ratings are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

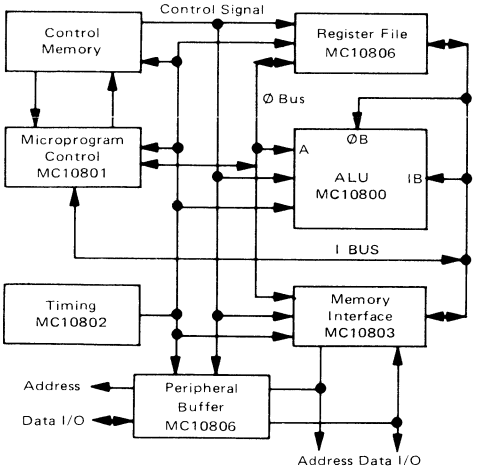
2. Input voltage limit is V_{CC} to -2 Volts when the bus is used as an input and the output drivers are disabled.

SYSTEM OVERVIEW

The Motorola M10800 family of LSI processor circuits combines the cost and size advantages of LSI with system design flexibility. Each family part is a major system building block which can be interconnected and programmed for a wide range of processor applications. Figure 1 illustrates a method of using the various circuits in a general-purpose processor. The MC10800 4-Bit ALU Slice performs the various arithmetic, logic, and shift functions. This circuit features full BCD capability and a complete set of status outputs. The MC10801 Microprogram Control Function addresses and sequences through microprogram control memory. A set of 16 control instructions provides for direct jumps, conditional branches, and subroutines within microprogram. The MC10802 Timing Function generates clock phases and features single-cycle or single-phase clock increment for troubleshooting or diagnostics.

The Register File has been made a separate block so that the designer can optimize the size and configuration for his particular system. The main function of the Register File is to provide storage for addresses and data. Also, the access time of the Register File must be fast in order to efficiently utilize the high speed of the overall processor system.

FIGURE 1 – MICROPROGRAMMED PROCESSOR



The MC10806 Dual Access Stack provides the register-file function in the processor as well as providing a memory buffer interface to peripheral devices. The MC10806 contains 32 words by 9 bits of memory in which 2 words can be independently addressed for read or write operations on two separate data I/O ports. Also, the circuit has the ability to check for parity errors on both the address and the data.

In the Register File block of the processor configuration shown in Figure 1, the two Data I/O ports of the MC10806 are connected to the two internal busses of the processor, the I Bus and the Ø Bus. The addresses and control signals are connected to the Control Memory. In the configuration shown, two locations of register file can be operated on by the ALU when the clock is at "0" with the result placed on the I Bus when the block is at "1", so that it may be written back into the register file in the same microcycle. More details for this configuration are given in the Application section.

In the Peripheral Buffer block, the MC10806 can be used as a temporary buffer for storing data from the processor to the peripheral device or vice versa. One Data I/O and Address port of the MC10806 is connected to the Data I/O and Address port of the MC10803. The other Data I/O and Address port are controlled by the peripheral device independent of the processor. In this application, the processor can read and write data into the peripheral buffer at high speed using the MC10803, while the peripheral device can read and write into buffer at a slower or faster speed independent of the processor. Flag status and interrupt conditions could also be designed into the peripheral interface depending on the application requirements.

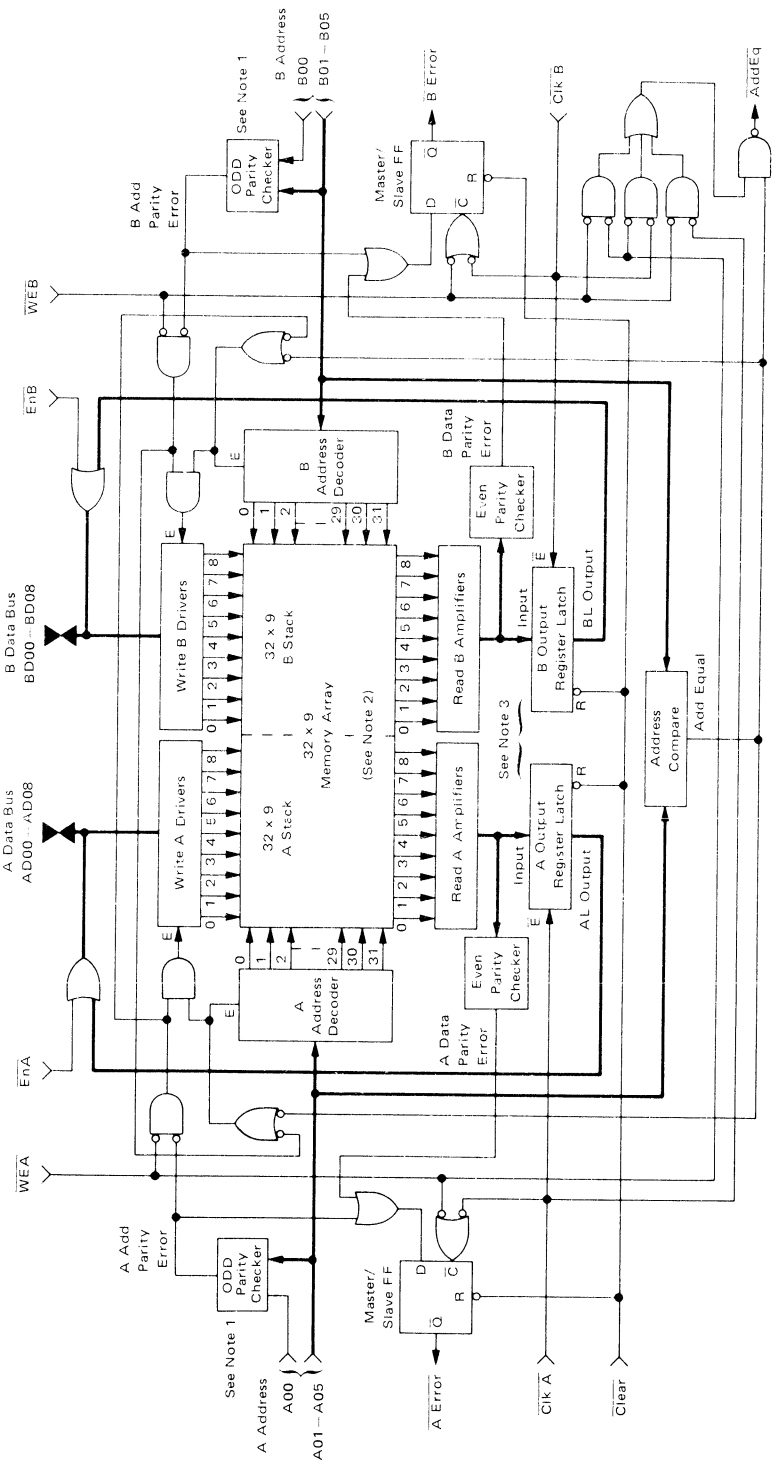
The Motorola M10800 circuits interface directly to all parts in the MECL 10,000 family. This provides a source for high-speed memories and a complete mix of MSI and SSI circuits. Circuits are available for special hardware functions from high-speed multiply to error detection and correction.

Versatility is a key word to describe each circuit in the Motorola M10800 family. The block diagram in Figure 1 and the examples in this data sheet are intended to illustrate ways to use these LSI parts and do not restrict the designer to any particular system configuration or application.

PIN ASSIGNMENTS

Pin Designation	Pin Number	Description
AD00	20	A Data Bus – Bit 0 I/O
AD01	22	A Data Bus – Bit 1 I/O
AD02	21	A Data Bus – Bit 2 I/O
AD03	13	A Data Bus – Bit 3 I/O
AD04	14	A Data Bus – Bit 4 I/O
AD05	15	A Data Bus – Bit 5 I/O
AD06	16	A Data Bus – Bit 6 I/O
AD07	19	A Data Bus – Bit 7 I/O
AD08	18	A Data Bus – Bit 8 I/O
BD00	4	B Data Bus – Bit 0 I/O
BD01	2	B Data Bus – Bit 1 I/O
BD02	3	B Data Bus – Bit 2 I/O
BD03	11	B Data Bus – Bit 3 I/O
BD04	10	B Data Bus – Bit 4 I/O
BD05	9	B Data Bus – Bit 5 I/O
BD06	8	B Data Bus – Bit 6 I/O
BD07	5	B Data Bus – Bit 7 I/O
BD08	6	B Data Bus – Bit 8 I/O
A00	29	A Address – Bit 0 Parity Bit Input
A01	30	A Address – Bit 1 LSB Input
A02	31	A Address – Bit 2 NLSB Input
A03	32	A Address – Bit 3 NLSB Input
A04	33	A Address – Bit 4 NMSB Input
A05	34	A Address – Bit 5 MSB Input
B00	41	B Address – Bit 0 Parity Input
B01	40	B Address – Bit 1 LSB Input
B02	39	B Address – Bit 2 NLSB Input
B03	38	B Address – Bit 3 NLSB Input
B04	37	B Address – Bit 4 NMSB Input
B05	35	B Address – Bit 5 MSB Input
$\overline{EnA}$	27	Enable A Register Latch to A Data Bus
$\overline{EnB}$	43	Enable B Register Latch to B Data Bus
$\overline{WEA}$	28	Write Enable A Data Bus to Memory
$\overline{WEB}$	42	Write Enable B Data Bus to Memory
$\overline{AError}$	23	A Address or Data Parity Error Output
$\overline{BError}$	47	B Address or Data Parity Error Output
$\overline{Clk\ A}$	26	Clock Enable A Register Latch Input
$\overline{Clk\ B}$	44	Clock Enable B Register Latch Input
$\overline{Clr}$	45	Clear A and B Error F/Fs and Register Latches
$\overline{AddEq}$	46	A and B Addresses are Equal and Error condition may exist
Clr Opt	48	Clear Option Input
V_{EE}	1	-5.2 Volt Supply
V_{EE}	24	-5.2 Volt Supply
V_{CC}	12	Ground
V_{CC}	36	Ground
V_{CCO}	7	Ground
V_{CCO}	17	Ground

FIGURE 2 – DETAILED MC10806 FUNCTION BLOCK DIAGRAM (NEGATIVE LOGIC)



NOTES: 1. If A00 is tied to V_{EE}, the A Address Parity Checker will be disabled.
If B00 is tied to V_{EE}, the B Address Parity Checker will be disabled.
2. Stack A and Stack B contain the same information; Data written into Stack A is automatically written into Stack B and vice versa.
3. If Pin 48 is left floating, the A and B Output Registers will be initialized to 0 1111 1111 when $\overline{Clear}$ = 0. If Pin 48 is tied to -2 V (V_{TT}), then the A and B Output Registers will be cleared to all 0s.

ARCHITECTURAL DESCRIPTION

The MC10806 Dual Access Stack as shown in Figure 2 contains a memory array of 32 words by 9 bits that can be read or written via two Address and two Data I/O ports. An output register, read/write control lines, an output enable, and a parity error output (via master/slave flip-flop) exists for each port. In addition, a Clear Input initializes the Parity Error flip-flops and Output Registers. Also, an Address Equal Output is available that indicates when the A and B Addresses are equal and the Write Enable of one port is active concurrently with either the Write Enable or the output latch register clock of the other port.

MEMORY ARRAY

The Memory Array actually contains two stacks with each containing 32 words by 9 bits. Each stack can be addressed independent of the other stack. When information is written into one stack, it is automatically written into the other stack at the same location. Thus, if Stack A is written via the A Bus into all address locations, Stack B will contain identical information. The advantage of this configuration is that the memory can be used as 32 9-bit registers in which reading and writing may be performed using two independent address and data ports.

One port could be writing into one stack location while the other port is reading from another stack location. Also, both ports could be reading or writing simultaneously at different stack locations. However, it is illegal to try to write into the same address from both ports simultaneously. As shown in Figure 2, the A Address Decoder and Write A Drivers are inhibited if the addresses are equal and the Write Enable is active ($\overline{WEB}$ = 0) on the B port. The reason for inhibiting the A Address Decoder is that the word line in the A Stack, corresponding to word line being enabled in the B Stack when writing, must be inhibited in order that the word can be duplicated in the A Stack.

OUTPUT REGISTER LATCH

An Output Register Latch exists for each data port which can be used as a temporary storage register which can be enabled onto the Data Bus at any time. Information in the memory can be read out at any time at the address specified by activating the Clock to the Latch Register ($\overline{Clk\ A\ or\ B}$ = 0). Information in the Register is latched when the Clock is deactivated ($\overline{Clk\ A\ or\ B}$ = 1).

ADDRESS CONTENTION

The $\overline{AddEq}$ output is activated whenever erroneous data is read out of memory or if an illegal write condition occurs. The illegal write condition occurs when writing into the same address from both ports simultaneously. Erroneous data can be read out of memory, if the addresses are equal when writing into one port and activating the clock of the Output Register of the other port. This is due to the inhibiting of the word line (as described earlier) which causes all 1s to be read into the latch. For these reasons the $\overline{AddEq}$ output goes to a "0", if the A and B addresses are equal and the Write Enable of one port is active concurrently with either the Write Enable or the Output Latch Register Clock of the other port.

PARITY CHECKING LOGIC

A master-slave flip-flop on each port is used to check address and data parity errors. The Error output goes to a 0 ($\overline{A\ Error}$ = 0 or $\overline{B\ Error}$ = 0), if there is a parity error when a 0 to 1 transition occurs on the clock (clock to A Error F/F = $\overline{WEA} \cdot \overline{ClkA}$ or the clock to B Error F/F = $\overline{WEB} \cdot \overline{ClkB}$). The Error output goes to a 1, if there is no parity error when a 0 to 1 transition occurs on the clock.

If an address parity error occurs, the contents of the selected address cannot be changed, when writing, in order to facilitate error recovery. The Address Parity Checker can be disabled by connecting the Address Parity Input (A00, B00) to the V_{EE} supply. The data that is read or written into memory is checked for even parity (an even number of 1s must exist in the 9-bit word), if negative logic is used, or odd parity, if positive logic is used. If the parity checking is not required, then a word in memory can consist of 9 bits of data with the Parity Error output ignored.

CLOCK

The clock to the A Error F/F (B Error F/F) is the AND function of the $\overline{WEA}$ ($\overline{WEB}$) and $\overline{ClkA}$ ($\overline{ClkB}$) inputs. The Error F/Fs are master-slave and trigger on a 0 to 1 transition (V_{OH} to V_{OL}) of the clock as defined above.

The A output Register (B Output Register) consists of latches with the $\overline{ClkA}$ ($\overline{ClkB}$) input controlling the clocking. When $\overline{ClkA}$ = 0 ($\overline{ClkB}$ = 0), the data addressed from memory is enabled to the output of the register. When $\overline{ClkA}$ = 1 ($\overline{ClkB}$ = 1), the data in the register is in the latched condition and cannot change.

$\overline{CLEAR}$

The $\overline{Clear}$ input, when a 0, is used to asynchronously reset the error flip-flops and the output registers. This causes the $\overline{A\ Error}$ and $\overline{B\ Error}$ outputs to go to a 1. The output registers are cleared to all 0s if pin 48 is tied to -2 V. If pin 48 is left open, the output register is cleared to 0 1111 1111 (the 0 corresponds to the BIT 00 position in the word).

FUNCTIONAL DESCRIPTION

The MC10806 Dual Access Stack (DAS) can be completely described by the truth tables shown in Tables 1 through 8, together with the block diagram (Figure 2) and the switching waveforms shown in the Electrical Parameters. **All truth tables are expressed in negative logic with V_{OL} being a logic 1 and V_{OH} a logic 0.**

NO OPERATION

Writing into the memory of the DAS is inhibited, if the write enable is not active ($\overline{WEA}$ = 1, $\overline{WEB}$ = 1). Reading from the memory to the output register is inhibited (contents of output register remains unchanged), if the clock is not active ($\overline{ClkA}$ = 1, $\overline{Clk\ B}$ = 1). Also, reading the contents of the Output Register to the Data Bus is inhibited, if the enable line is not active ($\overline{EnA}$ = 1, $\overline{EnB}$ = 1). However, even if no operation is being performed internally the Read Amplifiers will read the data from memory as addressed by the address lines (A01 – A05, B01 – B05).

READ OPERATION

There are three modes in which data can be read onto the data bus as shown in the switching waveforms. In the enable access mode (see Table 7), the activation of the enable line ($\overline{EnA}$ = 0, $\overline{EnB}$ = 0) transfers the contents of the 9-bit Output Register onto the bidirectional data bus. Normally, the contents of the Output Register have been previously loaded from memory making the enable access time very fast.

In the address access mode, the Address lines select the memory location to be accessed and the data appears at the Data Bus after the specified propagation delay has occurred. This assumes that the clock ($\overline{ClkA}$ = 0, $\overline{ClkB}$ = 0) and Enable ($\overline{EnA}$ = 0, $\overline{EnB}$ = 0) lines are both active.

In the third mode for reading data, the activation of the clock (with the addressed location having been set up previously) causes data to appear at the Data Bus (if $\overline{EnA}$ = 0, $\overline{EnB}$ = 0) after the specified propagation delay. Deactivating the clock (0 to 1 transition of $\overline{ClkA}$, $\overline{ClkB}$) causes the data to be latched in the Output Register (see Tables 5 and 6) and the Parity Error flip-flop to be activated ($\overline{A\ Error}$ = 0, $\overline{B\ Error}$ = 0), if there is an address or data parity error (see Tables 2, 3, and 4). When latching the data in the output register by deactivating the clock, the address lines must meet the setup and hold times that are specified.

WRITE OPERATION

The switching waveforms should be referred to in the following description of the write mode of operation. The Enable line, for reading data onto the data bus, must be deactivated ($\overline{EnA}$ = 1, $\overline{EnB}$ = 1) when writing data coming from external sources. However, the Enable line could be activated, if the source for writing data is the internal Output Register. The address should be set up prior to activating the Write Enable line in order that the parity of the address can be checked for error so that writing can be inhibited, if an error occurs (see Table 1). Information on the Data Bus is written into the memory location when the Write Enable is activated ($\overline{WEA}$ = 0, $\overline{WEB}$ = 0). The information must be valid during the setup and hold times referenced to the deactivation of the Write Enable (0 to 1 transition of $\overline{WEA}$, $\overline{WEB}$). Also, the deactivation of the Write Enable causes the Parity Error flip-flop to be activated, if there is an Address or Data Parity Error (see Tables 2, 3, and 4). Note that it is possible to read the data that is being written, into the Output Register by activating the Clock Enable of the same port being written.

PARITY CHECKING

The truth tables for the Parity Error flip-flops are shown in Tables 2, 3, and 4. A description of the parity checking logic is described in the Architectural Description. The Error flip-flops are in the activated state when a logic 0 so that they could be tied together forming the wired-AND function.

INITIALIZATION

Initializing the Error flip-flops and the Output Registers can be accomplished asynchronously by momentarily placing the Clear at a logic 0. Initialization of the Error flip-flops is included in Tables 3 and 4, while Tables 5 and 6 show the initialization states of the Output Registers.

CONFLICTS

An illegal write condition occurs for the dual write condition where both ports are writing into the same address simultaneously. It is the user's responsibility to ensure that writing into both ports simultaneously at the same address does not occur. A write on port A (when Address A = B) inhibits a selection of port B, and a write on port B inhibits a selection on port A. Thus, in a dual write case, theoretically neither writes as shown in Table 1. However, the practical case considers that one port's control signal will occur slightly before the other; thus, the contents of the equal location cannot be guaranteed.

Another possible conflict can occur when writing into one port and activating the Clock of the Output Register of the other port. The internal logic forces all 1s into the Output Register as shown in Table 1. However, if the Clock is held activated a sufficient amount of time after the Write Enable pulse, the contents of the Output

Register will be corrected to the information that was written into memory and a parity error will not occur due to the conflict. A parity error would occur, if the Clock is deactivated while all 1s were being forced into the Output Register, since all 1s is an odd parity condition.

The $\overline{\text{AddEq}}$ output is activated ($\overline{\text{AddEq}}$ = 0) whenever the two possible conflict conditions exist. A truth table is shown in Table 8 listing the various conflict conditions.

TABLE 1 – TRUTH TABLE FOR MEMORY ARRAY AND READ AMPLIFIER OUTPUTS

$\overline{\text{WEA}}$	(See Table 2a) A Address Parity Error	$\overline{\text{WEB}}$	(See Table 2b) B Address Parity Error	Address Equal Condition A01-05=B01-05	Memory Array Contents @ Address A	Memory Array Contents @ Address B	Read A Amp Output	Read B Amp Output	Comments
1	X	1	X	X	–	–	MA00-MA08	MB00-MB08	Read A; Read B
0	0	1	X	0	AD00-AD08	–	AD00-AD08	MB00-MB08	Write A; Read B
0	0	1	X	1	AD00-AD08	AD00-AD08	AD00-AD08	All 1s	Write A; Read B Amp = All 1s
0	1	1	X	X	–	–	MA00-MA08	MB00-MB08	Parity Error, No Write A; Read B
1	X	0	0	0	–	BD00-BD08	MA00-MA08	BD00-BD08	Read A; Write B
1	X	0	0	1	BD00-BD08	BD00-BD08	All 1s	BD00-BD08	Read A Amp = All 1s; Write B
1	X	0	1	X	–	–	MA00-MA08	MB00-MB08	Read A; Parity Error, No Write B
0	0	0	0	0	AD00-AD08	BD00-BD08	AD00-AD08	BD00-BD08	Write A; Write B
0	1	0	0	0	–	BD00-BD08	MA00-MA08	BD00-MB08	Parity Error, No Write A; Write B
0	0	0	1	0	AD00-AD08	–	AD00-AD08	MB00-MB08	Write A; Parity Error, No Write B
0	1	0	1	X	–	–	MA00-MA08	MB00-MB08	Parity Error, No Write A; Parity Error, No Write B
0	0	0	0	1	–	–	All 1s	All 1s	Writing is Inhibited
0	1	0	0	1	BD00-BD08	BD00-BD08	All 1s	BD00-BD08	Parity Error, No Write A; Write B
0	0	0	1	1	AD00-AD08	AD00-AD08	AD00-AD08	All 1s	Write A; Parity Error, No Write B

X = Don't Care State – = No Change

NOTE: MA00-MA08 represents the data in the Memory Array at the location addressed by A01-A05. MB00-MB08 represents the data in the Memory Array at the location addressed by B01-B05.

TABLE 2 – TRUTH TABLE FOR ADDRESS PARITY ERROR

a. A Address Parity Error

Parity Bit A00	A Address A01-A05	A Address Parity Error
V_{EE}	X	0
0	Odd Number of 1s	0
1	Odd Number of 1s	1
0	Even Number of 1s	1
1	Even Number of 1s	0

b. B Address Parity Error

Parity Bit B00	B Address B01-B05	B Address Parity Error
V_{EE}	X	0
0	Odd Number of 1s	0
1	Odd Number of 1s	1
0	Even Number of 1s	1
1	Even Number of 1s	0

X = Don't Care Condition

TABLE 3 – TRUTH TABLE FOR $\overline{\text{A ERROR}}$ (OUTPUT OF MASTER/SLAVE FF)

$\overline{\text{Clear}}$	$\overline{\text{Clk A}}$	$\overline{\text{WEA}}$	A Address Parity Error (See Table 2a)	Read A Amp Output (See Table 1)	$\overline{\text{A Error}}$
0	X	X	X	X	1
1	0	X	X	X	–
1	X	0	X	X	–
1	1 or 1 → 0	1 or 1 → 0	X	X	–
1	0 → 1	1	0	Even Number of 1s	1
1	0 → 1	1	1	X	0
1	0 → 1	1	X	Odd Number of 1s	0
1	1	0 → 1	0	Even Number of 1s	1
1	1	0 → 1	1	X	0
1	1	0 → 1	X	Odd Number of 1s	0

X = Don't Care State – = No Change

NOTES: 1. 0 → 1 denotes a transition from logic 0 to logic 1 (negative logic).
2. The $\overline{\text{A Error}}$ output changes state on a 0 to 1 transition of $\overline{\text{Clk A}}$ or $\overline{\text{WEA}}$ input.

TABLE 4 – TRUTH TABLE FOR $\overline{\text{B ERROR}}$ (OUTPUT OF MASTER/SLAVE FF)

$\overline{\text{Clear}}$	$\overline{\text{Clk B}}$	$\overline{\text{WEB}}$	B Address Parity Error (See Table 2b)	Read B Amp Output (See Table 1)	$\overline{\text{B Error}}$
0	X	X	X	X	1
1	0	X	X	X	–
1	X	0	X	X	–
1	1 or 1 → 0	1 or 1 → 0	X	X	–
1	0 → 1	1	0	Even Number of 1s	1
1	0 → 1	1	1	X	0
1	0 → 1	1	X	Odd Number of 1s	0
1	1	0 → 1	0	Even Number of 1s	1
1	1	0 → 1	1	X	0
1	1	0 → 1	X	Odd Number of 1s	0

X = Don't Care State – = No Change

NOTES: 1. 0 → 1 denotes a transition from logic 0 to logic 1 (negative logic).
2. The $\overline{\text{B Error}}$ output changes state on a 0 to 1 transition of $\overline{\text{Clk B}}$ or $\overline{\text{WEB}}$ input.

TABLE 5 – TRUTH TABLE FOR A OUTPUT REGISTER LATCH (AL)

Clr Opt ①	$\overline{\text{Clear}}$	$\overline{\text{Clk A}}$	A Output Register Latch (AL)								
			AL00	AL01	AL02	AL03	AL04	AL05	AL06	AL07	AL08
Open	0	X	0	1	1	1	1	1	1	1	1
-2 V	0	X	0	0	0	0	0	0	0	0	0
X	1	1 ②	--	–	–	–	–	–	–	–	–
X	1	0 ③	Read A Amp Output (See Table 1)								

X = Don't Care State – = No Change

NOTES: ① The Clr Opt, Pin 48, may be left "Open" or connected to -2 Volts.
② Information is "latched" when $\overline{\text{Clk A}}$ = 1.
③ The Read A Amp Outputs are enabled to the output of the A Register Latch when $\overline{\text{Clk A}}$ = 0.

TABLE 6 – TRUTH TABLE FOR B OUTPUT REGISTER LATCH (BL)

Clr Opt ①	$\overline{\text{Clear}}$	$\overline{\text{Clk B}}$	B Output Register Latch (BL)								
			BL00	BL01	BL02	BL03	BL04	BL05	BL06	BL07	BL08
Open	0	X	0	1	1	1	1	1	1	1	1
-2 V	0	X	0	0	0	0	0	0	0	0	0
X	1	1 ②	–	–	–	–	–	–	–	–	–
X	1	0 ③	Read B Amp Output (See Table 1)								

X = Don't Care State – = No Change

NOTES: ① The Clr Opt, Pin 48, may be left "Open" or connected to -2 Volts.

② Information is "latched" when $\overline{\text{Clk B}}$ = 1.

③ The Read B Amp Outputs are enabled to the output of the B Register Latch when $\overline{\text{Clk B}}$ = 0.

TABLE 7 – TRUTH TABLES FOR A AND B DATA BUS OUTPUTS

a. A Data Bus Output

$\overline{\text{EnA}}$	A Data Bus AD00-AD08
1	Logic 1s (Disabled)
0	AL00-AL08 (Enabled)

b. B Data Bus Output

$\overline{\text{EnB}}$	B Data Bus BD00-BD08
1	Logic 1s (Disabled)
0	BL00-BL08 (Enabled)

TABLE 8 – TRUTH TABLE FOR $\overline{\text{AddEq}}$ OUTPUT

$\overline{\text{WEA}}$	$\overline{\text{WEB}}$	$\overline{\text{Clk A}}$	$\overline{\text{Clk B}}$	Address Equal A01-05=B01-05	$\overline{\text{AddEq}}$
X	X	X	X	0	1
1	1	X	X	X	1
1	0	1	X	1	1
X	0	0	X	1	0
0	1	X	1	1	1
0	X	X	0	1	0
0	0	X	X	1	0

X = Don't Care State

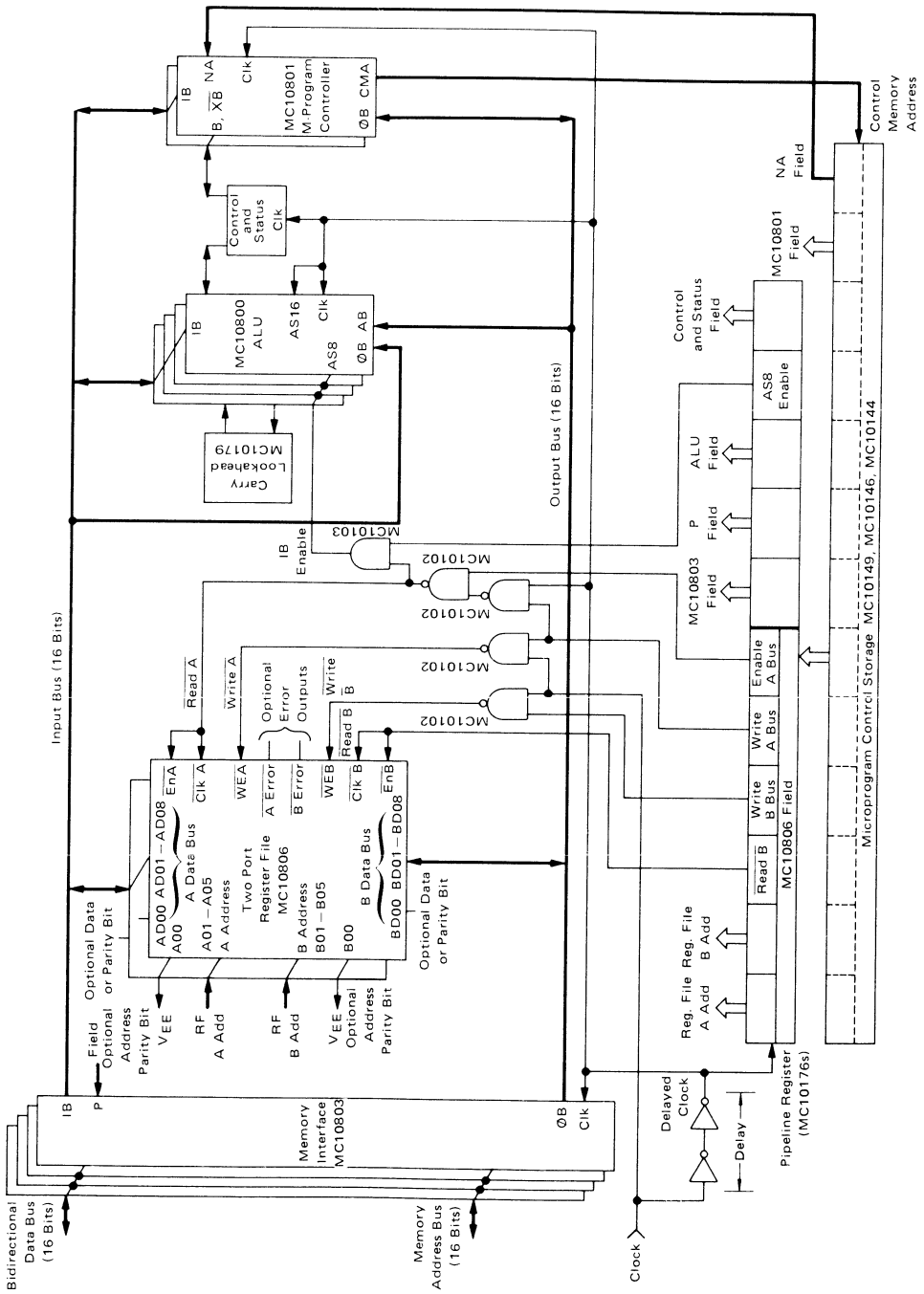
APPLICATION INFORMATION

Figure 3 shows two MC10806s interconnected to form a 32 word by 16-bit Register File in a typical 16-bit pipelined configuration. The Register File is designed so that two words can be read and operated within the ALU with the result being written back into the Register File (A plus B → A) all in the same cycle as shown in the timing diagram in Figure 4. The Clock is delayed about 5 ns in order to satisfy the hold time of data on the Input Bus with respect to the deactivation of the $\overline{\text{Write A}}$ signal. The delay could be made using a delay line or gate delay. The gating of the Clock for reading and writing into the Register File is shown in Figure 3 as well as the interconnections required on the MC10800s for latching the data (AS16) and controlling the enable (AS8) for data to the IB port.

For the A plus B → A operation, the following describes the cycle. First, the microprogram information for the A plus B → A operation is clocked into the Pipelined Register when the Clock goes from a 1 to a 0. After the delay of the register the two address locations A and B are accessed via the Register File with the data appearing on the Input and Output Bus. Then the ALU performs the A plus B operation via the ØB and AB ports of the MC10800. When the Clock goes to a 1, the information on the ØB port is latched in the MC10800; the result of the A plus B operation is enabled to the Input Bus; and, the $\overline{\text{ReadA}}$ line is deactivated (goes to a 1). On the 1 to 0 transition of the Clock, the data is stored in the Register File and a new operation is available at the output of the pipeline register.

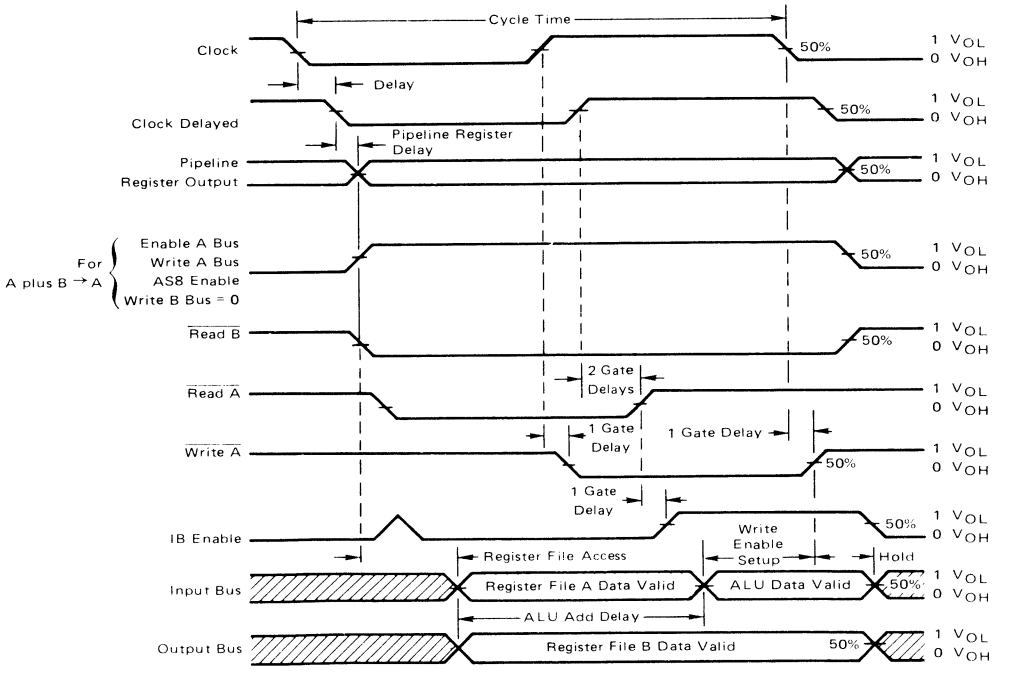
The Register File is also capable of writing into two locations in the same timing cycle. If a third Register File (C Address) was made available from microprogram memory, the operation A plus B → C could be performed in one cycle. This is accomplished by selecting the C Address onto the A Address inputs of the MC10806 when

FIGURE 3 – MC10806 REGISTER FILE APPLICATION USED IN A TYPICAL M10800 SYSTEM



the Clock goes from a 0 to a 1. The $\overline{\text{WriteA}}$ pulse would need to be narrowed using a 4 phase clock system in order to meet the address 4 phase clock system in order to meet the address setup time of the MC10806. In other words, the $\overline{\text{WriteA}}$ should not be activated until the C address is stable, meeting the address setup time of the MC10806. The cycle time for the system shown in Figure 3 is typically 85 ns. Worst case numbers can be calculated from the data sheets of parts used in the system along with the timing diagram information. The architecture of the system can be changed depending on system requirements. Versatility is of prime concern to the system designers and this flexibility is built into the M10800 family.

FIGURE 4 – TIMING DIAGRAM FOR MC10806 REGISTER FILE APPLICATION (FIG. 3)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage (V_{CC} = 0 Volts)	V_{EE}	−4.68 to −5.72	Vdc
Operating Temp. (Functional)	T_A	−30 to +85	°C
Output Drive	–	50Ω to −2.0 Vdc	–
Maximum Clock Input Rise and Fall Time (20% to 80%)	t_r, t_f	10	ns

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_{EE}	1, 24	–	–	–	330	413	–	–	mAdc	–	–	–	–	1, 24	7, 12, 17, 36
Input Current	I_{inH}	2	–	–	–	–	50	–	–	µAdc	2	27	–	–	1, 24	7, 12, 17, 36
		29	–	–	–	–	210	–	–		29	–	–	–		
		30	–	–	–	–	370	–	–		30	–	–	–		
		27	–	–	–	–	435	–	–		27	–	–	–		
	I_{inL}	29	–	–	0.5	–	–	–	–		–	29	–	–		
Logic "0" Output Voltage	V_{OH}	22	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	45, 27	26*	–	–	1, 24	7, 12, 17, 36
		46	−1.060	−0.890	−0.960	–	−0.810	−0.890	−0.700	Vdc	28, 42	**	–	–	1, 24	7, 12, 17, 36
Logic "1" Output Voltage	V_{OL}	22	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	45, 27	26	–	–	1, 24	7, 12, 17, 36
		46	−1.890	−1.675	−1.850	–	−1.650	−1.825	−1.615	Vdc	–	26, 28, 42, 44	–	–	1, 24	7, 12, 17, 36
	V_{OLB}	22	–	−1.980	–	–	−1.980	–	−1.980	Vdc	–	27	–	–	1, 24	7, 12, 17, 36
Logic "0" Threshold Voltage	V_{OHA}	22	−1.080	–	−0.980	–	–	−0.910	–	Vdc	45	26*	27	–	1, 24	7, 12, 17, 36
		46	−1.080	–	−0.980	–	–	−0.910	–	Vdc	–	27	–	–	1, 24	7, 12, 17, 36
Logic "1" Threshold Voltage	V_{OLA}	22	–	−1.655	–	–	−1.630	–	−1.595	Vdc	45	26	27	–	1, 24	7, 12, 17, 36
		46	–	−1.655	–	–	−1.630	–	−1.595	Vdc	–	28, 42, 44	–	26	1,24	7, 12, 17, 36
	V_{OLB}	22	–	−1.980	–	–	−1.980	–	−1.980	Vdc	–	–	–	27	1, 24	7, 12, 17, 36

*Pin 48 = −2.0 V

**V_{IH} on Pins 30, 31, 32, 33, 34, 35, 37, 38, 39, 40

SETUP AND HOLD TIME (NANOSECONDS AT 25°C)

Input	Input Reference	$\overline{\text{Clk A}}$ or $\overline{\text{Clk B}}$ (0 → 1)				WEA or WEB (0 → 1)			
		Set Up		Hold		Set Up		Hold	
		Min	Typ	Min	Typ	Min	Typ	Min	Typ
Address A, B	A00-A05 B00-B05	—	12	—	0	—	10*	—	0
Data Bus A, B,	AD00-AD08 BD00-BD08	—	—	—	—	—	14	—	0

* Address setup time is referenced to the 1 → 0 transition of $\overline{\text{WEA}}$ or $\overline{\text{WEB}}$.

IPD, PROPAGATION DELAY TIME (NANOSECONDS AT 25°C)

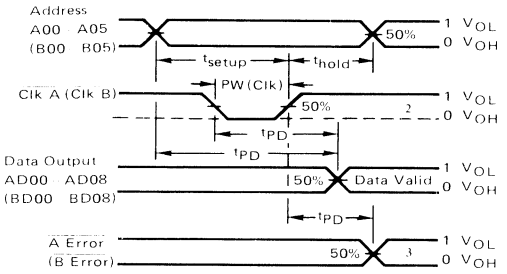
Input	Output	A Data Bus AD00-AD08 B Data Bus BD00-BD08		$\overline{\text{A Error}}$ $\overline{\text{B Error}}$		$\overline{\text{AddEq}}$	
		Typ	Max	Typ	Max	Typ	Max
Address A, B	A01-A05 B01-A05	19	—	—	—	—	—
$\overline{\text{EnA}}$, $\overline{\text{EnB}}$		6	—	—	—	—	—
$\overline{\text{Clk A}}$, $\overline{\text{Clk B}}$		7	—	5.5	—	7.5	—
$\overline{\text{WEA}}$, $\overline{\text{WEB}}$		—	—	—	—	8	—
$\overline{\text{Clear}}$		12	—	—	—	—	—

PULSE WIDTH TIME (NANOSECONDS AT 25°C)

Input	Min	Typ	
$\overline{\text{Clk A}}$, $\overline{\text{Clk B}}$	—	4.5	
$\overline{\text{WEA}}$, $\overline{\text{WEB}}$	—	12	Address A01-A05 ≠ B01-B05
	—	18	Addresses Equal A01-A05 = B01-B05
$\overline{\text{Clear}}$	—	4.5	

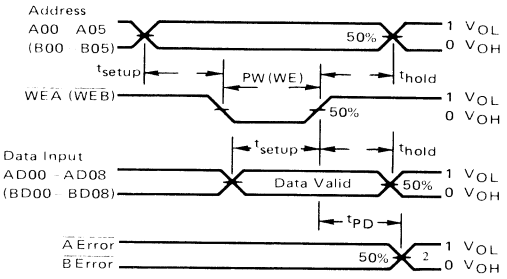
SWITCHING WAVEFORMS

Read Mode — Address Access[1]
(Port A or B or Both)



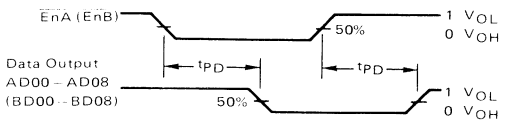
NOTES: 1. $\overline{EnA}$ ($\overline{EnB}$) is maintained at a Logic 0.
2. $\overline{ClkA}$ ($\overline{ClkB}$) can be maintained at a Logic 0 in the Read Mode.
3. $\overline{A\,Error}$ ($\overline{B\,Error}$) goes to a 0, if there is a Parity Error.

Write Mode[1]
(Port A or B or Both)



NOTES: 1. $\overline{EnA}$ ($\overline{EnB}$) is maintained at a Logic 1.
2. $\overline{A\,Error}$ ($\overline{B\,Error}$) goes to a 0, if there is a Parity Error.

Read Mode — Enable Access
(Port A or B or Both)



TEST PROCEDURE FOR SETUP AND HOLD

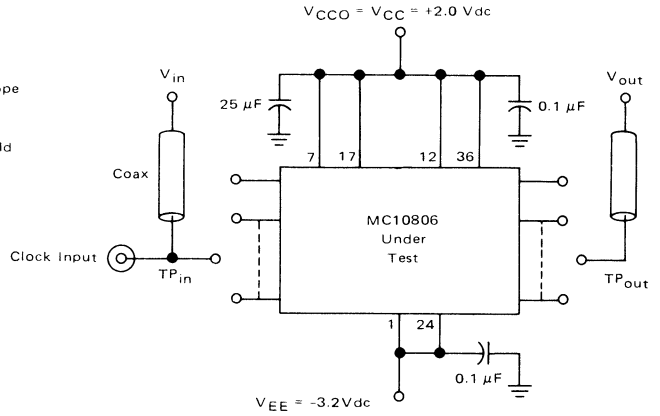
a. Establish setup time with long t_{hold}.
b. Keeping the leading edge of the input constant (t_{setup}) vary the trailing edge of the input to determine t_{hold}.

NOTE: t_{setup} and t_{hold} as defined are positive. Internal delays in the data path may result in a shift of the data waveform to the left, with respect to the clock, resulting in negative hold times.

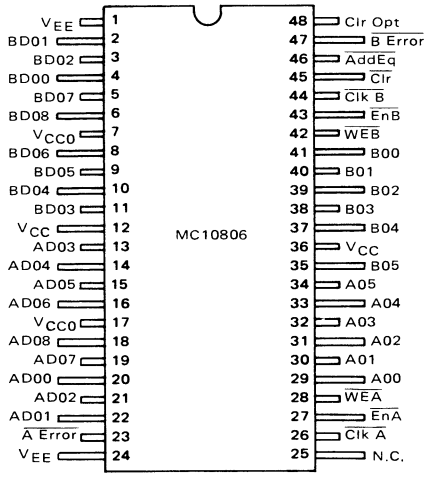
SWITCHING TIME TEST CIRCUIT

50 ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be $<\frac{1}{4}$ inch from TP_{in} to input pin and TP_{out} to output pin.

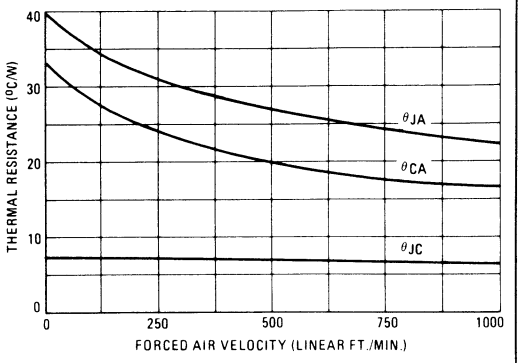


PIN ASSIGNMENT

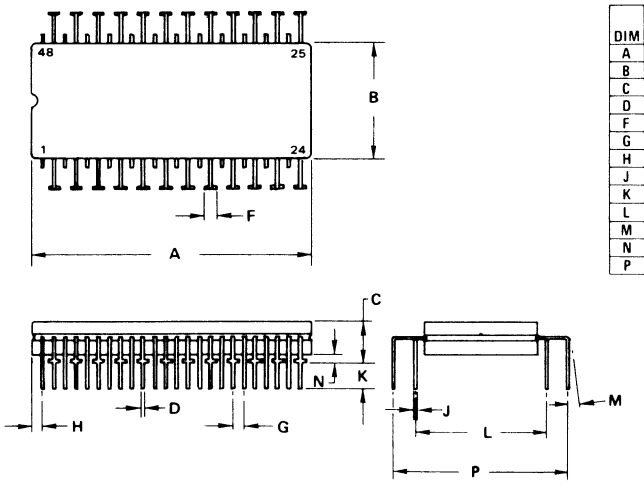


N.C. = No Connection

THERMAL CHARACTERISTICS (TYPICAL)



PACKAGE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.57	5.59	0.180	0.220
D	0.38	0.53	0.015	0.021
F	1.14	1.40	0.045	0.055
G	1.27 BSC		0.050 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.54	3.30	0.100	0.130
L	15.24 BSC		0.600 BSC	
M	–	7°	–	7°
N	0.51	1.52	0.020	0.060
P	20.32 BSC		0.800 BSC	

Case 725-01

A socket for the QUIL package is available from ELECTRONIC MOLDING CORPORATION. (Part number 7178-295-5)

QUIL is a trademark of Motorola Inc.

MOTOROLA Semiconductors

MC10807

Advanced Information

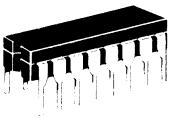
MECL
5-BIT BIDIRECTIONAL
BUS TRANSCEIVER

INTRODUCTION

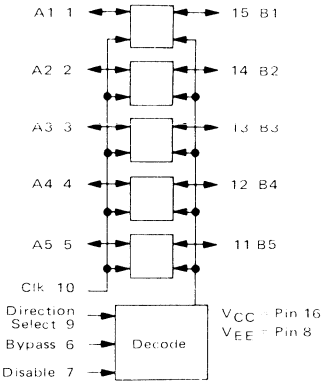
The MC10807 is a 5-bit bidirectional MECL bus transceiver. Data can be transferred directly in either direction (A port → B port or B port → A port), and an optional gated latch is also provided. Operation is shown in the truth table.

The MC10807 is in a 16-pin ceramic package and is a member of the high performance M10800 MECL/LSI processor family. It is designed to provide bidirectional exchange of MECL level signals in multiprocessor installations, and multiplexing of buses to a single processor.

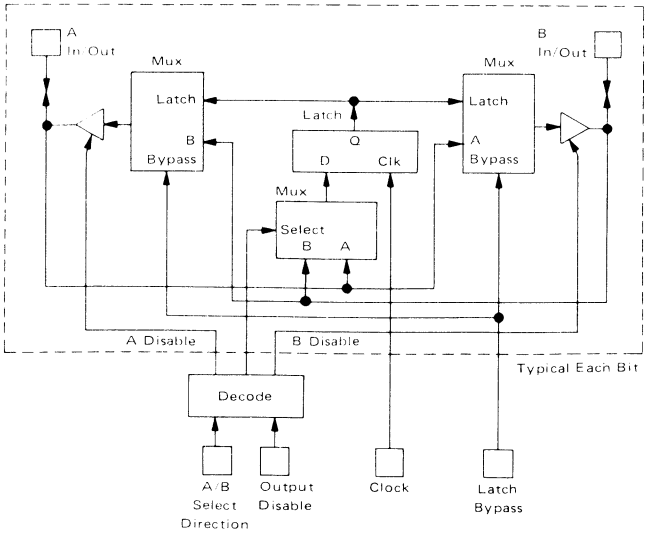
- Bidirectional Data Transfer
- Standard MECL 50 Ohm Drive Outputs
- Latch – Can Be Bypassed for High Speed



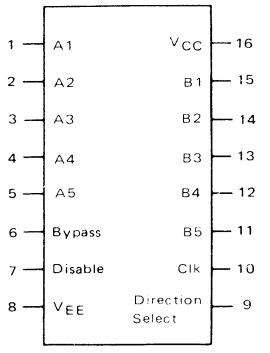
L SUFFIX
CERAMIC PACKAGE
CASE 620



BLOCK DIAGRAM



PIN ASSIGNMENTS



This is advance information on a new introduction and specifications are subject to change without notice.

ADI 509

FUNCTIONAL DESCRIPTION

The MC10807 consists of a function decode section, a clock buffer, and five identical bit channels. Each bit consists of a bidirectional A port, a bidirectional B port, and a latch.

Three logic pins control the function selection. These pins, along with the clock, all operate at standard MECL levels. The block diagram and truth table define the functions. The individual pin descriptions are as follows:

Output Disable

The Output Disable, when at V_{IL}, disables both the A and B port output buffers. That is, both are forced to high-impedance states. When the Output Disable is at V_{IH} the data translation takes place normally, and the appropriate output ports enabled by the direction select are active. Regardless of the state of the Output Disable pin, clocked data can be loaded into the latch from the selected input port.

A/B Direction Select

The A/B Direction Select pin controls the direction of data transfers. When at V_{IL}, the B-to-A direction is selected. In this case, the B output drivers are disabled, data is input to the latch from the B port, and data is output onto the A port. When the select pin is at V_{IH}, the A-to-B direction is selected and the function is the reverse.

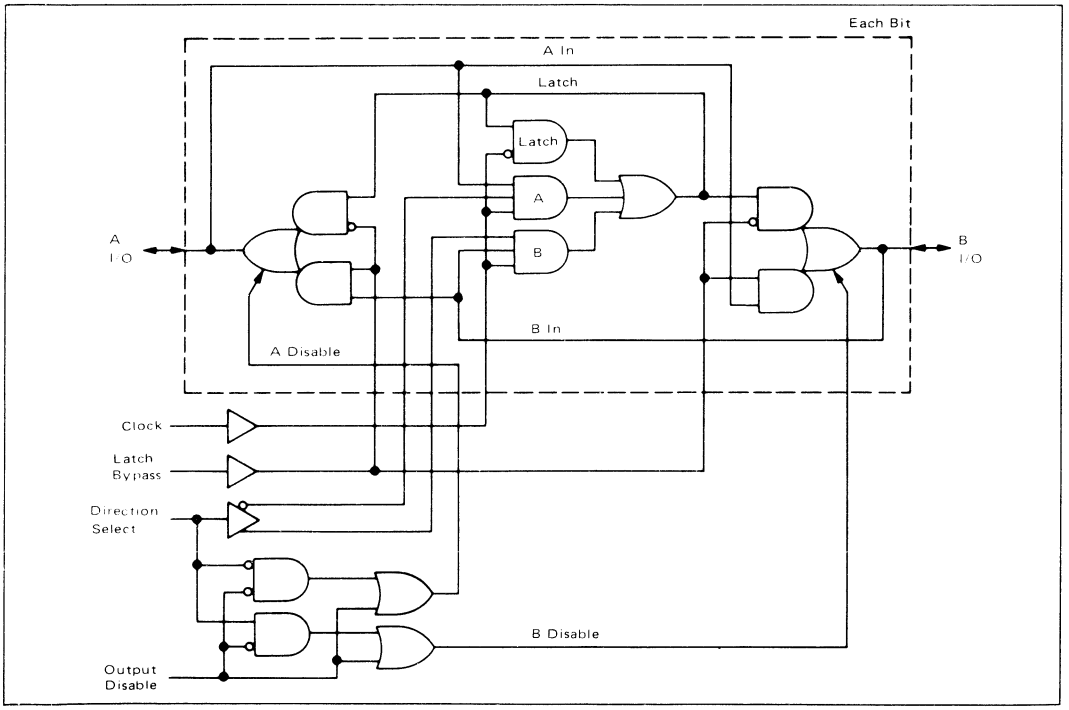
Latch Bypass

The Latch Bypass select line bypasses the latch circuitry for the fast data transfer. When the select line is at V_{IL}, the data is directed to both the latch input and the output buffer simultaneously. This feature enhances the speed of translation because the delay through the latch is bypassed. When the Latch Bypass pin is at V_{IH}, the data must first go into the latch then be sent to the output ports.

Clock

The Clock input is common to all latches and controls the storage of data. When the Clock is at V_{IL} the latch is open and data ripples through from the D input to the Q output. Data is stored or latched on the V_{IL}-to-V_{IH} transition of the Clock input.

NEGATIVE LOGIC DIAGRAM



TRUTH TABLE

SELECT INPUTS (ECL LEVELS, H = -.9V, L = -1.7V)				FUNCTION		
Disable	Direction Select	Bypass	Clock (2)	Latch (1)	B I/O**	A I/O**
H	H	H	H	* Q = H * Q = L	Output = Q = H = L	Off Off
H	H	H	L	Q = A Input = H = L	Output = Q = H = L	Input = H = L
H	H	L	H	* *	Output = A = H = L	Input = H = L
H	H	L	L	Q = A Input = H = L	Output = A = H = L	Input = H = L
H	L	H	H	* Q = H * Q = L	Off Off	Output = Q = H = L
H	L	H	L	Q = B Input = H = L	Input = H = L	Output = Q = H = L
H	L	L	H	* *	Input = H = L	Output = B = H = L
H	L	L	L	Q = B Input = H = L	Input = H = L	Output = B = H = L
L	H	H	H	*	Off	Off
L	H	H	L	Q = A Input = H = L	Off Off	Input = H = L
L	H	L	H	*	Off	Off
L	H	L	L	Q = A Input = H = L	Off Off	Input = H = L
L	L	H	H	*	Off	Off
L	L	H	L	Q = B Input = H = L	Input = H = L	Off
L	L	L	H	*	Off	Off
L	L	L	L	Q = B Input = H = L	Input = H = L	Off

NOTES: (1) * Denotes "NO CHANGE" (2) Latch transfers data when clock is "L" and stores data when clock is "H"
(3) **Output driver is disabled to V_{OLZ} during "Off" state.

SETUP AND HOLD TIMES (NANOSECONDS AT 25°C)

Input	Setup		Hold	
	Min	Typ	Min	Typ
A1-5, B1-5	–	2.0	–	4.0
Direction Select	–	4.5	–	1.5

PROPAGATION DELAY TIMES (NANOSECONDS AT 25°C)

Path	Mode	Typical	Max
A1-5 → B1-5	Latch Bypassed	3.9	–
B1-5 → A1-5	Latch Bypassed	3.9	–
A1-5 → B1-5	Via Latch	6.4	–
B1-5 → A1-5	Via Latch	6.4	–
Bypass → Output		6.4	–
Disable → Output		4.9	–
Direction Select → Output	Direct	7.4	–
Direction Select → Output	Via Latch	8.9	–
Clock → Output		7.0	–

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage (V_{CC} = 0 Volts)	V_{EE}	−4.68 to −5.72	Vdc
Operating Temperature (Functional)	T_A	−30 to +85	°C
Output Drive	—	50 Ω to −2.0 Vdc	—
Maximum Clock Input Rise and Fall Time (20% to 80%)	t_r, t_f	10	ns
Minimum Clock Pulse Width	PW	5	ns

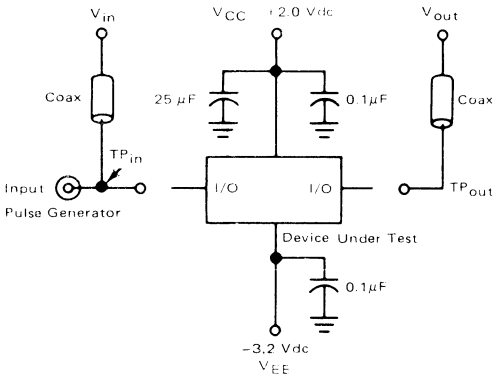
ELECTRICAL CHARACTERISTICS

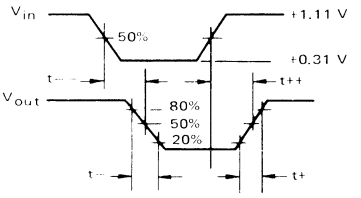
Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
−30°C	−0.0890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

Characteristic	Symbol	Pin Under Test	MC10807 TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_{EE}	8	—	—	—	87	—	—	—	mAdc	—	—	—	—	8	16
Input Current	I_{inH}	6	—	—	—	—	350	—	—	μAdc	6	—	—	—	8	16
		1	—	—	—	—	410	—	—		1	—	—	—	8	16
	I_{inL}	6	—	—	0.5	—	—	—	—	μAdc	—	6	—	—	8	16
Logic "0" Output Voltage	V_{OH}	1	−1.060	−0.890	−0.960	—	−0.810	−0.890	−0.700	Vdc	7, 10, 15	6, 9	—	—	8	16
Logic "1" Output Voltage	V_{OL}	1	−1.890	−1.675	−1.850	—	−1.650	−1.825	−1.615	Vdc	7, 10	6, 9, 15	—	—	8	16
Logic "0" Threshold Voltage	V_{OHA}	1	−1.080	—	0.980	—	—	−0.910	—	Vdc	7, 10	6, 9	15	—	8	16
Logic "1" Threshold Voltage	V_{OLA}	1	—	−1.655	—	—	−1.630	—	−1.595	Vdc	7, 10	6, 9	—	15	8	16
Output Cutoff Voltage	V_{OLZ}	1	—	−1.980	—	—	−1.980	—	−1.980	Vdc	—	7	—	—	8	16

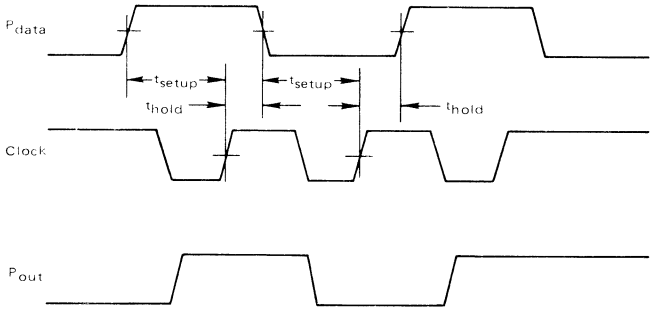
SWITCHING TIME TEST CIRCUIT AND WAVEFORMS @ 25°C
FOR PROPAGATION DELAY



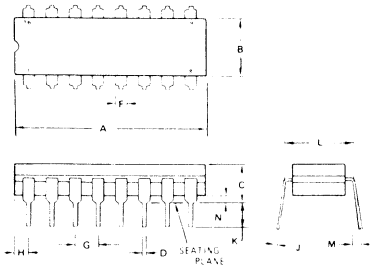


50-ohm termination to ground located in each scope channel input.
All input and output cables to the scope are equal lengths of 50 ohm coaxial cable.
Wire length should be ≤ 1/4 inch from TP_{in} to input pin and TP_{out} to output pin.

SETUP AND HOLD TIME WAVEFORMS



PACKAGE DIMENSIONS



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2. PKG INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.31	0.008	0.012
K	3.18	0.30	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

CASE 620-02

MOTOROLA Semiconductors

MC10808

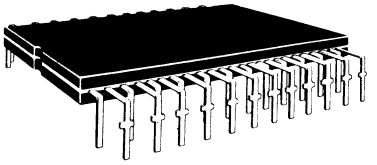
Advance Information

INTRODUCTION

The MC10808 Programmable Multi-Bit Shifter is an LSI building block for shifting data in a high-speed processor system. The circuit is essential when performing floating point operations for pre-normalization or alignment of exponents.

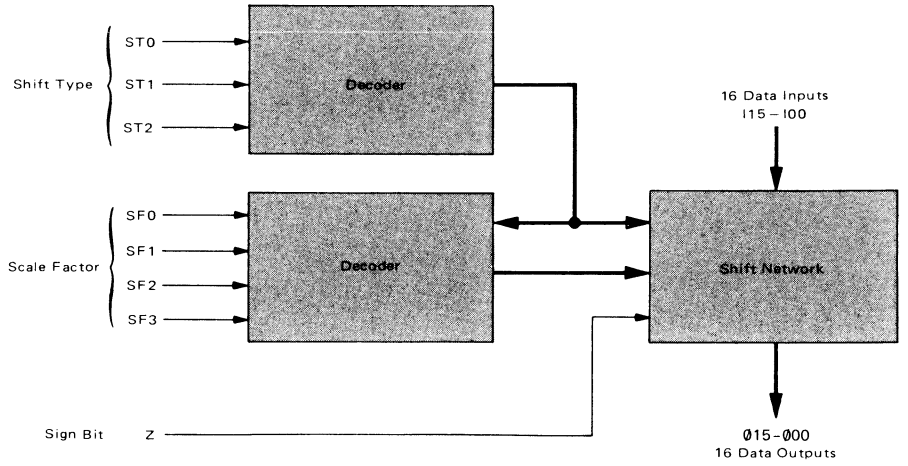
The Programmable Multi-Bit Shifter as shown in the block diagram contains a 16-bit shift network that is fully expandable in a shifter array to handle practically any number of bits. The shift type function select contains arithmetic, logic, and rotate shifting. Four scale factor inputs are provided for specifying the number of positions that the input data is to be shifted or rotated. A sign bit is also provided for arithmetic shift operations.

MECL — LSI PROGRAMMABLE 16-BIT SHIFTER FUNCTION



CASE 725-01

BLOCK DIAGRAM



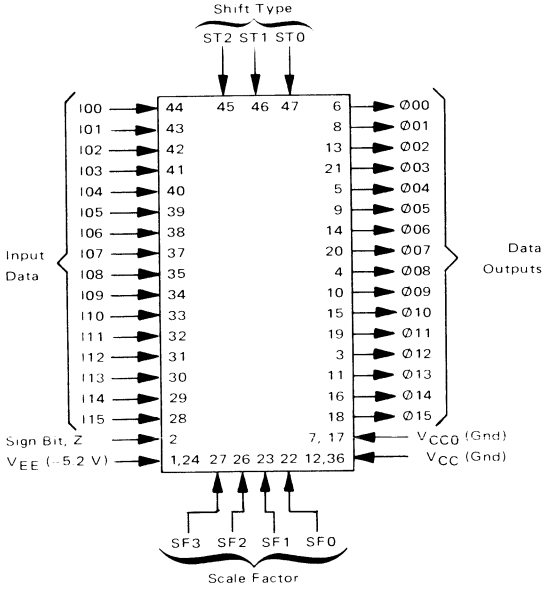
ADI-463

TABLE OF CONTENTS

IMPORTANT FEATURES

1. Three hundred gate complexity reduces package count considerably while increasing system speed.
2. Sixteen separate data inputs and sixteen data outputs are available with only two levels of gating separating them for high-speed operation. The sign bit input goes through only one level of gating.
3. Three shift type select lines are used to select eight different shift functions including shift left, shift right, and rotate.
4. Four scale factor inputs select the number of positions (in binary and 2's complement for shift right and shift left) the data is to be shifted.
5. Sign bit input is used for arithmetic shifting and for sign extend operations. Also, the sign bit is used in logic shifting for use in both positive and negative logic systems.
6. The outputs may be disabled for array expansions by selecting the "ODA" function.
7. High-speed operation of 6 ns typ delay from Data-In to Data-Out, 6 ns typ delay from Sign Bit to Data-Out, and 12 ns typ delay from the select lines to the Data-Out.
8. Two different shifter arrays can be built. One array requires only two package delays for a shifter requiring up to 256 bits. The other array requires only one package delay but more packages. A 64-bit shifter requires ten MC10808s with two package delays or sixteen MC10808s with one package delay.
9. Fully compatible with the MECL 10,000 family.

INPUT/OUTPUT DIAGRAM – MC10808



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating		Symbol	Value	Unit
Supply Voltage (V_{CC} = 0)		V_{EE}	-8 to 0	Vdc
Input Voltage (V_{CC} = 0)		V_{in}	0 to V_{EE}	Vdc
Output Source Current	Cont	I_o	< 50	mAdc
	Surge		< 100	
Storage Temperature		T_{stg}	-55 to +150	°C
Junction Temperature		T_j	165	

NOTE: Permanent device damage may occur if absolute maximum ratings are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

SYSTEM OVERVIEW

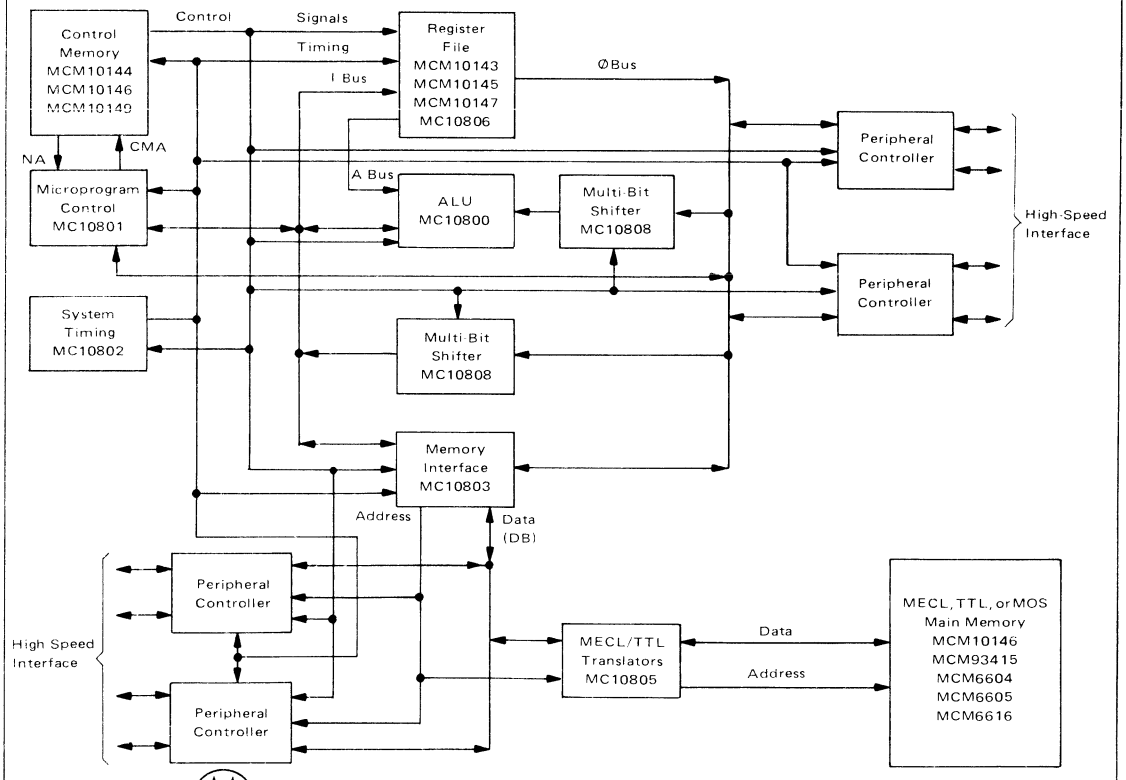
The Motorola M10800 family of LSI processor circuits combines the cost and size advantages of LSI with system design flexibility. Each family part is a major system building block which can be interconnected and programmed for a wide range of processor applications. Figure 1 illustrates a method of using the various circuits in a general purpose processor. The MC10800 4-Bit ALU Slice performs the various arithmetic, logic, and shift functions. This circuit features full BCD capability and a complete set of status outputs. The MC10801 Microprogram Control Function addresses and sequences through microprogram control memory. A set of 16 control instructions provides for direct jumps, conditional branches, and subroutines within microprogram. The MC10802 Timing Function generates clock phases and features single cycle or single phase clock increment for troubleshooting or diagnostics. The MC10803 Memory Interface Function interfaces between the LSI processor circuits and other parts of a system. The circuit generates memory addresses and provides for the bidirectional transfer of processor data.

In systems that use floating point data manipulation in high-speed systems, the MC10808 provides the shifting required for prenormalization or alignment of exponents. There are two ways that the MC10808 can be interconnected into the system as shown in Figure 1. One way is to connect the data input of the MC10808 to the Ø Bus and the output to the I Bus. Then the accumulator of the M10800, the external register file, or the register file of the M10803 can be shifted onto the I Bus and loaded back into the accumulator or register file. If the shifter input is connected to Ø Bus and if the output is connected to the Ø Bus input of the MC10800, then data in register file can be shifted before it is operated on by the ALU of the MC10800. Then the result may be loaded back into the register file using the I Bus.

The MC10808 performs the shift operation asynchronously with the number of shift positions determined by the shift type select and the scale factor. The speed for an equivalent operation using shift registers is a function of the number of clock pulses required to perform the shift.

Versatility is a main point of the M10800 family. The block diagram in Figure 1 is intended to illustrate the purpose of the various LSI functions and not restrict the designer to any particular system configuration or application.

FIGURE 1 – TYPICAL SYSTEM CONFIGURATION



PIN ASSIGMENTS

Pin Designation	Pin Number	Description
I00	44	Input Data – Bit 0 (LSB)
I01	43	Input Data – Bit 1
I02	42	Input Data – Bit 2
I03	41	Input Data – Bit 3
I04	40	Input Data – Bit 4
I05	39	Input Data – Bit 5
I06	38	Input Data – Bit 6
I07	37	Input Data – Bit 7
I08	35	Input Data – Bit 8
I09	34	Input Data – Bit 9
I10	33	Input Data – Bit 10
I11	32	Input Data – Bit 11
I12	31	Input Data – Bit 12
I13	30	Input Data – Bit 13
I14	29	Input Data – Bit 14
I15	28	Input Data – Bit 15 (MSB)
Ø00	6	Output Data – Bit 0 (LSB)
Ø01	8	Output Data – Bit 1
Ø02	13	Output Data – Bit 2
Ø03	21	Output Data – Bit 3
Ø04	5	Output Data – Bit 4
Ø05	9	Output Data – Bit 5
Ø06	14	Output Data – Bit 6
Ø07	20	Output Data – Bit 7
Ø08	4	Output Data – Bit 8
Ø09	10	Output Data – Bit 9
Ø10	15	Output Data – Bit 10
Ø11	19	Output Data – Bit 11
Ø12	3	Output Data – Bit 12
Ø13	11	Output Data – Bit 13
Ø14	16	Output Data – Bit 14
Ø15	18	Output Data – Bit 15
ST0	47	Shift Type – Select Input
ST1	46	Shift Type – Select Input
ST2	45	Shift Type – Select Input
SF0	22	Scale Factor – LSB Input
SF1	23	Scale Factor – NLSB Input
SF2	26	Scale Factor – NMSB Input
SF3	27	Scale Factor – MSB Input
Z	2	Sign Bit
V_{CC}	12	Ground
V_{CC}	36	Ground
V_{CC0}	7	Ground
V_{CC0}	17	Ground
V_{EE}	1	-5.2 Volt Supply
V_{EE}	24	-5.2 Volt Supply

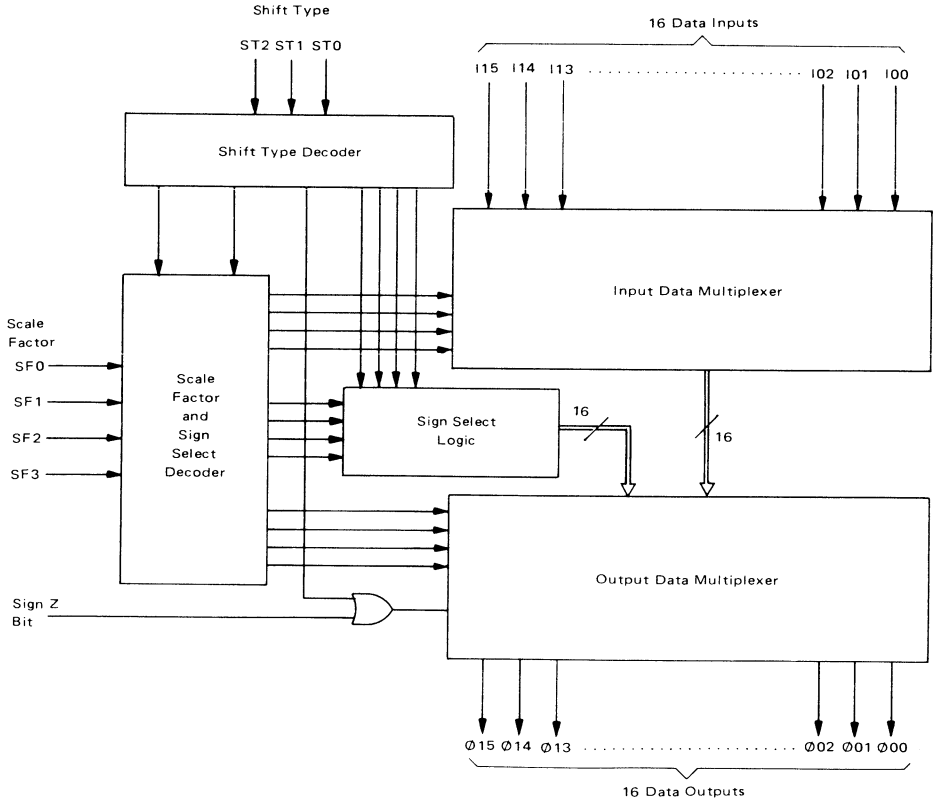
Pins 25 and 48 not used

ARCHITECTURAL DESCRIPTION

A functional block diagram of the MC10808 Programmable Multi-Bit Shifter is shown in Figure 2. There are sixteen inputs and sixteen outputs with two levels of gating to perform the shifting. There are three shift type select inputs—ST2, ST1, and ST0—that are used to select the appropriate shifting function. Also, four scale factor inputs specify the number of positions that the input data should be shifted or rotated. A sign bit input is used for arithmetic shift right or left and sign extend operations. The outputs can be disabled for wire-ANDing (negative logic) other device outputs by selecting the "ODA" command.

The input multiplexers do a right rotate only of 0, 1, 2, or 3 positions and the output multiplexers do a right rotate only of 0, 4, 8, or 12 positions. The sign select logic can force the Z input (see Figure 2) into the data output positions as selected by the shift type and the sign select scale factor. In this manner the function select (see Table 1) can be implemented to perform all the functions listed such as arithmetic shift right and left, rotate right and left, 2's complement right and left, sign extend, and output disable.

FIGURE 2 – FUNCTIONAL BLOCK DIAGRAM



MC10808 INPUT/OUTPUT SIGNALS

Pin Designation/Name	Function
Z/Sign Bit	The sign bit is used to specify the sign during an arithmetic shift or sign extend operation. The sign bit is usually connected to the most signficiant bit of the data word.
ST0, ST1, ST2/Shift Type Select	A description of the shift type select is described in Table 1.
SF0–SF3/Scale Factor Select	The truth tables for the scale factor versus various shift types are described in Tables 2 through 9.
I00–I15/Input Data	There are 16 input data lines for shifting to the output.
Ø00–Ø15/Output Data	There are 16 output data lines that contain the shifted data from the inputs.

FUNCTIONAL DESCRIPTION

Tables 1 through 9 describe the logical operation of the Programmable Multi-Bit Shifter (PMS) along with the block diagram in Figure 2. There are eight different shift types that may be selected as shown in Table 1. The following is a description of the various shift types. **All truth tables are expressed in negative logic with VOL being a logic 1 and VOH a logic 0.**

ALS–Arithmetic **S**hift **L**eft

As shown in Table 2, the input data is shifted to the left with the vacated bit positions filled with the logic level existing at the sign bit input. The sign bit input is connected to either VOL or VOH depending if the system uses positive or negative logic.

ARS–Arithmetic **S**hift **R**ight

As shown in Table 3, the input data is shifted to the right with the vacated bit positions filled with the sign bit for arithmetic shifting. For logic shifting, the sign bit input is connected to either VOL or VOH depending if the system uses positive or negative logic.

RLT–Rotate **L**ef**T**

As shown in Table 4, the input data is rotated to the left as specified by the binary number specified by the scale factor.

RRT–Rotate **R**igh**T**

This function is very useful in building shifter arrays requiring 16, 32, 64, 128, and 256 bits. As shown in Table 5, the input data is rotated to the right a number of positions as specified by the scale factor.

SRC–Shift **R**ight Using 2's **C**omplement

This function is very useful in shifter arrays having a one package delay that requires a shift left operation. One example is shown in Figure 4, a 32-bit shift/rotate array. Table 6 shows the truth table for the SRC function with the inputs shifted to the right as selected by the 2's complement of the scale factor. Negative logic 1s fill the vacated positions.

SLC–Shift **L**eft Using 2's **C**omplement

This function is very useful in implementing shifter arrays (one package delay) requiring a shift right operation. The SLC function is used to extend the number of bits to any number larger than 16 bits when performing an arithmetic or logic shift right. The SLC function can also be used in shifter arrays for performing the shift left operaton where the scale factor is in 2's complement notation. Table 7 shows the truth table for the SLC function. Note that logic 1s fill the vacated positions.

ODA–Output **D**is**A**ble

This function is used to disable the outputs to a negative logic 1 as shown in Table 8.

SBO–Sign **B**it is placed at all **O**utputs

This function places the sign bit at all the outputs regardless of the scale factor, as shown in Table 9. It is very useful in extending the sign in shifter arrays when performing an arithmetic shift right.

TABLE 1. SHIFT TYPE SELECT DESCRIPTION (NEGATIVE LOGIC)

Shift Type			Symbol	Description
ST2	ST1	ST0		
0	0	0	SBO	Sign Bit is placed at all Outputs. The Ø15 through Ø00 are filled with the sign bit for use in arithmetic shifting.
0	0	1	ODA	Output DisAble. The Ø15 through Ø00 outputs are forced to logic 1s, so that the device can be wire-ANDed to other device outputs.
0	1	0	SLC	Shift Left using 2's Complement. The I15 – I00 inputs are shifted to the left at the Ø15 – Ø00 outputs as selected by the 2's complement of the scale factor inputs SF3 – SF0. The vacated bit positions are filled with negative logic 1s.
0	1	1	SRC	Shift Right using 2's Complement. The I15 – I00 inputs are shifted to the right at the Ø15 – Ø00 outputs as selected by the 2's complement of the scale factor inputs SF3 – SF0. The vacated bit positions are filled with negative logic 1s.
1	0	0	RRT	Rotate RighT. The I15 - I00 inputs are rotated to the right at the Ø15 - Ø00 outputs as selected by the binary number specified by the scale factor inputs.
1	0	1	RLT	Rotate LefT. The I15 - I00 inputs are rotated to the left at the Ø15 - Ø00 outputs as selected by the binary number specified by the scale factor inputs.
1	1	0	ARS	Arithmetic Shift Right. The I15 – I00 inputs are shifted to the right at the Ø15 – Ø00 outputs as selected by the binary number specified by the scale factor inputs. The vacated bit positions are filled with the sign bit.
1	1	1	ALS	Arithmetic Shift Left. The I15 – I00 inputs are shifted to the left at the Ø15 – Ø00 outputs as selected by the binary number specified by the scale factor inputs. The vacated bit positions are filled with the sign bit.

TABLE 2. OUTPUT TRUTH TABLE FOR ARITHMETIC SHIFT LEFT (ST2 = 1, ST1 = 1, ST0 = 1)

Scale Factor				Output													
SF3	SF2	SF1	SF0	Ø15	Ø14	Ø13	Ø12	Ø11	Ø10	Ø09	Ø08	Ø07	Ø06	Ø05	Ø04	Ø03	Ø02	Ø01	Ø00
0	0	0	0	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00
0	0	0	1	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	Z
0	0	1	0	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	Z	Z
0	0	1	1	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	Z	Z	Z
0	1	0	0	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	Z	Z	Z	Z
0	1	0	1	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	Z	Z	Z	Z	Z
0	1	1	0	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	Z	Z	Z	Z	Z	Z
0	1	1	1	I08	I07	I06	I05	I04	I03	I02	I01	I00	Z	Z	Z	Z	Z	Z	Z
1	0	0	0	I07	I06	I05	I04	I03	I02	I01	I00	Z	Z	Z	Z	Z	Z	Z	Z
1	0	0	1	I06	I05	I04	I03	I02	I01	I00	Z	Z	Z	Z	Z	Z	Z	Z	Z
1	0	1	0	I05	I04	I03	I02	I01	I00	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
1	0	1	1	I04	I03	I02	I01	I00	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
1	1	0	0	I03	I02	I01	I00	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
1	1	0	1	I02	I01	I00	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
1	1	1	0	I01	I00	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z
1	1	1	1	I00	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

TABLE 3. OUTPUT TRUTH TABLE FOR ARITHMETIC SHIFT RIGHT (ST2 = 1, ST1 = 1, ST0 = 0)

Scale Factor				Output													
SF3	SF2	SF1	SF0	Ø15	Ø14	Ø13	Ø12	Ø11	Ø10	Ø09	Ø08	Ø07	Ø06	Ø05	Ø04	Ø03	Ø02	Ø01	Ø00
0	0	0	0	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00
0	0	0	1	Z	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01
0	0	1	0	Z	Z	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02
0	0	1	1	Z	Z	Z	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03
0	1	0	0	Z	Z	Z	Z	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04
0	1	0	1	Z	Z	Z	Z	Z	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05
0	1	1	0	Z	Z	Z	Z	Z	Z	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06
0	1	1	1	Z	Z	Z	Z	Z	Z	Z	I15	I14	I13	I12	I11	I10	I09	I08	I07
1	0	0	0	Z	Z	Z	Z	Z	Z	Z	Z	I15	I14	I13	I12	I11	I10	I09	I08
1	0	0	1	Z	Z	Z	Z	Z	Z	Z	Z	Z	I15	I14	I13	I12	I11	I10	I09
1	0	1	0	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	I15	I14	I13	I12	I11	I10
1	0	1	1	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	I15	I14	I13	I12	I11
1	1	0	0	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	I15	I14	I13	I12
1	1	0	1	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	I15	I14	I13
1	1	1	0	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	I15	I14
1	1	1	1	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	I15

TABLE 4. OUTPUT TRUTH TABLE FOR LEFT ROTATE (ST2 = 1, ST1 = 0, ST0 = 1)

Scale Factor				Output													
SF3	SF2	SF1	SF0	Ø15	Ø14	Ø13	Ø12	Ø11	Ø10	Ø09	Ø08	Ø07	Ø06	Ø05	Ø04	Ø03	Ø02	Ø01	Ø00
0	0	0	0	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00
0	0	0	1	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	I15
0	0	1	0	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	I15	I14
0	0	1	1	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	I15	I14	I13
0	1	0	0	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	I15	I14	I13	I12
0	1	0	1	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	I15	I14	I13	I12	I11
0	1	1	0	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	I15	I14	I13	I12	I11	I10
0	1	1	1	I08	I07	I06	I05	I04	I03	I02	I01	I00	I15	I14	I13	I12	I11	I10	I09
1	0	0	0	I07	I06	I05	I04	I03	I02	I01	I00	I15	I14	I13	I12	I11	I10	I09	I08
1	0	0	1	I06	I05	I04	I03	I02	I01	I00	I15	I14	I13	I12	I11	I10	I09	I08	I07
1	0	1	0	I05	I04	I03	I02	I01	I00	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06
1	0	1	1	I04	I03	I02	I01	I00	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05
1	1	0	0	I03	I02	I01	I00	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04
1	1	0	1	I02	I01	I00	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03
1	1	1	0	I01	I00	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02
1	1	1	1	I00	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01

TABLE 5. OUTPUT TRUTH TABLE FOR RIGHT ROTATE (ST2 = 1, ST1 = 0, ST0 = 0)

Scale Factor				Output													
SF3	SF2	SF1	SF0	Ø15	Ø14	Ø13	Ø12	Ø11	Ø10	Ø09	Ø08	Ø07	Ø06	Ø05	Ø04	Ø03	Ø02	Ø01	Ø00
0	0	0	0	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00
0	0	0	1	I00	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01
0	0	1	0	I01	I00	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02
0	0	1	1	I02	I01	I00	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03
0	1	0	0	I03	I02	I01	I00	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04
0	1	0	1	I04	I03	I02	I01	I00	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05
0	1	1	0	I05	I04	I03	I02	I01	I00	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06
0	1	1	1	I06	I05	I04	I03	I02	I01	I00	I15	I14	I13	I12	I11	I10	I09	I08	I07
1	0	0	0	I07	I06	I05	I04	I03	I02	I01	I00	I15	I14	I13	I12	I11	I10	I09	I08
1	0	0	1	I08	I07	I06	I05	I04	I03	I02	I01	I00	I15	I14	I13	I12	I11	I10	I09
1	0	1	0	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	I15	I14	I13	I12	I11	I10
1	0	1	1	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	I15	I14	I13	I12	I11
1	1	0	0	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	I15	I14	I13	I12
1	1	0	1	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	I15	I14	I13
1	1	1	0	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	I15	I14
1	1	1	1	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	I15

TABLE 6. OUTPUT TRUTH TABLE FOR SHIFT RIGHT, 2'S COMPLEMENT (ST2 = 0, ST1 = 1, ST0 = 1)

Scale Factor				Output														
SF3	SF2	SF1	SF0	Ø15	Ø14	Ø13	Ø12	Ø11	Ø10	Ø09	Ø08	Ø07	Ø06	Ø05	Ø04	Ø03	Ø02	Ø01	Ø00
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	I15
0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	I15	I14
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	I15	I14	I13
0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	I15	I14	I13	I12
0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	I15	I14	I13	I12	I11
0	1	1	0	1	1	1	1	1	1	1	1	1	1	I15	I14	I13	I12	I11	I10
0	1	1	1	1	1	1	1	1	1	1	1	1	I15	I14	I13	I12	I11	I10	I09
1	0	0	0	1	1	1	1	1	1	1	1	I15	I14	I13	I12	I11	I10	I09	I08
1	0	0	1	1	1	1	1	1	1	1	I15	I14	I13	I12	I11	I10	I09	I08	I07
1	0	1	0	1	1	1	1	1	1	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06
1	0	1	1	1	1	1	1	1	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05
1	1	0	0	1	1	1	1	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04
1	1	0	1	1	1	1	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03
1	1	1	0	1	1	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02
1	1	1	1	1	I15	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01

TABLE 7. OUTPUT TRUTH TABLE FOR SHIFT LEFT, 2'S COMPLEMENT (ST2 = 0, ST1 = 1, ST0 = 0)

Scale Factor				Output														
SF3	SF2	SF1	SF0	Ø15	Ø14	Ø13	Ø12	Ø11	Ø10	Ø09	Ø08	Ø07	Ø06	Ø05	Ø04	Ø03	Ø02	Ø01	Ø00
0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	0	1	I00	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	0	I01	I00	1	1	1	1	1	1	1	1	1	1	1	1	1	1
0	0	1	1	I02	I01	I00	1	1	1	1	1	1	1	1	1	1	1	1	1
0	1	0	0	I03	I02	I01	I00	1	1	1	1	1	1	1	1	1	1	1	1
0	1	0	1	I04	I03	I02	I01	I00	1	1	1	1	1	1	1	1	1	1	1
0	1	1	0	I05	I04	I03	I02	I01	I00	1	1	1	1	1	1	1	1	1	1
0	1	1	1	I06	I05	I04	I03	I02	I01	I00	1	1	1	1	1	1	1	1	1
1	0	0	0	I07	I06	I05	I04	I03	I02	I01	I00	1	1	1	1	1	1	1	1
1	0	0	1	I08	I07	I06	I05	I04	I03	I02	I01	I00	1	1	1	1	1	1	1
1	0	1	0	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	1	1	1	1	1	1
1	0	1	1	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	1	1	1	1	1
1	1	0	0	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	1	1	1	1
1	1	0	1	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	1	1	1
1	1	1	0	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	1	1
1	1	1	1	I14	I13	I12	I11	I10	I09	I08	I07	I06	I05	I04	I03	I02	I01	I00	1

TABLE 8. OUTPUT TRUTH TABLE FOR OUTPUT DISABLE (ODA) (ST2 = 0, ST1 = 0, ST0 = 1)

Scale Factor				Output														
SF3	SF2	SF1	SF0	Ø15	Ø14	Ø13	Ø12	Ø11	Ø10	Ø09	Ø08	Ø07	Ø06	Ø05	Ø04	Ø03	Ø02	Ø01	Ø00
X	X	X	X	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

X = Don't Care

TABLE 9. OUTPUT TRUTH TABLE FOR SIGN BIT PLACED AT ALL OUTPUTS (SBO) (ST2 = 0, ST1 = 0, ST0 = 0)

Scale Factor				Output														
SF3	SF2	SF1	SF0	Ø15	Ø14	Ø13	Ø12	Ø11	Ø10	Ø09	Ø08	Ø07	Ø06	Ø05	Ø04	Ø03	Ø02	Ø01	Ø00
X	X	X	X	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z	Z

APPLICATION INFORMATION

Table 10 shows a function select that can be used in building shift/rotate arrays with only two select lines labeled X and Y. The important functions that are normally required in a shifter are included such as Rotate Right, Logic and Arithmetic Right, and Logic Left. A rotate left can be obtained by using the rotate right command and changing the scale factor select lines to the 2's complement of binary number to be rotated. A rotate left command could be added to Table 10; however, three function select lines would be required.

Figures 3 through 7 show some examples of implementing shift arrays using the selected commands shown in Table 10. **These examples are actually applicable to positive logic systems even though the drawings are shown using negative logic.** The reason is that negative logic 1s (VOH) are shifted into the vacated bit positions for logic shift right and left which is the correct format for positive logic systems.

Two different shifter arrays can be built to satisfy the selected commands shown in Table 10. Figures 3, 4, 5, and 6a show the design for implementing a 16-, 32-, 48-, and 64-bit shift/rotate array with only one package delay. The truth table and equations for designing a 64-bit shift/rotate array are shown in Figure 6b. Other bit configurations can be designed using these techniques. Any bit configuration could be designed by adjusting the scale factor inputs on certain devices in the array during rotate and shift left commands. The secret to the design of the shift/rotate array with one package delay is the wire "ANDing" of the common bit outputs and the 2's complement shift left and right operations.

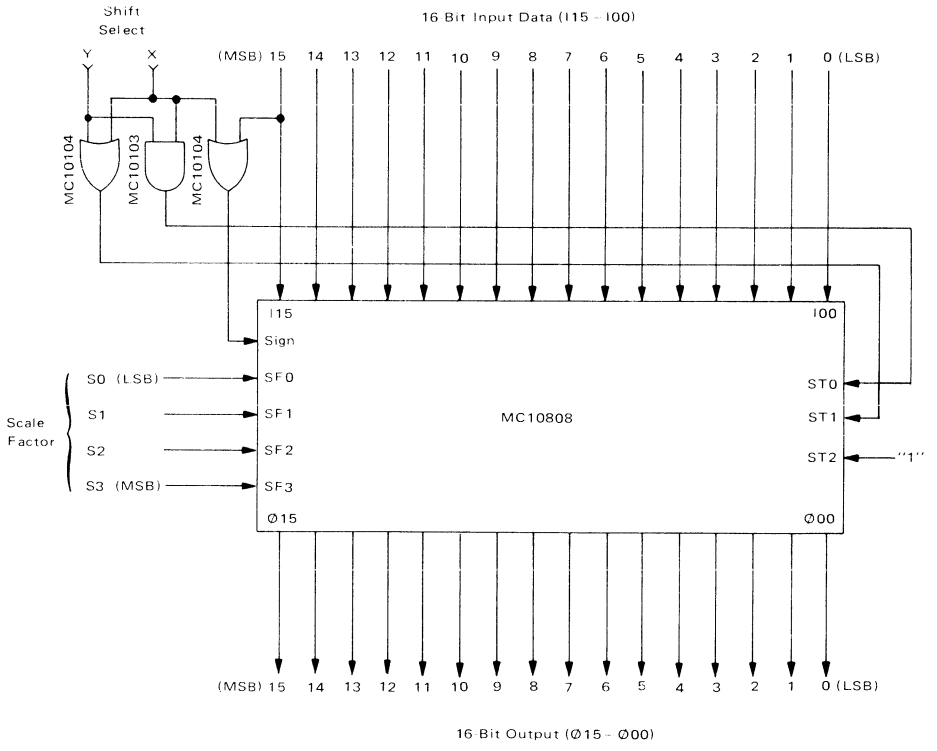
The other shifter array requires two package delays from data-in to data-out. Figure 7 is an example of a 64-bit shift/rotate with two package delays. Note that only three additional gates are required along with only ten of the shifter devices to complete the design. The top array, devices (1) through (6), shifts the input data right or left, or right rotates the data 0, 1, 2, or 3 positions as defined by the two least significant scale factor inputs, S0 and S1. The bottom array, devices (7) through (10), completes the shift array by the unique interconnections of the outputs of devices (1) through (6) to inputs of devices (7) through (10). The four upper scale factor inputs, S2 through S5, select the shifting of the input data in multiples of four positions at a time. The interconnection and design of the shifting array for devices (1) through (10) is unique to the shift function (X and Y) code shown in Table 10. The result is a highly flexible design that can be implemented with many variations in shift functions. Using the same techniques shown in Figure 7, a 128-bit shift/rotate array with two package delays could be built with twenty-four MC10808s or a 256-bit shift/rotate array which would require sixty-three MC10808s and only one additional gate package.

TABLE 10. FUNCTION SELECT DESCRIPTION THAT CAN BE USED WITH VARIOUS SHIFT/ROTATE ARRAYS

Function Select		Symbol	Description
Y	X		
0	0	RRS	Rotate Right Shift. The input data is rotated to the right at the outputs as selected by the binary number specified by the scale factor inputs.
0	1	LSR	Logic Shift Right. The input data is shifted to the right at the outputs as selected by the binary number specified by the scale factor inputs. The vacated bit positions are filled with logic 1s (negative logic).
1	0	ASR	Arithmetic Shift Right. The input data is shifted to the right at the outputs as selected by the binary number specified by the scale factor inputs. The vacated bit positions are filled with the sign bit.
1	1	LSL	Logic Shift Left. The input data is shifted to the left at the outputs as selected by the binary number specified by the scale factor inputs. The vacated bit positions are filled with logic 1s (negative logic).

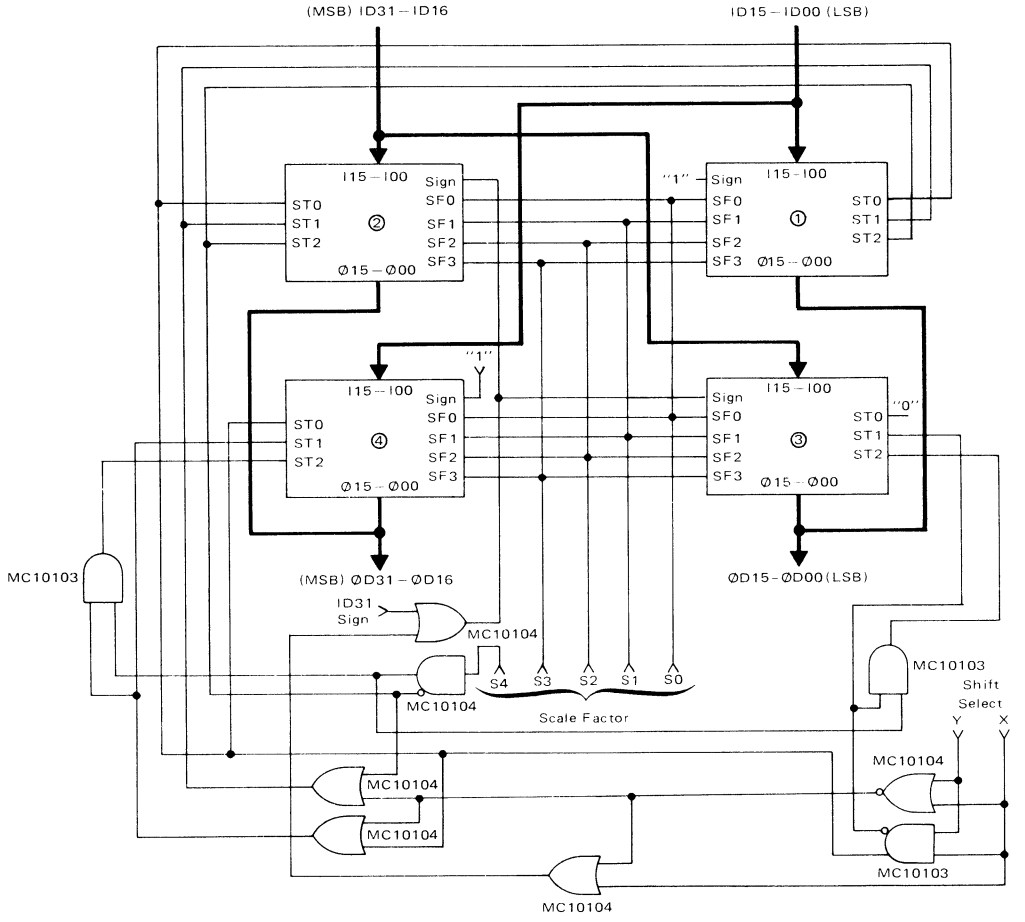
NOTE: The function select shown above is used in the shift/rotate arrays shown in Figures 3 through 7.

FIGURE 3 – 16-BIT SHIFT/ROTATE ARRAY



Negative logic is used.

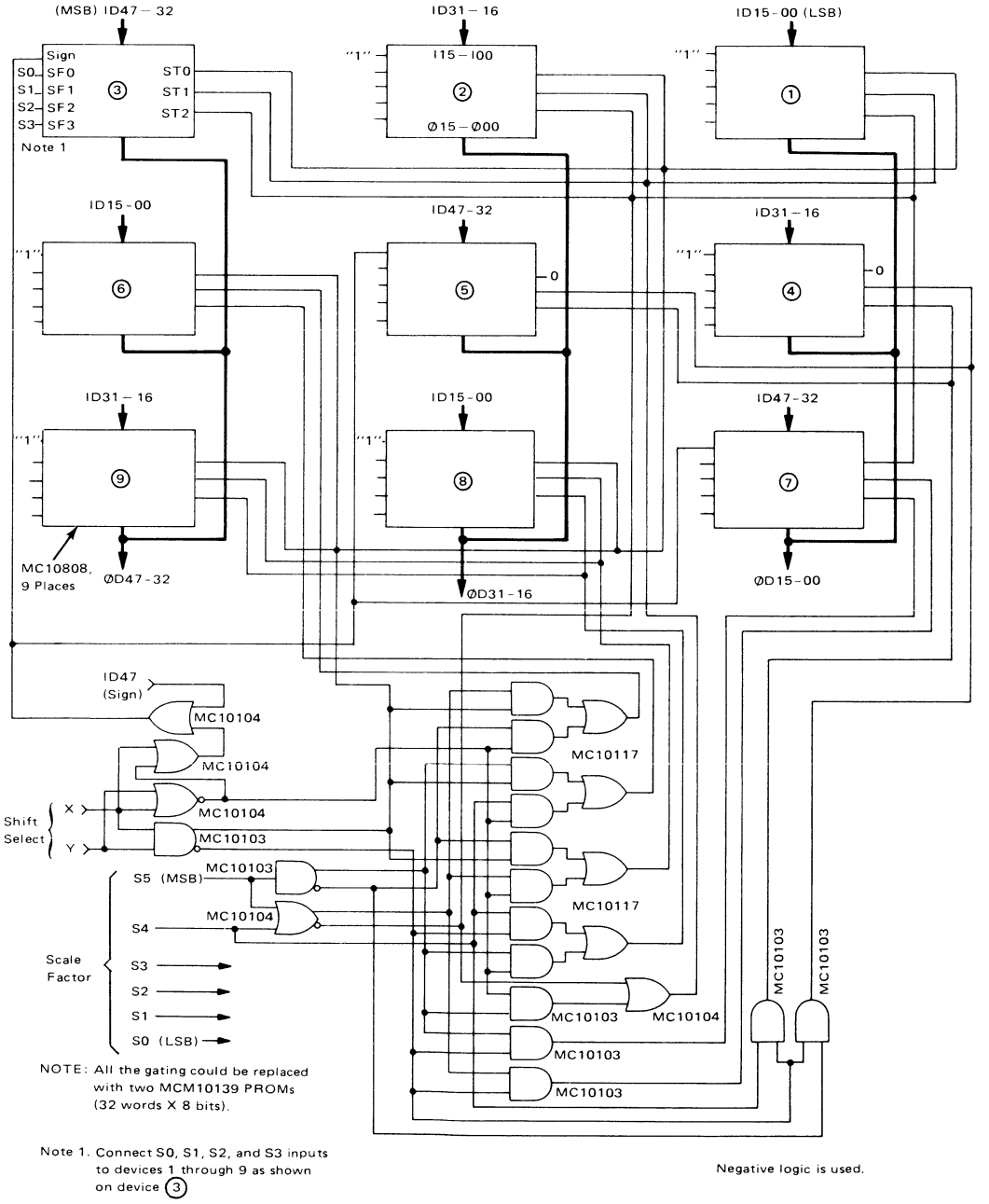
FIGURE 4 – 32-BIT SHIFT/ROTATE ARRAY



Negative Logic is used.

Shift Select		
Y	X	Shift Function
0	0	Rotate Right
0	1	Logic Right
1	0	Arithmetic Right
1	1	Logic Left

FIGURE 5 – 48-BIT SHIFT/ROTATE ARRAY WITH ONE PACKAGE DELAY



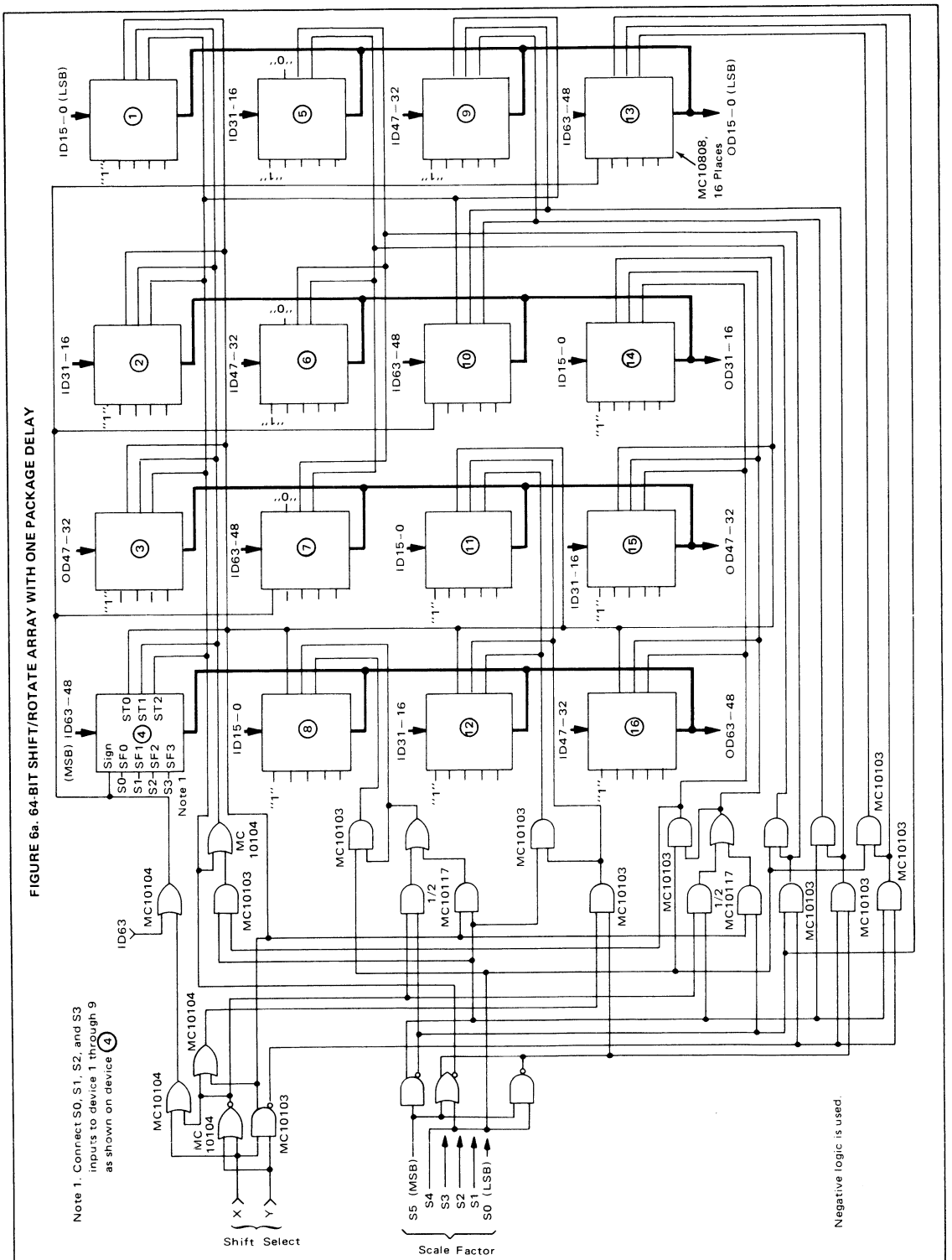


FIGURE 6a. 64-BIT SHIFT/ROTATE ARRAY WITH ONE PACKAGE DELAY

MOTOROLA Semiconductor Products Inc.

FIGURE 6b. TRUTH TABLE FOR 64-BIT SHIFTER (See Figure 6a)

Shift Select (See Table 10)			Scale Factor Bits		Sign Bit Devices 4, 7, 10, 13				Devices 1, 2, 3, 4			Device 8			Devices 5, 6, 7			Devices 11, 12			Devices 9, 10			Devices 14, 15, 16			Device 13		
Mnemonic	Y	X	S5	S4	Z4	Z7	Z10	Z13	ST2	ST1	ST0	ST2	ST1	ST0	ST2	ST1	ST0	ST2	ST1	ST0	ST2	ST1	ST0	ST2	ST1	ST0	ST2	ST1	ST0
RRS	0	0	0	0	1	1	1	1	1	1	0	0	1	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	1
ARS	1	0	0	0	ID63	–	–	–	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	1
LLS	1	1	0	0	1	1	1	1	1	1	1	0	0	1	0	0	0	0	0	1	0	0	1	0	1	1	0	0	1
LRS	0	1	0	0	1	1	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	1
RRS	0	0	0	1	1	1	1	1	0	0	0	1	1	0	1	1	0	0	1	0	0	1	0	0	0	0	0	0	1
ARS	1	0	0	1	ID63	ID63	–	–	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1
LLS	1	1	0	1	1	1	1	1	0	0	1	0	0	1	0	0	0	0	1	1	0	0	0	1	1	1	0	0	1
LRS	0	1	0	1	1	1	1	1	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0	0	0	1
RRS	0	0	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0	0	1	0	0	1	0
ARS	1	0	1	0	ID63	ID63	ID63	–	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0
LLS	1	1	1	0	1	1	1	1	0	0	1	0	1	1	0	0	0	1	1	1	0	0	0	0	0	1	0	0	0
LRS	0	1	1	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	1	0
RRS	0	0	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0
ARS	1	0	1	1	ID63	ID63	ID63	ID63	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
LLS	1	1	1	1	1	1	1	1	0	0	1	1	1	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0
LRS	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

– = Don't Care

$Z_4 = ID63 + [X + (\overline{X+Y})]$

$Z_7 = Z_4$

$Z_{10} = Z_4$

$Z_{13} = Z_4$

Device 8

$$\begin{cases} ST0_8 = X \cdot Y \\ ST1_8 = S5 \cdot (X \cdot Y) + \overline{S5} \cdot (\overline{X+Y}) \\ ST2_8 = ST1_8 \cdot S4 \end{cases}$$

Devices 11, 12

$$\begin{cases} ST0_{11} = X \cdot Y \\ ST1_{11} = (S5 \oplus S4) \cdot (\overline{X \oplus Y}) \\ ST2_{11} = ST1_{11} \cdot S5 \end{cases}$$

Devices 14, 15, 16

$$\begin{cases} ST0_{14} = X \cdot Y \\ ST1_{14} = \overline{S5} \cdot (X \cdot Y) + S5 \cdot (\overline{X+Y}) \\ ST2_{14} = ST1_{14} \cdot S4 \end{cases}$$

Devices 1, 2, 3, 4

$$\begin{cases} ST0_1 = X \cdot Y \\ ST1_1 = (\overline{S5+S4}) + ST2_{14} \cdot S5 \\ ST2_1 = (\overline{S4+S4}) \end{cases}$$

Device 13

$$\begin{cases} ST1_{13} = S5 \cdot (\overline{XY}) \\ ST2_{13} = ST1_{13} \cdot S4 \\ ST0_{13} = \overline{S5} \end{cases}$$

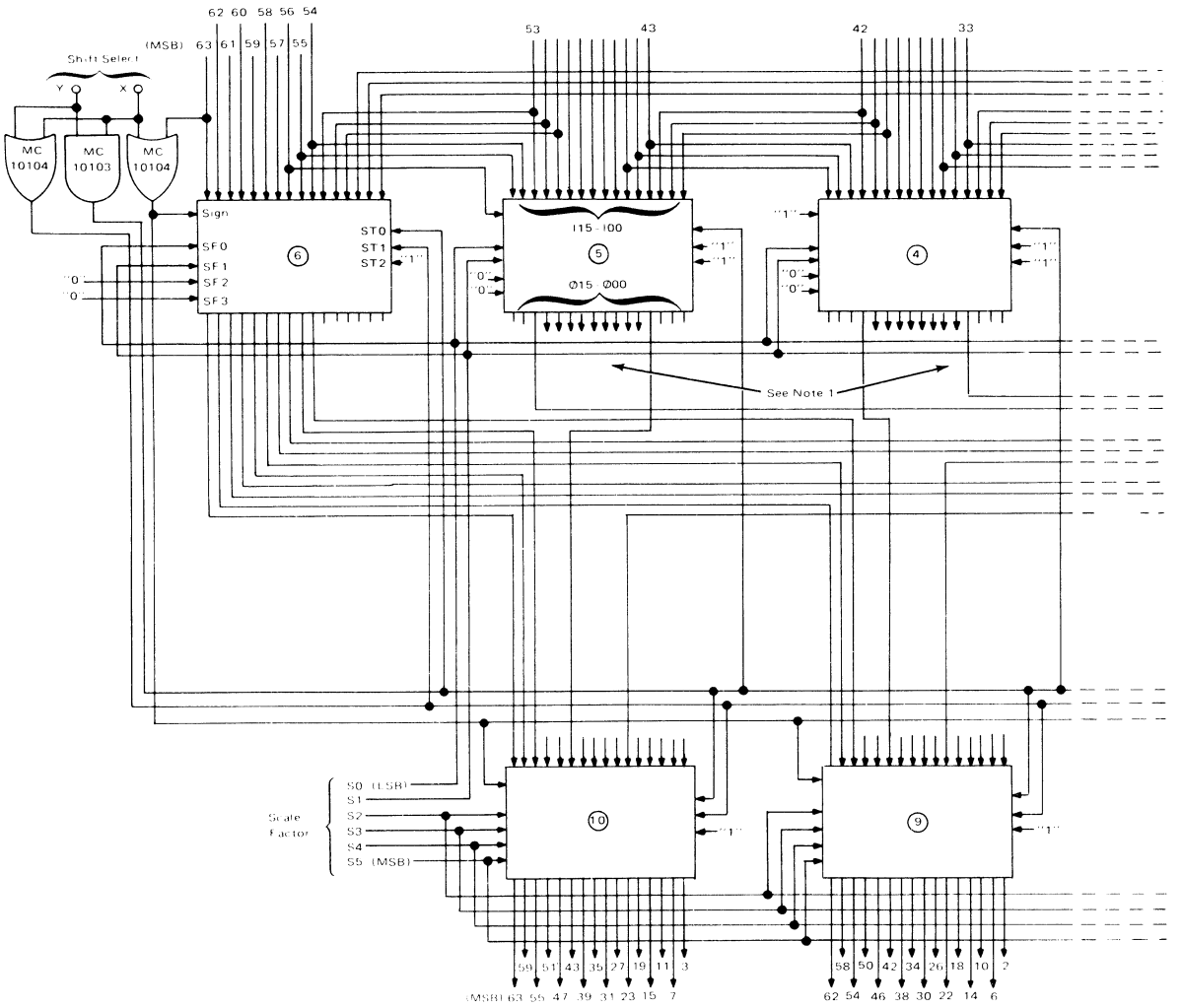
Devices 9, 10

$$\begin{cases} ST1_9 = (S5 \oplus S4) \cdot \overline{XY} \\ ST2_9 = ST1_9 \cdot S5 \\ ST0_9 = \overline{S5} \cdot \overline{S4} \end{cases}$$

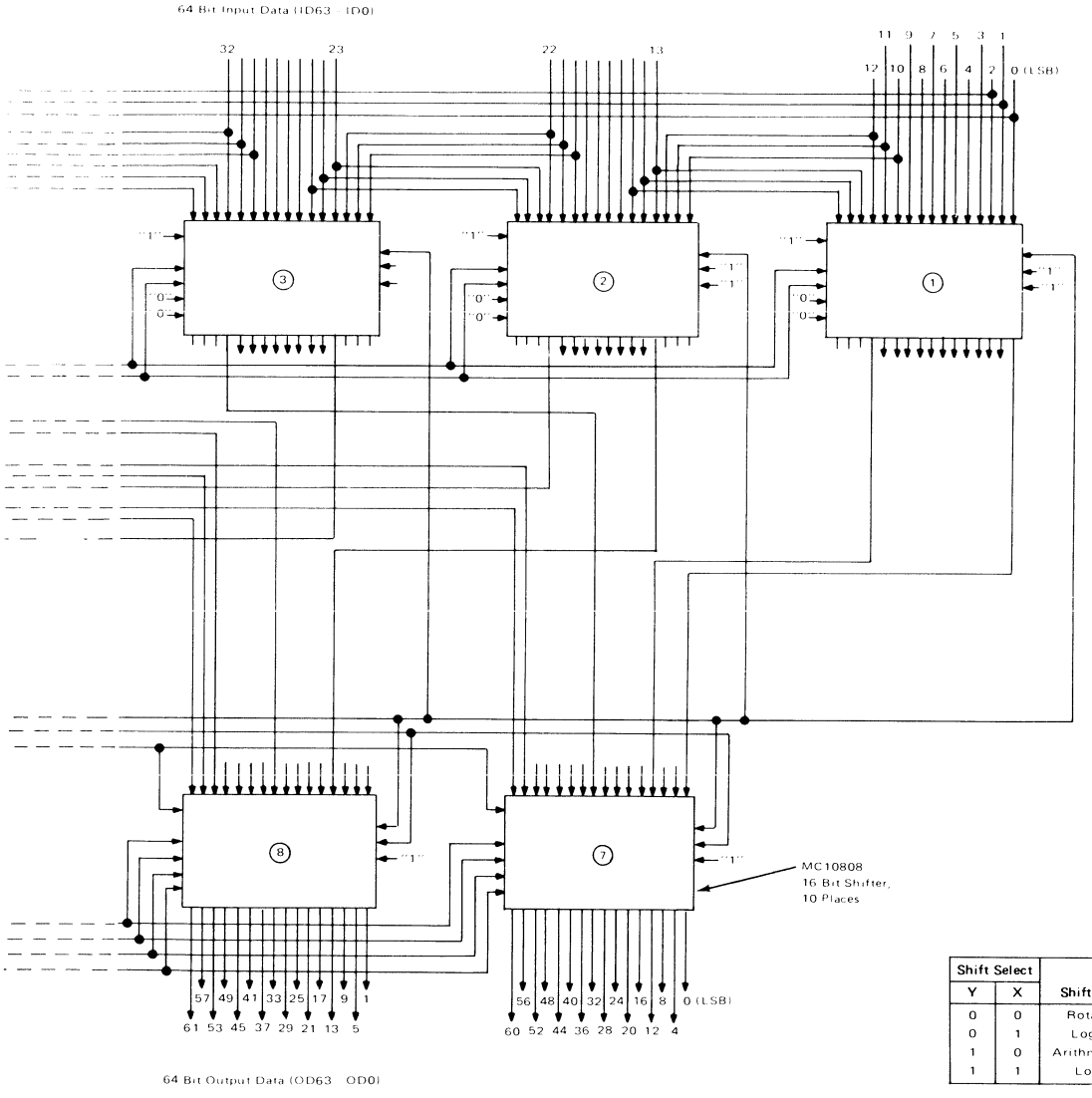
Devices 5, 6, 7

$$\begin{cases} ST1_5 = \overline{S5} \cdot (\overline{X \cdot Y}) \\ ST2_5 = ST1_5 \cdot S4 \end{cases}$$

FIGURE 7 – 64-BIT SHIFT/ROTATE ARRAY



NOTE 1: The outputs of devices (1) through (5) are connected to devices (7) through (10) in the same manner as shown for connecting the outputs of device (6).



Shift Select		
Y	X	Shift Function
0	0	Rotate Right
0	1	Logic Right
1	0	Arithmetic Right
1	1	Logic Left

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value	Unit
Supply Voltage (V_{CC} = 0 Volts)	V_{EE}	−4.68 to −5.72	Vdc
Operating Temperature (Functional)	T_A	−30 to +85	°C
Output Drive	—	50 Ω to −2.0 Vdc	—

ELECTRICAL CHARACTERISTICS

Each MECL 10,000 series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 linear fpm is maintained. Outputs are terminated through a 50-ohm resistor to −2.0 volts. Test procedures are shown for only one input, or for one set of input conditions. Other inputs tested in the same manner.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}
−30°C	−0.890	−1.890	−1.205	−1.500	−5.2
+25°C	−0.810	−1.850	−1.105	−1.475	−5.2
+85°C	−0.700	−1.825	−1.035	−1.440	−5.2

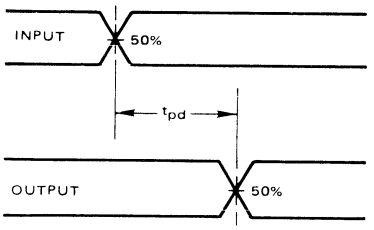
Characteristic	Symbol	Pin Under Test	MC10808 TEST LIMITS −30°C Min	−30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	VOLTAGE APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_{EE}	1,24	—	—	—	278	348	—	—	mAdc	—	—	—	—	1,24	—
Input Current	I_{inH}	22	—	—	—	—	330	—	—	μAdc	22	—	—	—	1,24	7,12,
		2	—	—	—	—	390	—	—	↓	2	—	—	—	↓	17,36
		44	—	—	—	—	435	—	—		44	—	—	—		↓
	I_{inL}	44	—	—	0.5	—	—	—	—		—	44	—	—		
Logic "0" Output Voltage	V_{OH}	6	−1.060	−0.890	−0.960	—	−0.810	−0.890	−0.700	Vdc	44,45, 46,47	—	—	—	1,24	7,12, 17,36
Logic "1" Output Voltage	V_{OL}	6	−1.890	−1.675	−1.850	—	−1.650	−1.825	−1.615	Vdc	45,46, 47	44	—	—	1,24	7,12, 17,36
Logic "0" Threshold Voltage	V_{OHA}	6	−1.080	—	−0.980	—	—	−0.910	—	Vdc	44,46, 47	—	45	—	1,24	7,12, 17,36
Logic "1" Threshold Voltage	V_{OLA}	6	—	−1.655	—	—	−1.630	—	−1.595	Vdc	45,46, 47	—	—	44	1,24	7,12, 17,36

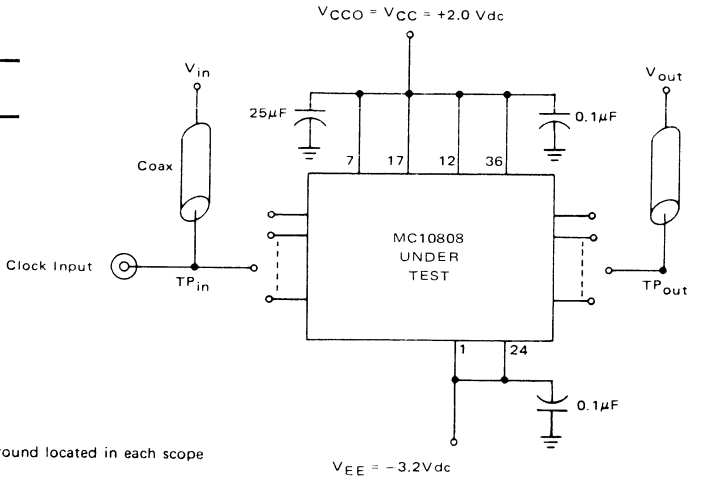
PROPAGATION DELAY TIMES
(Nanoseconds at 0 to 70°C to
Data Outputs (Ø15–Ø00)

	Typ
Data Inputs, I15–I00	6
Sign Bit, Z	6
Scale Factor, SF0–SF3	12
Shift Type, ST0–ST2	12

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

PROPAGATION DELAYS

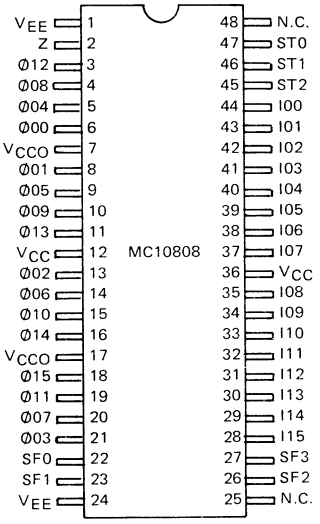




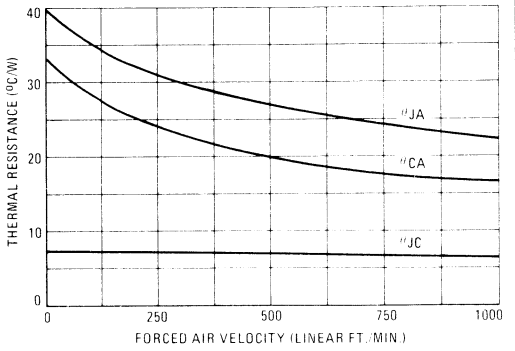
50 ohm termination to ground located in each scope channel input.

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. Wire length should be <¼ inch from TP_{in} to input pin and TP_{out} to output pin.

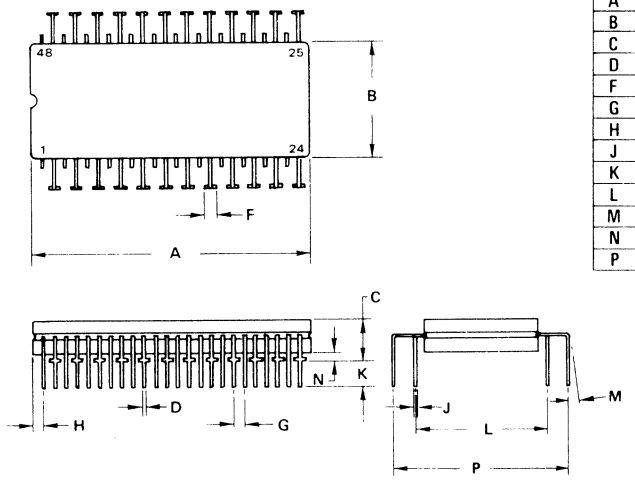
PIN ASSIGNMENT



THERMAL CHARACTERISTICS
(TYPICAL)



PACKAGE DIMENSIONS



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.57	5.59	0.180	0.220
D	0.38	0.53	0.015	0.021
F	1.14	1.40	0.045	0.055
G	1.27 BSC		0.050 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.54	3.30	0.100	0.130
L	15.24 BSC		0.600 BSC	
M	–	7°	–	7°
N	0.51	1.52	0.020	0.060
P	20.32 BSC		0.800 BSC	

Case 725–01

A socket for the QUIL package is available from ELECTRONIC MOLDING CORPORATION. (Part number 7178-295-5)

QUIL is a trademark of Motorola Inc.

MOTOROLA Semiconductors

MC10318

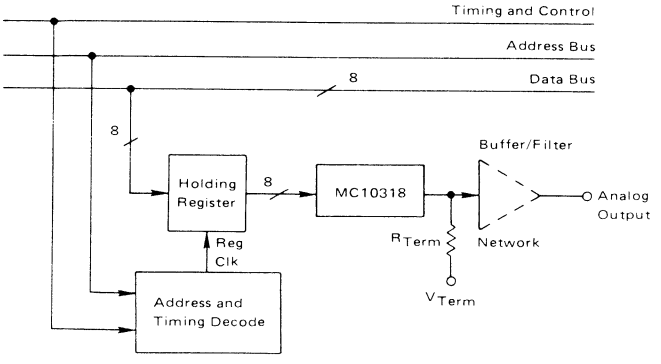
Advance Specifications and Applications Information

HIGH SPEED 8-BIT DIGITAL-TO-ANALOG CONVERTER

The MC10318 is a high speed 8-bit D/A converter capable of data conversion rates in excess of 25 MHz. It is intended for applications in high speed instrumentation and communication equipment, display processing, storage oscilloscopes, radar processing, and TV broadcast systems. The inputs are compatible with MECL 10,000 series logic, while the complementary current outputs have 51 mA full scale capability. 8-bit accurate (±1/2 LSB) and monotonic over the full temperature range, the outputs typically settle in less than 10 ns.

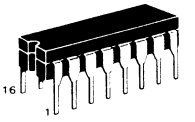
- FAST! Settling Time – 10 ns Typ
- 8-Bit Accuracy (±0.19%)
- Inputs MECL 10,000 Compatible
- Complementary Current Outputs
- Output Compliance: -1.3 V to +2.5 V
- Standard: -5.2 V Supply
- Standard 16 Pin Ceramic Package
- Low Dissipation – Typically Less Than 500 mW
- Low Cost

TYPICAL MC10318 TO MC10800 PROCESSOR INTERFACE



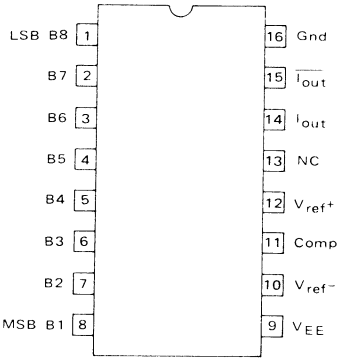
HIGH SPEED 8-BIT DIGITAL-TO-ANALOG CONVERTER

SILICON MONOLITHIC INTEGRATED CIRCUIT



L SUFFIX
CERAMIC PACKAGE
CASE 620

PIN CONNECTIONS



This is advance information and specifications are subject to change without notice.

ADI-510

MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{EE}	−6.0 to +0.5	Vdc
Digital Input Voltage	V_I	0 to V_{EE}	Vdc
Applied Output Voltage	V_O	+5.0	Vdc
Reference Current	$I_{ref}(12)$	5.0	mA
Reference Amplifier Input Range	V_{ref}	+0.5 to V_{EE}	Vdc
Reference Amplifier Differential Inputs	$V_{ref}(D)$	±5.0	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C
Junction Temperature Ceramic Package	T_J	+175	°C

CHARACTERISTICS

These specifications apply for V_{EE} = −5.2 V, I_{FS} = 51 mA, T_A = 0°C to +70°C after thermal equilibrium is reached.

	TEST VOLTAGE VALUES (Note 1)				
	Volts				
@ Test Temperature	$V_{IH}max$	$V_{IL}min$	$V_{IHA}min$	$V_{ILA}max$	V_{EE}
0°C	−0.845	−1.868	−1.151	−1.516	−5.2
25°C	−0.810	−1.850	−1.105	−1.505	−5.2
70°C	−0.727	−1.830	−1.052	−1.480	−5.2

Characteristics	Symbol	Min	Typ	Max	Unit
Power Supply Voltage Range	V_{EE}	−5.46	−5.2	−4.94	V
Power Supply Current (Pins 1 thru 8 Open, I_{FS} = 51 mA)	I_{EE}	—	90	130	mA
Monotonicity	—	8.0	8.0	—	Bits
Nonlinearity	—	—	—	±0.19	% FS
Settling Time to 1/2 LSB (All Bits Switched On or Off, T_A = 25°C, Note 3)	t_s	—	10	—	ns
Full Scale Output Temperature Drift	TCI_{FS}	—	±50	±150	ppm/°C
Full Scale Current — Figure 1 (R3, R4 = 3.300 kΩ, V_{ref} = 10.560 V, Note 2)	I_{FS}	46.000	51	56.000	mA
Zero Scale Current (Note 2)	I_{ZS}	—	5.0	50	μA
Full Scale Symmetry ($I_{FS15} - I_{FS14}$, Note 2)	I_{FSS}	—	15	100	μA
Output Voltage Compliance (Full Scale Current Change < 1/2 LSB, Note 2)	V_{OC}	−1.3	—	2.5	V
Power Supply Sensitivity (of Full Scale Current) (V_{EE} = −4.94 V to −5.46 V)	$PSSI_{FS}$	—	±0.002	±0.02	%/%
Reference Bias Current, Pin 10 (I_{ref} = 3.2 mA)	I_{10}	—	6.0	15	μA
Propagation Delay 50% to 50% (All Bits Switched Low to High, High to Low)	tP	—	3.0	—	ns

NOTES: 1. Logic input levels are compatible with MECL 10,000 logic series.
2. Output characteristics apply to both pins 14 and 15, I_{out} and $\overline{I_{out}}$.
3. See comments on construction and evaluation techniques in Figure 2 and text.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

FIGURE 1 – FULL SCALE CURRENT TEST CIRCUIT

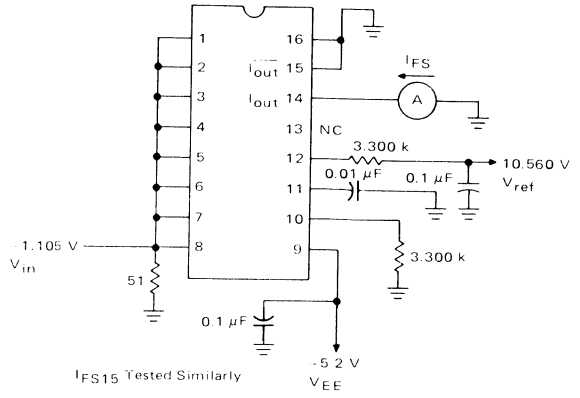
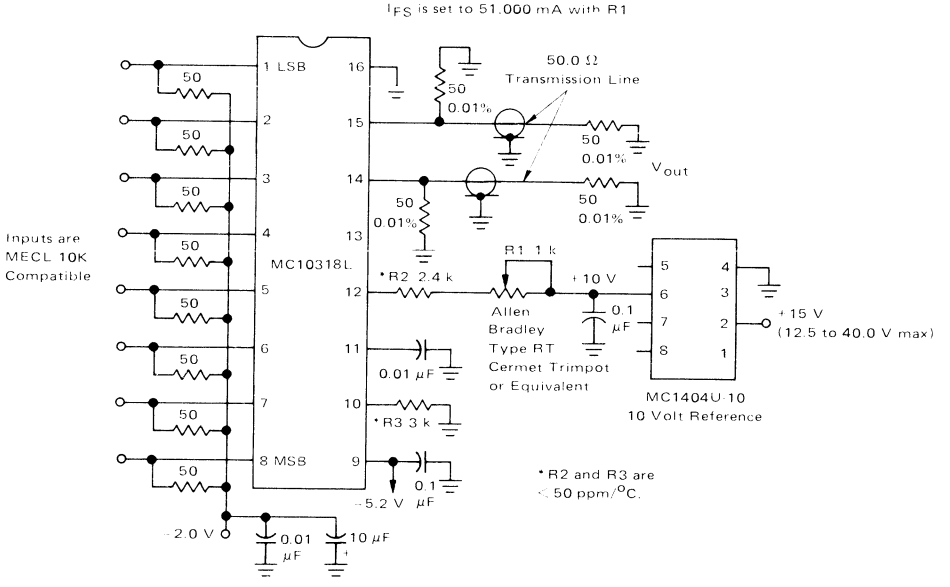
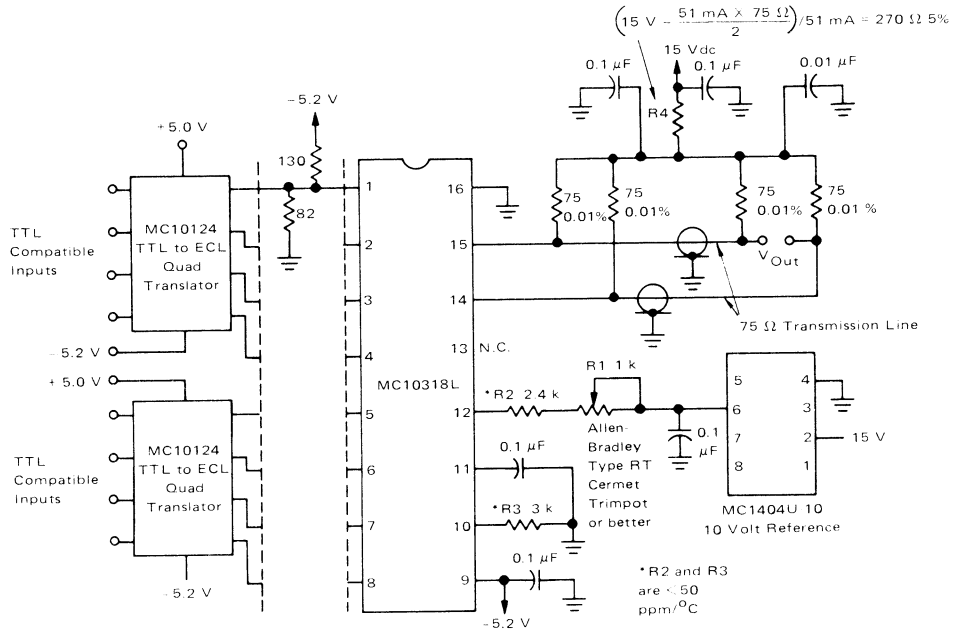


FIGURE 2 – TYPICAL CONNECTIONS FOR 50 Ω TRANSMISSION LINE



NOTE: Line impedances and termination impedance must be homogeneous 50.00 Ω. Any deviation will cause reflections which will seriously affect settling time. Optimum performance cannot be realized with sockets. Good 1.0 GHz microstripline techniques must be used.

FIGURE 3 – TYPICAL CONNECTIONS FOR 75 Ω TRANSMISSION LINE AND TTL-COMPATIBLE INPUTS



NOTE: See caution on line and termination impedance in Figure 2 and text.

APPLICATION INFORMATION

Functional Test Circuit Construction

Test circuits used to evaluate this device or circuit designs used in actual practical situations must employ good 1.0 GHz RF microstripline practices if optimum performance is to be achieved from this device. Both line and termination impedances must be matched to within ±0.19% to minimize reflections which will appear as increased settling time. The use of sockets for initial evaluation is not recommended if specified settling time is to be obtained.

Applications information can be obtained by contacting:

Application Engineering
(602) 244-3021

If desired, test circuit artwork and board specifications will be supplied by contacting:

Linear Interface Marketing
(602) 962-2294

Successive Approximation A/D Converter

The circuit shown in Figure 4 uses the MC10318 in a successive approximation analog-to-digital converter. The circuit as shown will operate at a clock frequency above 30 MHz if proper attention is given to layout.

The full-scale voltage (V_{FS}) for the circuit as shown is 10.20 V. This full-scale voltage may be changed by changing the 200 Ω resistor to a value given by:

$$R = \frac{V_{FS}}{I_{FS}} = \frac{V_{FS}}{51\ mA}$$

However, at low values of V_{FS} the resolution of the comparator must be considered to maintain a ± 1/2 LSB accuracy.

FIGURE 4 – SUCCESSIVE APPROXIMATION A/D CONVERTER USING MC10318

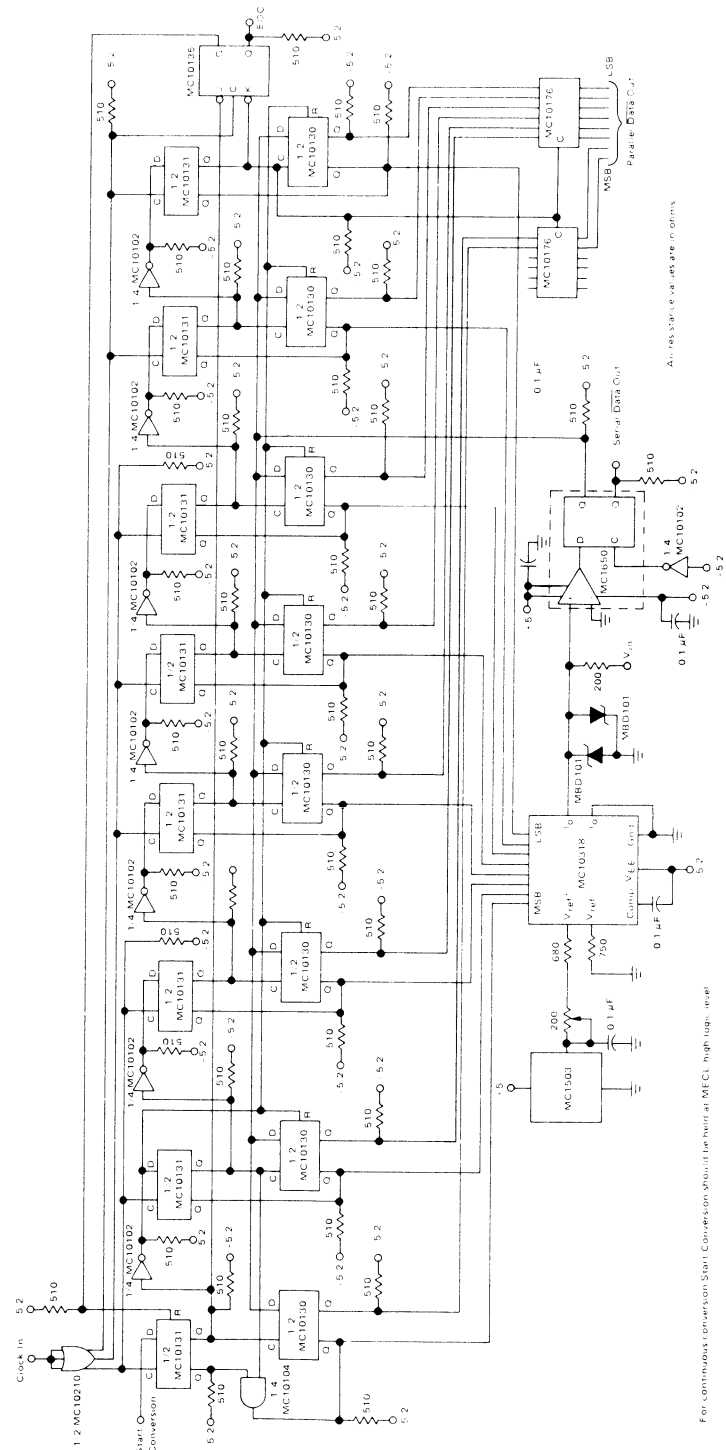
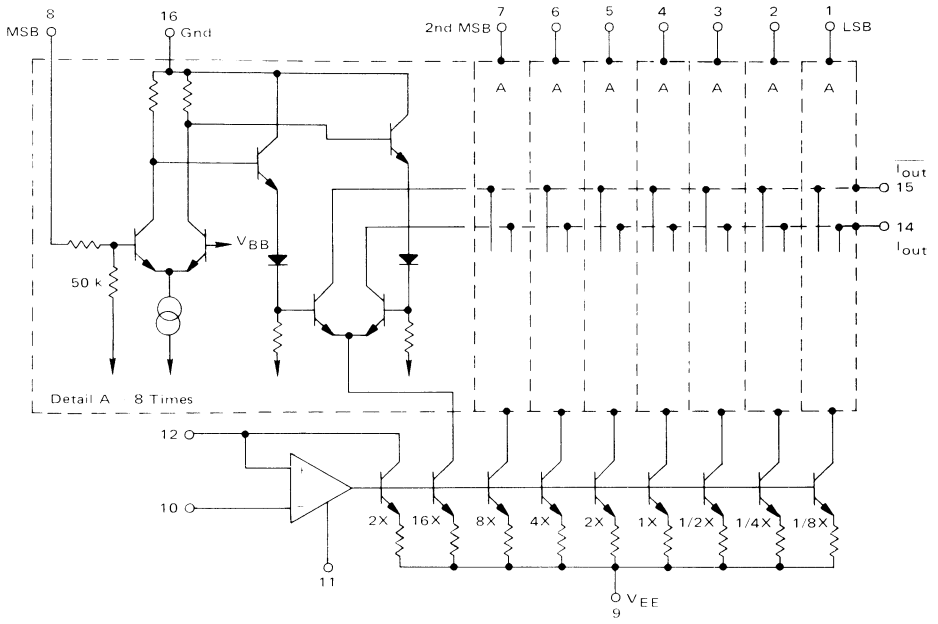
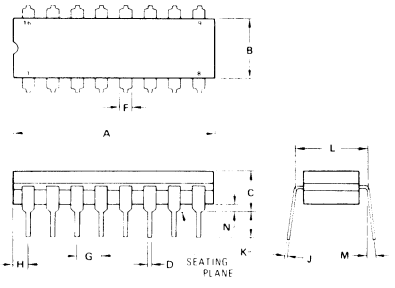


FIGURE 5 – MC10318 EQUIVALENT CIRCUIT



OUTLINE DIMENSIONS



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.18	4.07	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040

NOTES
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2. PKG INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

CASE 620-02

PHASE-LOCKED LOOP COMPONENTS

6

COMPONENTS FOR PHASE-LOCKED LOOP APPLICATIONS

Motorola offers the designer a choice of specially designed integrated circuits for performing phase-locked loop functions: phase detection, frequency division, filtering, and voltage-controlled signal generation. New MECL functions for phase-locked loop applications are now being characterized. In addition, supplementary circuits in TTL, CMOS, and linear technologies are available.

For convenience, the MECL functions characterized by data sheets included in this book are indicated by ●. For detailed specifications of all other devices, please request a separate data sheet from your Motorola sales representative or authorized distributor.

The following functions are given in order of decreasing frequency within each category.

	Function	Family	Frequency MHz typ	Power Dissipation mW typ/pkg	Type -55 to +125°C	Type 0 to +75°C	Case ①
	COMBINATION FUNCTIONS						
	Digital Mixer Translator	MECL	250	470	–	MC12000	632, 646
	Analog Loop	MECL	50	170	MC12530	MC12030	620, 648
	Frequency Synthesizer	CMOS	10.24	3mA*	–	MC145104§	648
	Frequency Synthesizer	CMOS	10.24	3mA*	–	MC145106§	707
	Frequency Synthesizer	CMOS	10.24	3mA*	–	MC145107§	648
	Frequency Synthesizer	CMOS	10.24	3mA*	–	MC145109§	648
	Frequency Synthesizer	CMOS	10.24	3mA*	–	MC145112§	707
	Phase Comparator/Programmable Counters	CMOS	10	10 nA†	MC14568B‡	MC14568B‡	620, 648
	Phase Comparators/VCO	CMOS	1.4	10 nA†	MC14046B‡	MC14046B‡	620, 648
	Phase-Locked Loop	LINEAR	0.5	825	–	LM565C	646
	OSCILLATORS						
	Crystal Oscillator	MECL	2.0 to 20	210	MC12561	MC12061	620, 648
	Crystal Oscillator	MECL	0.1 to 2.0	175	MC12560	MC12060	620, 648
●	Voltage-Controlled Oscillator	MECL	225	150	MC1648M	MC1648#	607, 632, 646
●	Voltage-Controlled Multivibrator	MECL	150	150	–	MC1658#	620, 648, 650
	Dual Voltage-Controlled Multivibrator	MTTL	30	150	MC4324	MC4024	607, 632, 646
	PHASE DETECTORS						
	Digital Phase-Frequency Detector	MECL	70	520	MC12540	MC12040	607, 632, 646
	Phase-Frequency Detector	MTTL	8.0	85	MC4344	MC4044	607, 632, 646
	Analog Analog Mixer – Double Balanced	MECL	100	60	MC12502	MC12002#	632, 646
	Modulator/Demodulator	LINEAR	10	575	MC1596	MC1496	603, 632, 646
	CONTROL FUNCTIONS						
	Counter Control Logic	MECL	25	150	MC12514	MC12014	620, 648
	Offset Control	MECL	–	35	MC12520	MC12020#	632, 646
	Offset Programmer	MECL	–	35	MC12521	MC12021#	620, 648
	PRESCALERS						
●	÷4 Counter	MECL	1100	322	–	MC1697	626
●	÷4 Counter	MECL	1100	322	–	MC1699#	620, 650
	Two-Modulus Prescaler (÷5/÷6)	MECL	500	350	–	MC12009	620, 648
	Two-Modulus Prescaler (÷8/÷9)	MECL	550	350	–	MC12011	620, 648
	Two-Modulus Prescaler (÷10/11)	MECL	600	350	MC12513	MC12013#	620, 648, 650
	UHF Type D Prescaler (÷2)	MECL	500		–	MC1690#	620, 650
	Two-Modulus Prescaler (÷2, ÷5/6, ÷10/11, ÷10/12)	MECL	200	500	–	MC12012	620, 648
	Dual Type D	LS TTL	45	20	SN54LS74	SN74LS74	717, 632, 646

①Plastic package available for commercial-temperature devices only.

*Operating Supply Current @ 10.24 MHz

†Quiescent Current @ V_{DD} = 10 V

‡For CMOS devices, add suffix for temperature range: A for −55 to +125°C, C for −40 to +85°C, followed by package suffix.

§T_A = −40 to +85°C

#T_A = −30 to +85°C

PLL FUNCTIONS (continued)

(In order of decreasing frequency within each category.)

Function	Family	Frequency MHz typ	Power Dissipation mW typ/pkg	Type		Case ①
				-55 to +125°C	0 to +75°C	
COUNTERS						
Binary	MECL	325	750	–	MC1654#	620
Bi-Quinary (÷2, ÷5, ÷10)	MECL	325	750	–	MC1678#	620
Universal Hexadecimal (÷0-15)	MECL	150	625	MC10536	MC10136#	620, 648, 650
Universal Decade	MECL	150	625	MC10537	MC10137#	620, 648, 650
Bi-Quinary	MECL	150	370	MC10538	MC10138#	620, 648, 650
Binary	MECL	150	370	MC10578	MC10178#	620, 648, 650
Presettable Binary (÷2, ÷8)	LS TTL	60	60	SN54LS197	SN74LS197	717, 632, 646
Presettable Decade (÷2, ÷5)	LS TTL	60	60	SN54LS196	SN74LS196	717, 632, 646
Presettable Up/Down Decade	LS TTL	40	95	SN54LS192	SN74LS192	620, 648, 650
Presettable Up/Down Binary	LS TTL	40	95	SN54LS193	SN74LS193	620, 648, 650
Presettable Decade	LS TTL	35	95	SN54LS160	SN74LS160	620, 648, 650
Presettable Binary	LS TTL	35	95	SN54LS161	SN74LS161	620, 648, 650
Presettable Decade	LS TTL	35	95	SN54LS162	SN74LS162	620, 648, 650
Presettable Binary	LS TTL	35	95	SN54LS163	SN74LS163	620, 648, 650
Presettable Up/Down Decade	LS TTL	35	95	SN54LS190	SN74LS190	620, 648, 650
Presettable Up/Down Binary	LS TTL	35	95	SN54LS191	SN74LS191	620, 648, 650
Decade (÷2, ÷5)	LS TTL	32**	45	SN54LS90	SN74LS90	717, 632, 646
Binary (÷2, ÷8)	LS TTL	32**	45	SN54LS93	SN74LS93	717, 632, 646
Universal (÷2-12 except 7 and 11)	MTTL	30	200	MC4323	MC4023	607, 632, 646
Decade (÷2, ÷5, ÷10)	MTTL	20	160	MC5490A	MC7490A	607, 632, 646
Decade (÷10)	CMOS	12 ##	10 nA †	MC14017B ‡	MC14017B ‡	620, 648
Programmable ÷N Decade (÷0-9)	MTTL	10	250	MC4316	MC4016	620, 648, 650
Two Programmable ÷N (÷0-1, ÷0-4)	MTTL	10	250	MC4317	MC4017	620, 648, 650
Programmable ÷N Hexadecimal (÷0-15)	MTTL	10	250	MC4318	MC4018	620, 648, 650
Two Programmable ÷N (÷0-3, ÷0-3)	MTTL	10	250	MC4319	MC4019	620, 648, 650
Binary ($\div 2^{14}$)	CMOS	9 ##	10 nA †	MC14020B ‡	MC14020B ‡	620, 648
Binary ($\div 2^{12}$)	CMOS	9 ##	10 nA †	MC14040B ‡	MC14040B ‡	620, 648
Dual Programmable BCD/Binary Down	CMOS	8 ##	10 nA †	MC14569B ‡	MC14569B ‡	620, 648
BCD Up/Down	CMOS	6 ##	10 nA †	MC14510B ‡	MC14510B ‡	620, 648
Binary Up/Down	CMOS	6 ##	10 nA †	MC14516B ‡	MC14516B ‡	620, 648
Dual BCD Up	CMOS	6 ##	10 nA †	MC14518B ‡	MC14518B ‡	620, 648
Dual Binary Up	CMOS	6 ##	10 nA †	MC14520B ‡	MC14520B ‡	620, 648
Programmable ÷N BCD (÷0-9)	CMOS	5 ##	10 nA †	MC14522B ‡	MC14522B ‡	620, 648
Programmable ÷ Binary (÷0-15)	CMOS	5 ##	10 nA †	MC14526B ‡	MC14526B ‡	620, 648

①Plastic package available for commercial-temperature devices only.

T_A = -30 to +85°C

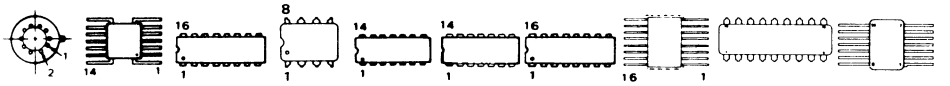
** When using $\overline{CP}_0$

@ V_{DD} = 10 V

† Quiescent Current @ V_{DD} = 10 V

‡ For CMOS devices, add suffix for temperature range: A for -55 to +125°C, C for -40 to +85°C, followed by package suffix

Package Styles



CASE		603	607	620	626	632	646	648	650	707	717
MATERIAL		Metal	Ceramic	Ceramic	Plastic	Ceramic	Plastic	Plastic	Ceramic	Plastic	Ceramic
SUFFIX after type number	LS TTL	–	–	J	–	J	N	N	W	–	W
	Others	G	F	L	P	L	P	P	F	P	F

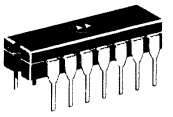
6

MC12000

DIGITAL MIXER/TRANSLATOR
(D Flip-Flop w/Translator)

The MC12000 is intended for use as a digital mixer in phase-locked loop frequency synthesizers and other applications where a MECL "D" flip-flop with translators is required. Toggle frequency is typically 250 MHz. MTTL to MECL and MECL to MTTL translators are provided to facilitate interfacing with MECL or MTTL circuits.

The MC12000 is designed to operate from a single power supply of either +5.0 Vdc or -5.2 Vdc.



CERAMIC PACKAGE
CASE 632

Pin Assignment

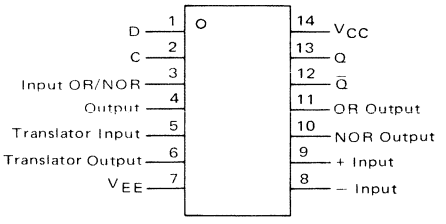
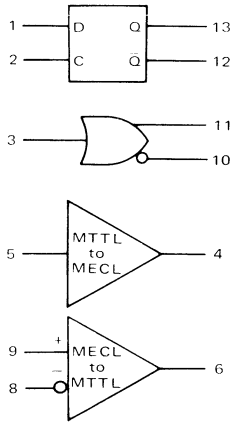


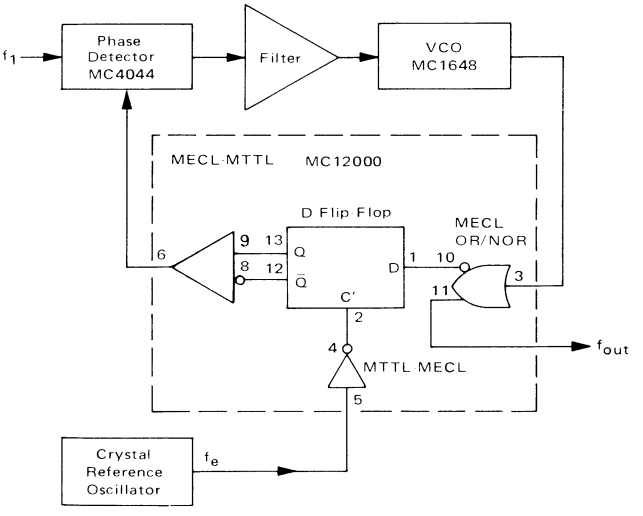
FIGURE 1 – LOGIC DIAGRAM



V_{CC} = Pin 14
V_{EE} = Pin 7

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

FIGURE 2 – TYPICAL DIGITAL MIXER

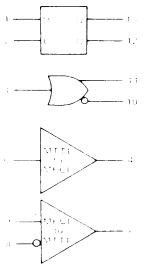


Note: All MECL outputs have 510-ohm internal pulldown resistors.

6

ELECTRICAL CHARACTERISTICS

Supply Voltage = +5.0 V



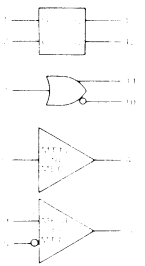
@ Test Temperature	TEST VOLTAGE/CURRENT VALUES													
	Volts											mA		
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHA}	V_R	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}
0°C	+4.160	+3.130	+3.855	+3.510	+0.5	+2.4	+5.0	+4.5	+2.0	+0.8	+5.0	-2.5	16	-1.6
25°C	+4.190	+3.150	+3.895	+3.525	+0.5	+2.4	+5.0	+4.5	+2.0	+0.8	+5.0	-2.5	16	-1.6
75°C	+4.280	+3.170	+3.955	+3.550	+0.5	+2.4	+5.0	+4.5	+2.0	+0.8	+5.0	-2.5	16	-1.6

Characteristic	Symbol	Pin Under Test	MC12000 0°C Min	MC12000 0°C Max	MC12000 +25°C Min	MC12000 +25°C Typ	MC12000 +25°C Max	MC12000 +75°C Min	MC12000 +75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}	(V_{EE}) Gnd
Power Supply Drain Current	I_E	7				85				mAdc											14				7
Input Current	I_{INH1}	1					200			µAdc	1	7									14				7
		2					200				2	1													
		3					200				3														
	I_{INH2}	5		4.0			40		40								5								
	I_{INH3}	8			3.8		6.5			mAdc	9	8													
		9			3.8		6.5				9	8													
	I_{INL1} (Leakage Current)	1					2.0			µAdc											14				1,7
		2					2.0																		2,7
		3					2.0																		3,7
	I_{INL2}	5		-1.6			-1.6		-1.6	mAdc					5										7
	I_{INL3}	8			3.8		6.5				8	9													
		9			2.0		4.0				8	9													
Logic "1" Output Voltage	V_{OH1}	4	4.000	4.160	4.040		4.190	4.100	4.280	Vdc		3				5					14	4			7
		10																				10			
		11									3											11			
		12†										1										12			
		13†									1											13			
	V_{OH2}	6	2.400		2.400			2.400		Vdc	9	8									14			6	7
Logic "0" Output Voltage	V_{OL1}	4	3.130	3.370	3.150		3.380	3.170	3.410	Vdc					5						14	4			7
		10									3											10			
		11										3										11			
		12†									1											12			
		13†										1										13			
	V_{OL2}	6		0.500			0.500		0.500	Vdc	8	9									14		6		7
Logic "1" Threshold Voltage	V_{OHA}	4	3.980		4.020			4.080		Vdc				3					5		14	4			7
		10											3									10			
		11												1								11			
		12†											1									12			
		13†																				13			
Logic "0" Threshold Voltage	V_{OLA}	4		3.390			3.400		3.430	Vdc										5	14	4			7
		10											3									10			
		11												3								11			
		12†											1									12			
		13†												1								13			
Short Circuit Current	I_{SC}	6	-20	-65	-20		-65	-20	-65	mAdc	9	8									-4				6,7

†Output Level to be measured after a clock pulse has been applied to the C input (pin 2). V_{IHmax} / V_{ILmin}

ELECTRICAL CHARACTERISTICS

Supply Voltage = -5.2 V



@ Test Temperature	TEST VOLTAGE/CURRENT VALUES													
	Volts											mA		
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}
0°C	-0.840	-1.870	-1.145	-1.490	-4.7	-2.8	+0.0	-0.7	-3.2	-4.4	-5.2	-2.5	16	-1.6
25°C	-0.810	-1.850	-1.105	-1.475	-4.7	-2.8	+0.0	-0.7	-3.2	-4.4	-5.2	-2.5	16	-1.6
75°C	-0.720	-1.830	-1.045	1.450	-4.7	-2.8	+0.0	-0.7	-3.2	-4.4	-5.2	-2.5	16	-1.6

Characteristic	Symbol	Pin Under Test	MC12000 0°C Min	MC12000 0°C Max	MC12000 25°C Min	MC12000 25°C Typ	MC12000 25°C Max	MC12000 +75°C Min	MC12000 +75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OL}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	7				90				mAdc											7				14
Input Current	I_{INH1}	1					200			µAdc	1	2									7				14
		2					200				2	1													
		3					200				3														
	I_{INH2}	5		40			40		40								5								
	I_{INH3}	8			3.8		6.5			mAdc	9	8													
		9			3.8		6.5				9	8													
	I_{INL1} (Leakage Current†)	1					2.0			µAdc											1.7				14
		2					2.0														2.7				
		3					2.0														3.7				
	I_{INL2}	5		-1.6			-1.6		-1.6	mAdc					5						7				
	I_{INL3}	8			3.8		6.5				8	9													
		9			2.0		4.0				8	9													
Logic "1" Output Voltage	V_{OH1}	4	-1.000	-0.840	-0.960		-0.810	-0.900	-0.720	Vdc						5					7	4			14
		10										3										10			
		11									3											11			
		12†										1										12			
		13†									1											13			
	V_{OH2}	6	-2.800		-2.800			-2.800		Vdc	9	8									7			6	14
Logic "0" Output Voltage	V_{OL1}	4	-1.870	-1.635	-1.850		-1.620	-1.830	-1.595	Vdc					5						7	4			14
		10									3											10			
		11										3										11			
		12†									1											12			
		13†										1										13			
	V_{OL2}	6		-4.700			-4.700		-4.700	Vdc	8	9									7		6		14
Logic "1" Threshold Voltage	V_{OHA}	4	-1.020		-0.980			-0.920		Vdc						3			5		7	4			14
		10																				10			
		11											3									11			
		12†														1						12			
		13†											1									13			
Logic "0" Threshold Voltage	V_{OLA}	4		-1.615			-1.600		-1.575	Vdc										5	7	4			14
		10											3									10			
		11												3								11			
		12†											1									12			
		13†												1								13			
Short Circuit Current	I_{SC}	6	-20	-65	-20		-65	-20	-65	mAdc	9	8									6.7				14

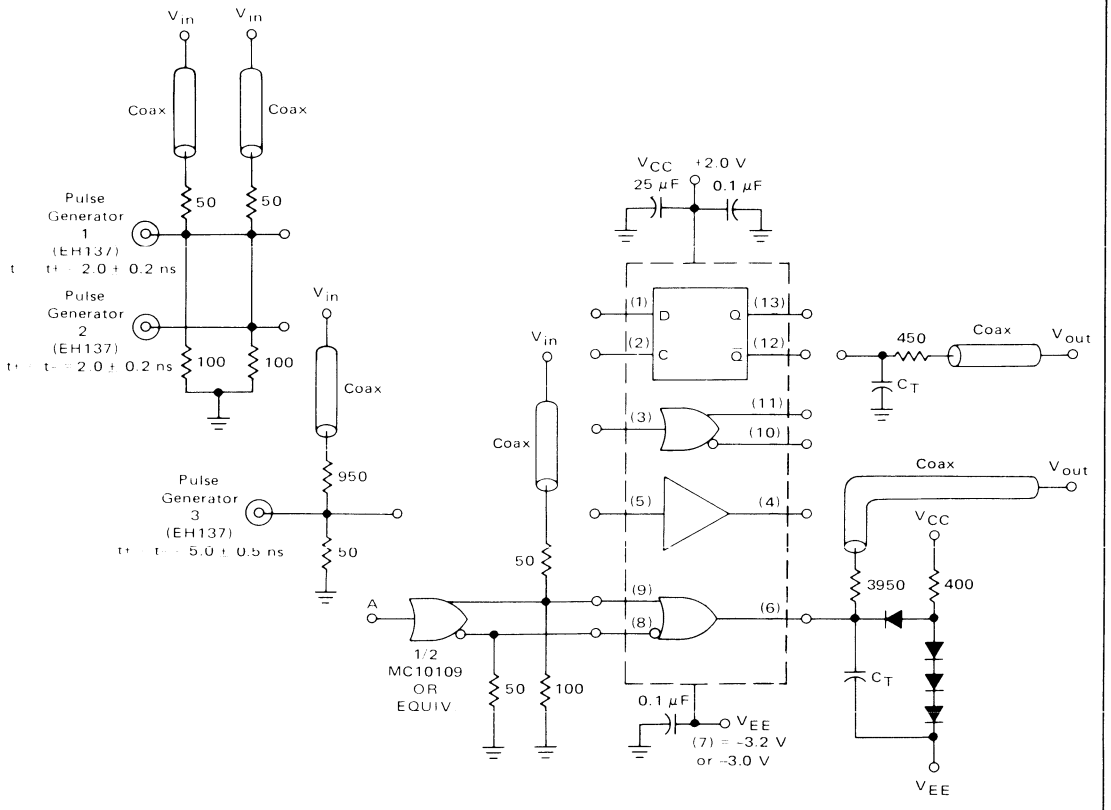
†Output Level to be measured after a clock pulse has been applied to the C input (pin 2). V_{IHmax} / V_{ILmin}

AC ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC12000 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse Gen. 1	Pulse Gen. 2	Pulse Gen. 3	Pulse Out	V_{EE} -3.2 V or -3.0 V	V_{CC} +2.0 V
Propagation Delay (See Figure 4)	t_{2+13+}	2,13	–	–	1.5	2.4	4.0	–	–	ns	2	1	–	13	7	14
	t_{2+13-}	2,13	–	–	1.5	2.4	4.0	–	–	ns	2	1	–	13	7	14
	t_{2+12+}	2,12	–	–	1.5	2.4	4.0	–	–	ns	2	1	–	12	7	14
	t_{2+12-}	2,12	–	–	1.5	2.4	4.0	–	–	ns	2	1	–	12	7	14
	t_{3+11+}	3,11	–	–	1.0	1.5	3.0	–	–	ns	3	–	–	11	7	14
	t_{3-11-}	3,11	–	–	1.0	1.5	3.0	–	–	ns	3	–	–	11	7	14
	t_{3+10-}	3,10	–	–	1.0	1.5	3.0	–	–	ns	3	–	–	10	7	14
	t_{3-10+}	3,10	–	–	1.0	1.5	3.0	–	–	ns	3	–	–	10	7	14
	t_{5+4+}	5,4	–	–	2.0	3	5.0	–	–	ns	–	–	5	4	7	14
	t_{5-4-}	5,4	–	–	1.0	1.5	3.0	–	–	ns	–	–	5	4	7	14
	t_{9+6+}	9,6	–	–	4.0	8.0	12.0	–	–	ns	A	–	–	6	7	14
	t_{9-6-}	9,6	–	–	3.0	5.0	10.0	–	–	ns	A	–	–	6	7	14
Output Rise Time (See Figure 4)	t_{13+}	13	–	–	–	2.8	–	–	–	ns	2	1	–	13	7	14
	t_{12+}	12	–	–	–	2.8	–	–	–	ns	2	1	–	12	7	14
	t_{11+}	11	–	–	–	2.0	–	–	–	ns	3	–	–	11	7	14
	t_{10+}	10	–	–	–	2.0	–	–	–	ns	3	–	–	10	7	14
	t_{4+}	4	–	–	–	2.4	–	–	–	ns	–	–	5	4	7	14
Output Fall Time (See Figure 4)	t_{13-}	13	–	–	–	2.8	–	–	–	ns	2	1	–	13	7	14
	t_{12-}	12	–	–	–	2.8	–	–	–	ns	2	1	–	12	7	14
	t_{11-}	11	–	–	–	2.0	–	–	–	ns	3	–	–	11	7	14
	t_{10-}	10	–	–	–	2.0	–	–	–	ns	3	–	–	10	7	14
	t_{4-}	4	–	–	–	2.4	–	–	–	ns	–	–	5	4	7	14
Setup Time (See Figure 5)	$t_{setup"1"}$	13	–	–	–	0.2	–	–	–	ns	2	1	–	–	7	14
	$t_{setup"0"}$	13	–	–	–	0.7	–	–	–	ns	2	1	–	–	7	14
Hold Time (See Figure 5)	$t_{hold"1"}$	13	–	–	–	0.0	–	–	–	ns	2	1	–	–	7	14
	$t_{hold"0"}$	13	–	–	–	1.0	–	–	–	ns	2	1	–	–	7	14
Toggle Frequency (See Figure 6)	f_{tog}	13	–	–	–	250	–	–	–	MHz	–	–	–	–	7	14

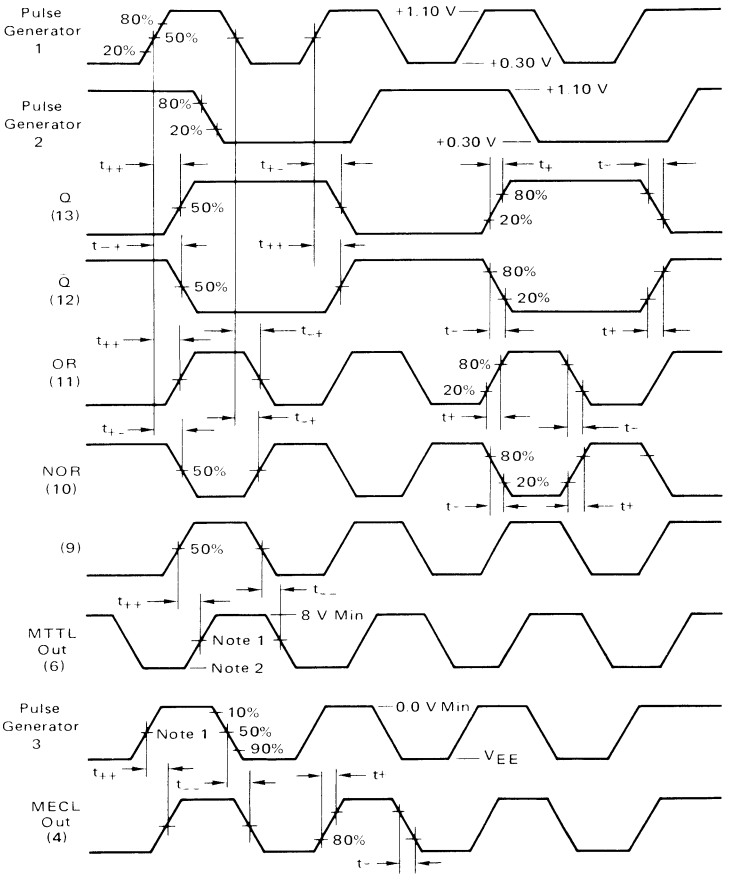
FIGURE 3 – SWITCHING TIME TEST CIRCUIT

All input and output cables to the scope are equal lengths of 50 ohm coaxial cable. All unused cables must be terminated with a 50 ohm resistor ± 1%.



C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

FIGURE 4 – AC TEST VOLTAGE WAVEFORMS



NOTES:
1. V_{EE} + 1.5 V
2. V_{EE} + 0.5 V max

FIGURE 5 – SETUP AND HOLD TIME WAVEFORMS (See Figure 3)

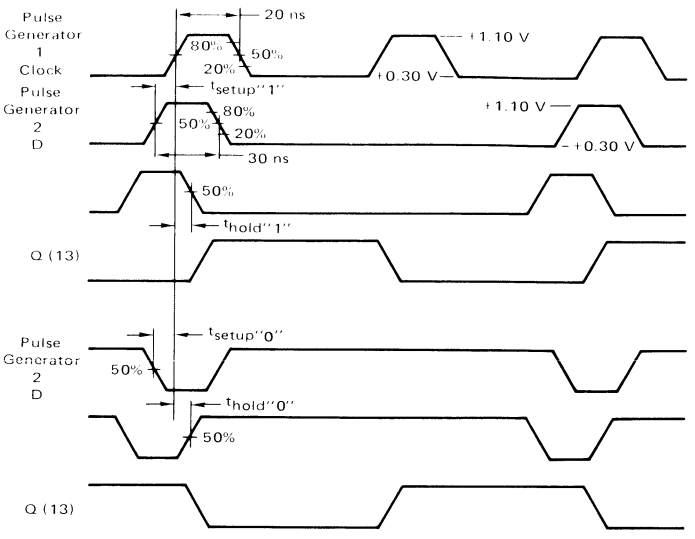
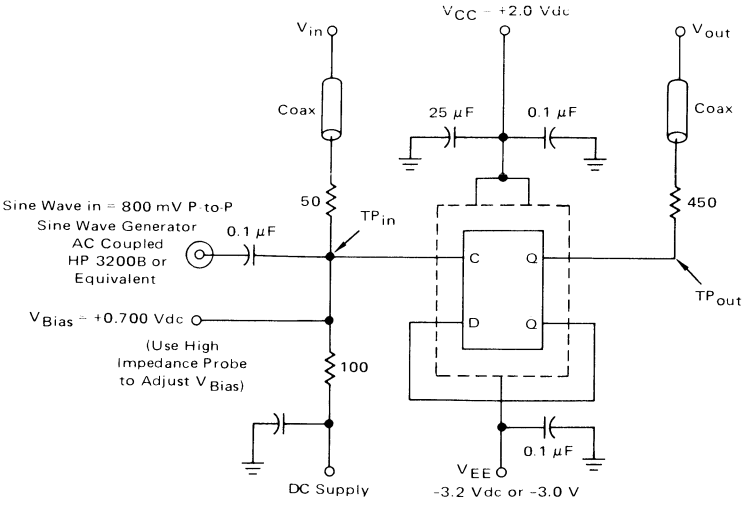


FIGURE 6 – TOGGLE FREQUENCY TEST CIRCUIT



The maximum Toggle Frequency of MC12000 has been exceeded when either:

1. The output Peak-to-Peak voltage swing falls below 600 mV

   or

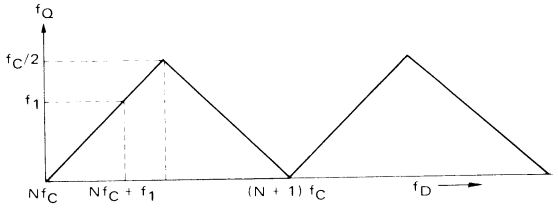
2. The devices cease to Toggle (divide by 2).

MC12000 DIGITAL MIXER

This device is a digital mixer designed to operate with logic levels at its input and output ports. In operation it is an MECL type "D" flip-flop with level translators to and from MTTL to accomodate most interfacing demands. Output frequency (f_Q) as a function of "D" and clock inputs is shown in Figure 7. It can be seen that either direct or harmonic mixing may be employed, that is, f_Q may be either the difference between f_D and f_C or the difference between f_D and the Nth harmonic of f_C.

One particular advantage of mixing in phase locked loops (PLL) is that lower frequencies may be generated for use in portions of the circuit where digital processing is done (with divide-by-P network and/or phase detector). Lower frequency operation often reduces overall system cost since a less expensive logic form may be utilized. However use of the mixing technique is not a panacea for all VHF applications and the design of such synthesizer systems must be approached with care.

FIGURE 7



Use of the MC12000 in a non-harmonic PLL is straightforward (Figure 8). Output frequency is the sum of both input quantities ($f_1 + f_C$) as long as f_1 is less than $f_C/2$ (See Figure 7), since f_Q can go no higher than that. Unless VCO output range is restricted somewhat there is a chance also that the loop may operate at the second harmonic of f_C. This problem is minimal in the loop of Figure 8, however, since the output frequency would have to vary more than 2:1.

Mixing is used because the digital phase detector has an upper frequency limit of about 10 MHz and many loops require direct locks at 20 MHz or more. Direct down-mixing does not change any loop characteristics except the sampling rate which restricts loop natural frequency to about $f_C/10$ in practical circuits. Although output frequency may be changed by varying either f_1 or f_C, the clock input is usually crystal controlled since it is of the same magnitude as f_D and more difficult to stabilize.

FIGURE 8

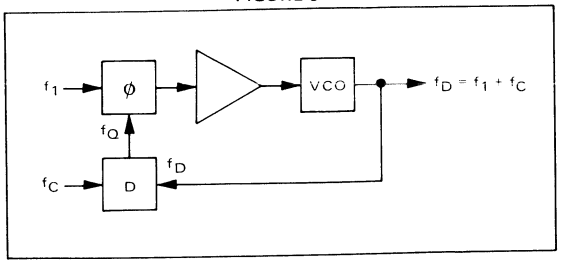
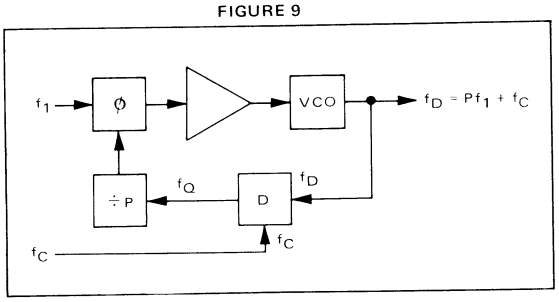


FIGURE 9



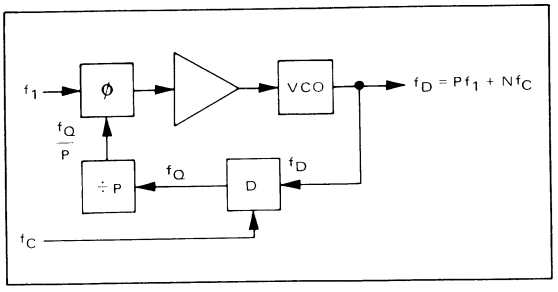
Combining a standard synthesis configuration with the mixer yields a circuit capable of high frequency operation at low cost (Figure 9), if the output frequency range is relatively small ($P_{max} - P_{min}$) $f_1 < f_C/2$. In fact the choice of harmonic or non-harmonic mixing is largely based on the availability of a suitable crystal or other reference source for f_C versus the needed frequency coverage. Considering all the restrictions on f_C, its value (and the maximum harmonic number N) are dictated by the following expressions:

$$N < \frac{f_{D(min)} - f_1}{2\,\Delta f_D} \qquad (1)$$

$$Nf_C = f_{D(min)} - f_1 \qquad (2)$$

where Δf_D = change in output frequency.

FIGURE 10



Using Equations (1) and (2) above the minimum value of f_C may be found for the circuit of Figure 10 and still get adequate frequency coverage. In this minimum configuration all necessary output frequencies may be generated by programming the "P" count string. But the divide number might bear no obvious relation to the output frequency such as often happens with non-mixing synthesizers.

DESIGN EXAMPLES

Example #1

Output Frequency: 48-54 MHz
Frequency Increments: 10 kHz
Using Equations (1) and (2), a minimum frequency (f_C) version can be designed:

$$f_1 = \text{increment} = 10\ \text{kHz}$$

$$N < \frac{48\ \text{MHz} - 10\ \text{kHz}}{2\ (54\text{-}48)\ \text{MHz}}$$

$$N < 4$$

Let N = 3

$$Nf_C = 47.99\ \text{MHz}$$

$$f_C = \frac{Nf_C}{N} = \frac{47.99}{3} = 15.99666\ \text{MHz}$$

$$f_C = 15.996666\ \text{MHz}$$

$$P_{min} = 1$$

$$P_{max} = \frac{\Delta f_D}{10\ \text{kHz}} + P_{min} \qquad (3)$$

$$P_{max} = \frac{6\ \text{MHz}}{10\ \text{kHz}} + P_{min}$$

$$P_{max} = 601$$

$$f_{O(max)} = P_{max}\ f_1$$
$$= 6.01\ \text{MHz} \qquad (4)$$

Equation (4) above puts the divider string (divide-by-P) into a medium frequency situation where devices such as the MC4016/4316 may be utilized. Note that the divider number now indicates the channel selected rather than output frequency. That is, at f_D = 48.000 MHz, P = 1; at f_D = 54.000 MHz, P = 601.

If "proper" divide-by-P readings are desired for direct frequency readout a slight circuit modification is necessary. To enable a division at 48.000 MHz the first divide-by-P must be 100 rather than 1, and P_{max} would then be 700 to cover all 6 MHz. Recalculating $f_{O(max)}$ from Equation 4 we still find that the 7 MHz maximum value allows use of the same components. The next question concerns the allowable range of f_O in relation to f_C ($f_O < f_C/2$). Since f_C is nearly 16 MHz, the range of f_O can be contained. A cosmetic change to the most significant digit switch completes the design. Instead of reading 1 through 7 it must be modified to display 48 through 54.

Example #2

Output Frequency: 144-148 MHz
Frequency Increments: 10 kHz

$$f_1 = \text{increment} = 10\ \text{kHz}$$

$$N < \frac{144.00 - 0.01}{2\ (4)}$$

$$N < 18$$

Let N = 17

$$Nf_C = 144.00 - 0.01\ \text{MHz}$$
$$= 143.99$$

$$f_C = \frac{Nf_C}{N} = 8.470\ \text{MHz}$$

$$P_{min} = 1$$

$$P_{max} = \frac{4\ \text{MHz}}{10\ \text{kHz}} + 1$$
$$= 401$$

$$f_{O(max)} = P_{max}\ f_1 = 4.01\ \text{MHz}$$

Maximum frequency seen by the divide-by-P chain is still well within the MC4016 rating.

When converting this synthesizer to one that needs frequency directly, a "1" is again added to the most significant digit (MSD). This results in a P_{min} of 100 to P_{max} of 500. In this example, however, $f_{O(max)}$ is 5 MHz which easily exceeds $f_C/2$. To alleviate this difficulty, the "N" factor must be decreased in order to raise f_C to at least 10 MHz.

$$N < \frac{f_{D(min)} - f_1}{f_C}$$

Let f_C = 10 MHz

$$N < \sim 14.4$$

Let N = 14

Nf_C = 143.99 (from above)

$$f_C = \frac{Nf_C}{N} = \frac{143.99}{14}$$

$$f_C = 10.28540\ \text{MHz} \qquad (5)$$

VCO RANGE RESTRICTIONS

As in all harmonically locked PLL's, it is possible for the loop to lock on the wrong harmonic if there is too wide a range in the VCO. This situation is shown in Figure 11 where the possible false lock areas are indicated near the (N - 1) and (N + 1) harmonic points. The problem of VCO restraint however is more than just making sure that output frequency f_D isn't able to go to B or A' (the closest false lock points). Actual operating limits are C and C', symmetrically placed frequencies corresponding to $f_{D(min)}$ about Nf_C and $f_{D(max)}$ about $(Nf+1/2)\ f_C$. If the VCO drops below C while the feedback counter is at P_{min} the phase detector will try to push f_D even lower, toward the stable condition at A (Figure 12). Likewise, at C' (when $P = P_{max}$) the tendency is for the loop to accelerate toward lockup at B' (Figure 13). When C or C' are exceeded the loop will "hang up" and not attain the proper lock.

FIGURE 11

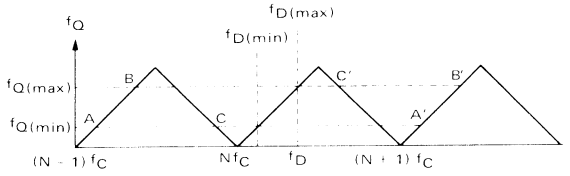


FIGURE 12

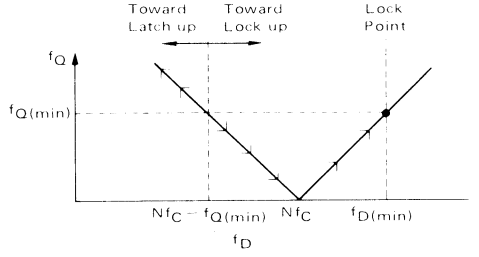
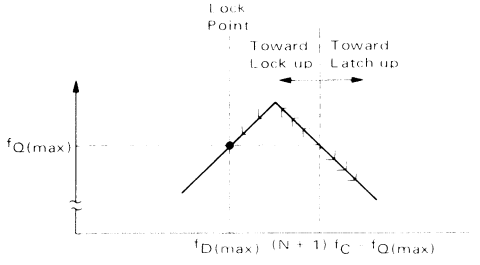
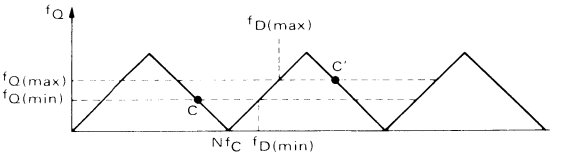


FIGURE 13



The VCO frequency constraints may be quite severe if the minimum f_C formulation is followed and the Nth harmonic is quite high. Where VCO constraint may pose a problem, decrease N below the maximum indicated by Equation (1) until sufficient room is generated by placing the operating range of f_Q on only a small part of the f_D slope (Figure 14). Note that f_C goes up as we approach the more idealized case (Equation 5).

FIGURE 14



The most likely reasons for a "latched up" state in a harmonic loop are turn-on transients and loop overshoot when changing frequency abruptly from one end of the range to the other.

SUMMARY OF SYNTHESIS PROCEDURE

1. Compute harmonic number N

$$N < \frac{f_{D(min)} - f_1}{2\ \Delta f_D}$$

where Δf_D = change in output frequency
f_1 = channel spacing

2. Compute minimum mixing frequency f_C

$$f_C = \frac{f_{D(min)} - f_1}{N}$$

3. Calculate feedback divider's maximum value

$$P_{max} = \frac{\Delta f_D}{f_1} + P_{min}$$

where $P_{min} = 1$ for minimum f_C

4. Find maximum divide-by-P frequency

$$f_{Q(max)} = \Delta f_D + f_1$$

5. Calculate allowable VCO swing

$$Nf_C - f_1 < f_{VCO} < (N + 1)\ f_C - f_{Q(max)}$$

6. If the above constraints are too tight choose the next lower number for N and repeat steps 2 and 5 until satisfied.

SKIP-LOCK TUNING

Harmonic mixing provides an alternate means to frequency synthesis without the feedback divide-by-P network. In this instance the design objective is to provide a large frequency coverage with a set (and relatively wide) channel spacing. The configuration is identical to a single frequency PLL (Figure 15) except it operates in the harmonic mode and tuning is accomplished at the VCO. Output frequency is fixed as being f_1 above all harmonics of f_C. As the VCO is tuned through its range, the loop will acquire and lose signals spaced f_C apart. Since these must be some frequency for the phase detector to operate with, the output frequency cannot be a direct harmonic of f_C. This facet of the circuit often causes users to refer to f_1 as the "offset" frequency.

The value of f_1 is often dictated by output frequency and channel spacing requirements. However the relationship of f_1 to f_C has a large effect on the tunability both up and down the frequency range. If, for example, the loop were locked at point A (Figure 16) and B were the next desired point, then the VCO must be "dragged" from A to A' before lock can be achieved. This frequency adjustment may be quite critical since the frequency difference between A' and B is only $2f_1$. If the VCO is tuned past B the opportunity for lock has been passed.

On the other hand, in going from B to A, the upper end of the VCO control range must only cross A' before the loop acquires frequency A. In either case it's apparent that the loop will not "jump" from one lock point to another and some indication of loop lock should be added. This is normally done by monitoring the VCO dc control line with a pair of comparators and noting when the line reaches its limits.

FIGURE 15

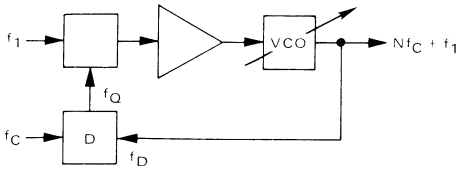
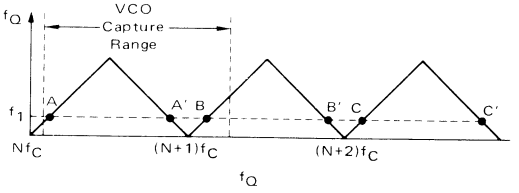


FIGURE 16



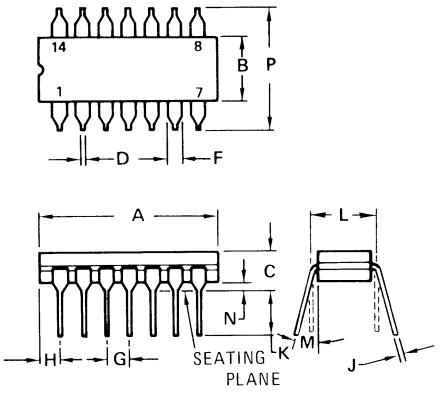
MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Ratings above which device life may be impaired:			
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8.0	Vdc
Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{IL} min	Vdc
Output Source Current	I_o	40	mAdc
Storage Temperature Range	T_{stg}	-55 to +125	°C
Recommended maximum ratings above which performance may be degraded:			
Operating Temperature Range	T_A	0 to +75	°C
DC Fan-Out* (Gates and Flip-Flops)	n	70	—

*AC fan-out is limited by desired system performance.

OUTLINE DIMENSIONS

CASE 632
TO-116



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54 BSC		0.100 BSC	
J	0.203	0.381	0.008	0.015
K	2.54	–	0.100	–
L	7.62 BSC		0.300 BSC	
M	–	15^0	–	15^0
N	0.51	0.76	0.020	0.030
P	–	8.25	–	0.325

All JEDEC dimensions and notes apply.

NOTE:

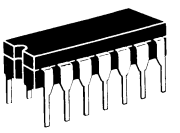
DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

ANALOG MIXER

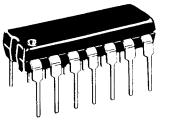
MC12002
MC12502

The MC12002/MC12502 is a double balanced analog mixer, including an input amplifier feeding the mixer carrier port and a temperature compensated bias regulator. The input circuits for both the amplifier and mixer are differential amplifier circuits. The on-chip regulator provides all of the required biasing.

This circuit is designed for use as a balanced mixer in high-frequency wide-band circuits. Other typical applications include suppressed carrier and amplitude modulation, synchronous AM detection, FM detection, phase detection, and frequency doubling, at frequencies up to UHF.

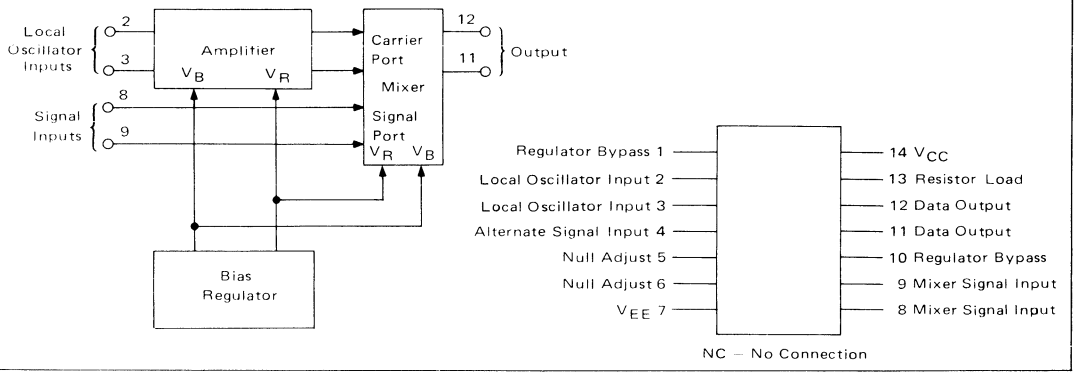


MC12002 – MC12502
L SUFFIX
CERAMIC PACKAGE
CASE 632

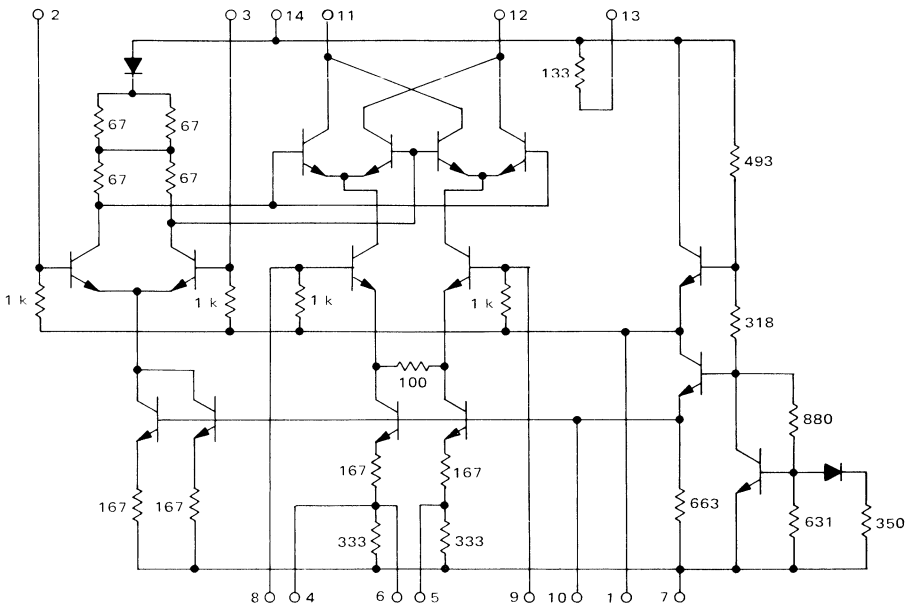


MC12002 only
P SUFFIX
PLASTIC PACKAGE
CASE 646

BLOCK DIAGRAM



ANALOG MIXER CIRCUIT SCHEMATIC



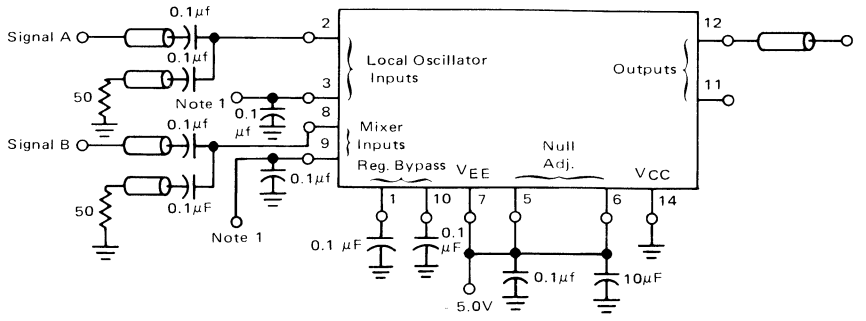
ELECTRICAL CHARACTERISTICS

	TEST VOLTAGE VALUES		
	Volts		
	V_{IHmax}	V_{ILmin}	V_{CC}
MC12502	+2.9	+2.0	+5.0
MC12002	+2.9	+2.0	+5.0

Characteristic	Symbol	Pin Under Test	MC12502 Test Limits							MC12002 Test Limits							VOLTAGE APPLIED TO PINS LISTED BELOW			
			−55°C		+25°C		+125°C			−30°C		+25°C		+85°C						
			Min	Max	Min	Max	Min	Max	Unit	Min	Max	Min	Max	Min	Max	Unit	V_{IHmax}	V_{ILmin}	V_{CC}	Gnd
Power Supply Drain	I_{CC}	14	—	—	—	16	—	—	mAdc	—	—	—	16	—	—	mAdc	—	—	11,12,14	5,6,7
Input Current	I_{inH}	2	—	—	—	0.75	—	—	mAdc	—	—	—	0.75	—	—	mAdc	2	—	11,12,14	5,6,7
		3	—	—	—	0.75	—	—	mAdc	—	—	—	0.75	—	—	mAdc	3	—	11,12,14	5,6,7
		8	—	—	—	0.75	—	—	mAdc	—	—	—	0.75	—	—	mAdc	8	—	11,12,14	5,6,7
		9	—	—	—	0.75	—	—	mAdc	—	—	—	0.75	—	—	mAdc	9	—	11,12,14	5,6,7
	I_{inL}	2	—	—	−0.7	—	—	—	mAdc	—	—	−0.7	—	—	—	mAdc	—	2	11,12,14	5,6,7
		3	—	—	−0.7	—	—	—	mAdc	—	—	−0.7	—	—	—	mAdc	—	3	11,12,14	5,6,7
		8	—	—	−0.7	—	—	—	mAdc	—	—	−0.7	—	—	—	mAdc	—	8	11,12,14	5,6,7
		9	—	—	−0.7	—	—	—	mAdc	—	—	−0.7	—	—	—	mAdc	—	9	11,12,14	5,6,7
Output Current	IO_1	11	—	—	0.7	1.3	—	—	mAdc	—	—	0.7	1.3	—	—	mAdc	—	—	11,12,14	7
		12	—	—	0.7	1.3	—	—	mAdc	—	—	0.7	1.3	—	—	mAdc	—	—	11,12,14	7
	IO_2	11	—	—	2.1	3.9	—	—	mAdc	—	—	2.1	3.9	—	—	mAdc	—	—	11,12,14	5,6,7
		12	—	—	2.1	3.9	—	—	mAdc	—	—	2.1	3.9	—	—	mAdc	—	—	11,12,14	5,6,7
	I_{out}	11	—	—	4.2	7.8	—	—	mAdc	—	—	4.2	7.8	—	—	mAdc	2,9	—	11,12,14	5,6
		11	—	—	4.2	7.8	—	—	mAdc	—	—	4.2	7.8	—	—	mAdc	3,8	—	11,12,14	5,6
		12	—	—	4.2	7.8	—	—	mAdc	—	—	4.2	7.8	—	—	mAdc	2,8	—	11,12,14	5,6
		12	—	—	4.2	7.8	—	—	mAdc	—	—	4.2	7.8	—	—	mAdc	3,9	—	11,12,14	5,6
Differential Current	ΔIO_1	11,12	−50	+50	−50	+50	−50	+50	μAdc	−100	+100	−100	+100	−100	+100	μAdc	—	—	11,12,14	7
	ΔIO_2	11,12	−100	+100	−100	+100	−100	+100	μAdc	−200	+200	−200	+200	−200	+200	μAdc	—	—	11,12,14	5,6,7
Bias Voltage	V_{Bias}	1	2.34	2.54	2.32	2.52	2.29	2.49	Vdc	2.33	2.53	2.32	2.52	2.30	2.50	Vdc	—	—	11,12,14	5,6,7
		4	390	590	400	600	420	620	mVdc	390	590	400	600	410	610	mVdc	—	—	11,12,14	5,6,7
		5	275	415	285	425	305	445	mVdc	275	415	285	425	295	435	mVdc	—	—	11,12,14	7
		6	275	415	285	425	305	445	mVdc	275	415	285	425	295	435	mVdc	—	—	11,12,14	7
		10	1.300	1.500	1.185	1.385	1.050	1.250	Vdc	1.260	1.460	1.185	1.385	1.105	1.305	Vdc	—	—	11,12,14	5,6,7
																	Pulse In	Pulse Out	−3.0 V	Gnd	V_{EE}
AC Gain (See Figure 1)	A_V	11	—	—	6.0	—	—	—	V/V	—	—	5.0	—	—	—	V/V	2	11	9	14	7
(Frequency = 100 MHz) *Note		11	—	—	0.33	—	—	—	V/V	—	—	0.28	—	—	—	V/V	8	11	3	14	7

*Note: AC Gain is a function of collector load impedance.

FIGURE 1 – A.C. GAIN TEST



Note 1:
V_{IL} = 3.0 V on pin 3 when pin 8 is under test.
V_{IL} = 3.0 V on pin 9 when pin 2 is under test.

Signal A = 30 mV p-p

Signal B = 300 mV p-p

Freq. = 100 MHz

All input and output cables to the scope are equal lengths of 50-ohm coaxial cable.
The unused output is connected to a 50-ohm resistor to ground.

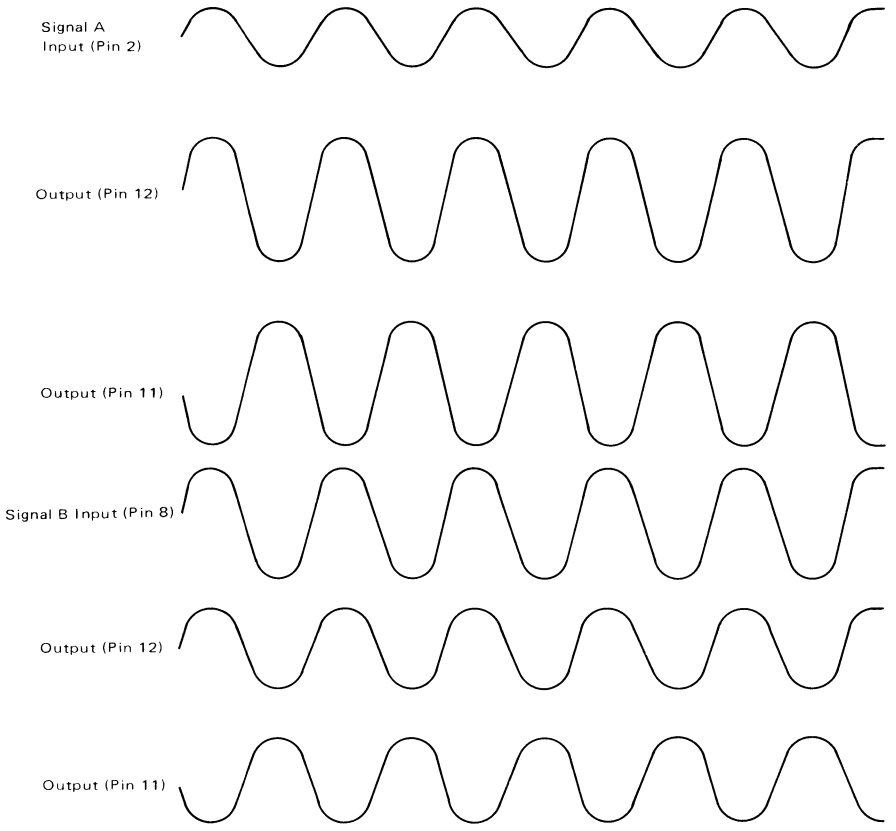


FIGURE 2 – CARRIER FEEDTHROUGH TEST CIRCUITS

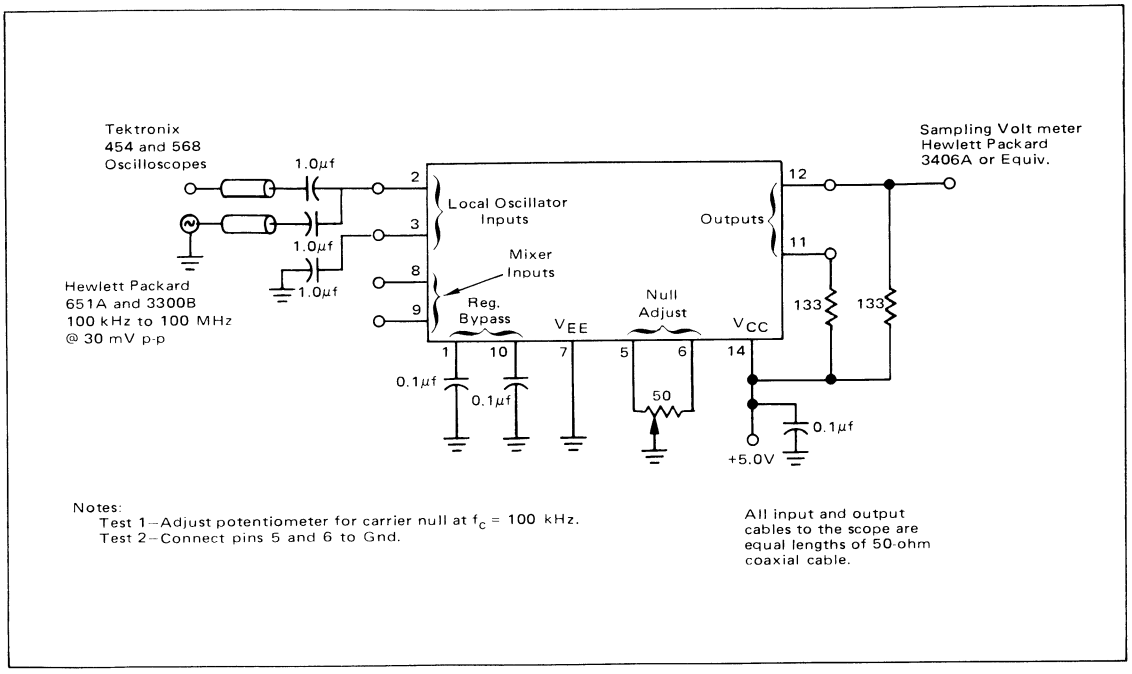


FIGURE 3 – CARRIER FEEDTHROUGH VERSUS FREQUENCY (Test 1)

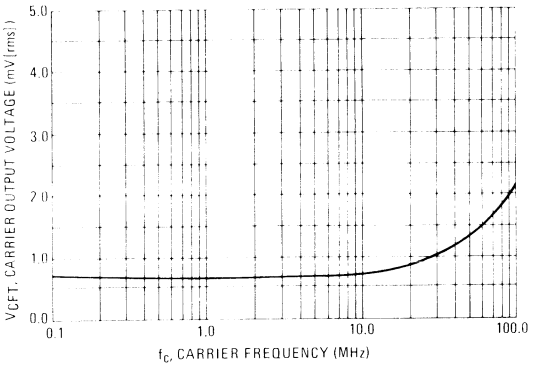


FIGURE 4 – CARRIER FEEDTHROUGH VERSUS FREQUENCY (Test 2)

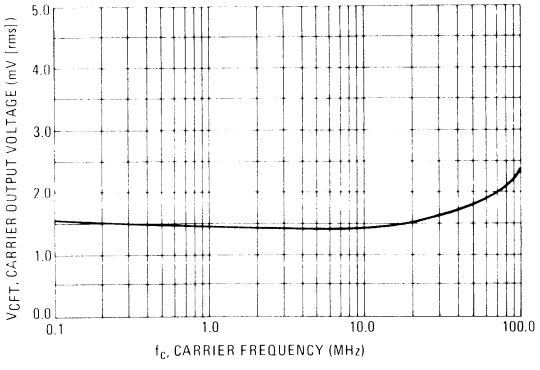


FIGURE 5 – CARRIER SUPPRESSION TEST CIRCUIT

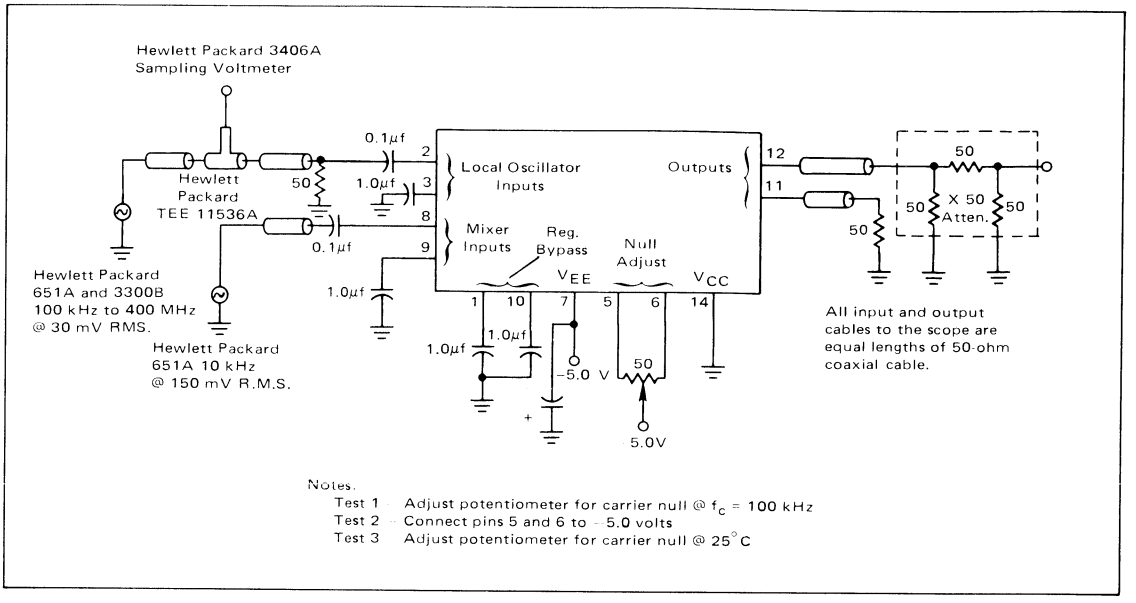


FIGURE 6 – CARRIER SUPPRESSION VERSUS FREQUENCY (Test 1)

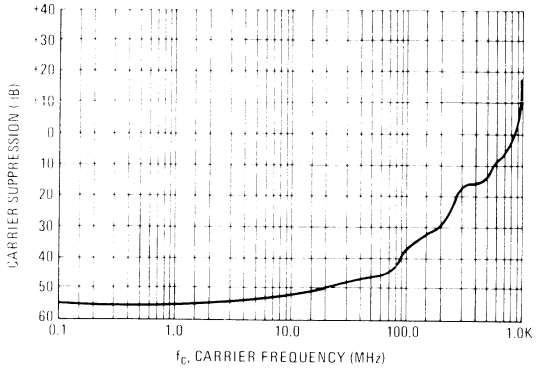


FIGURE 7 – CARRIER SUPPRESSION VERSUS FREQUENCY (Test 2)

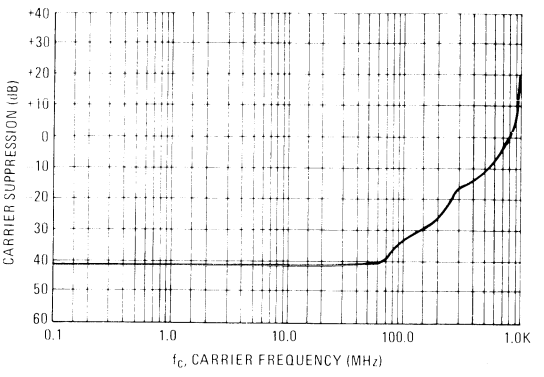


FIGURE 8 – CARRIER SUPPRESSION VERSUS TEMPERATURE

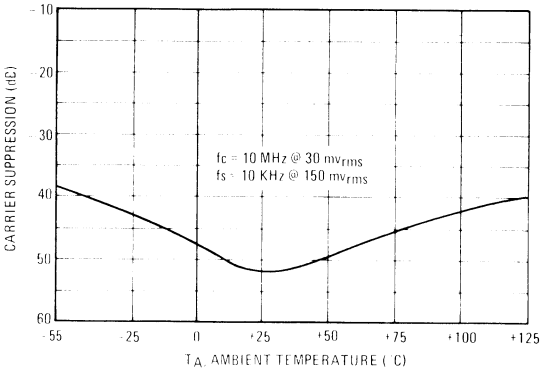
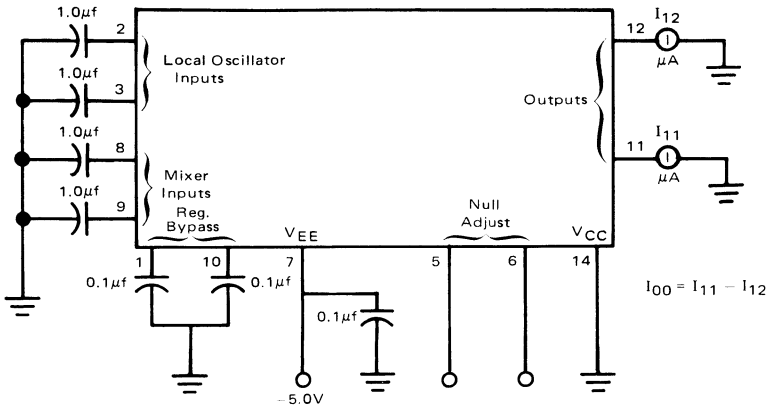


FIGURE 9 – OUTPUT OFFSET CURRENT (I_{00}) VERSUS TEMPERATURE



Notes:
Test 1 – Pins 5 and 6 left open
Test 2 – Pins 5 and 6 are tied to −5.0 volts

FIGURE 10 – OUTPUT OFFSET CURRENT VERSUS TEMPERATURE

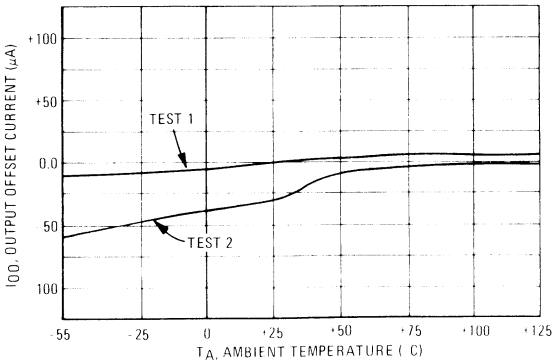
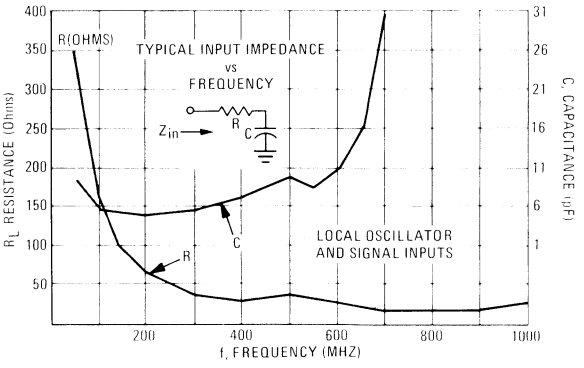


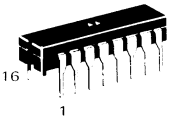
FIGURE 11 – TYPICAL INPUT IMPEDANCE VERSUS FREQUENCY (NO CIRCUIT)



TWO-MODULUS PRESCALER

MC12012

The MC12012 is a two-modulus prescaler which consists of three functional blocks: 1) a controllable divide by 5/divide by 6 prescaler; 2) a divide by 2 prescaler; and 3) a MECL to MTTL translator. When used with the MC12014 Counter Control Logic function and the MC4016 programmable counter, a divide by N programmable counter can be constructed for operation to 200 MHz. This arrangement is especially useful in frequency synthesizer applications.



CERAMIC PACKAGE
CASE 620

- ÷2, ÷5/÷6, ÷10/÷11, ÷10/÷12
- MECL to MTTL Translator on Chip
- +5.0 or -5.2 V Operation*
- 200 MHz (typ) Toggle Frequency

*When using +5.0 V supply, apply +5.0 V to pin 16 (V_{CC}) and ground pin 8 (V_{EE}). When using -5.2 V supply, ground pin 16 (V_{CC}) and apply -5.2 V to pin 8 (V_{EE}).

PIN ASSIGNMENT

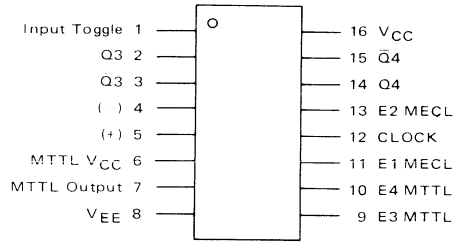
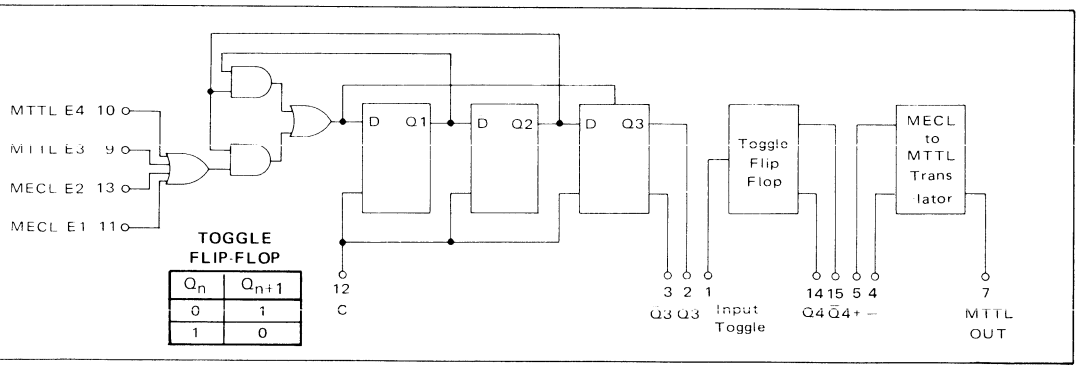


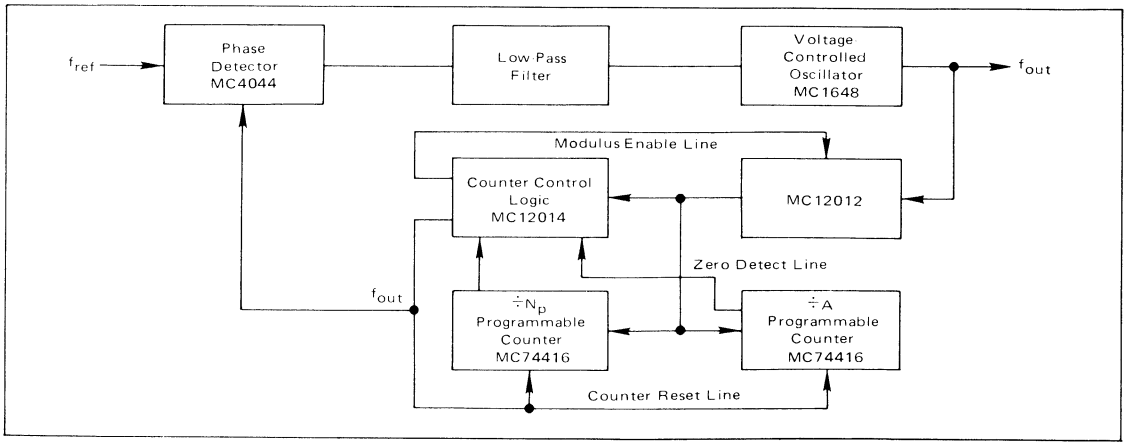
FIGURE 1 – LOGIC DIAGRAM



TOGGLE FLIP-FLOP

Q_n	Q_{n+1}
0	1
1	0

FIGURE 2 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Ratings above which device life may be impaired:			
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8.0	Vdc
Input Voltage (V_{CC} = 0)	V_{in}	0 to $V_{IL\,min}$	Vdc
Output Source Current	I_o	20	mAdc
Storage Temperature Range	T_{stg}	-55 to +125	°C
Recommended maximum ratings above which performance may be degraded:			
Operating Temperature Range	T_A	0 to +75	°C
DC Fan-Out* (Gates and Flip-Flops)	n	70	

*AC fan-out is limited by desired system performance.

ELECTRICAL CHARACTERISTICS

Supply Voltage -5.2 V

@ Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}
	TEST VOLTAGE/CURRENT VALUES													
	Volts											mA		
0°C	-0.840	-1.870	-1.145	-1.490	-4.7	-2.8	+0.3	-0.7	-3.2	-4.4	-5.2	-2.5	16	-1.6
25°C	-0.810	-1.850	-1.105	-1.475	-4.7	-2.8	+0.3	-0.7	-3.2	-4.4	-5.2	-2.5	16	-1.6
75°C	-0.720	-1.880	-1.045	-1.450	-4.7	-2.8	+0.3	-0.7	-3.2	-4.4	-5.2	-2.5	16	-1.6

Characteristic	Symbol	Pin Under Test	MC12012 0°C Min	MC12012 0°C Max	MC12012 +25°C Min	MC12012 +25°C Typ	MC12012 +25°C Max	MC12012 +75°C Min	MC12012 +75°C Max	Unit	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}	(V_{CC}) Gnd
			TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW																						
Power Supply Drain Current	I_E	8	–	–	–	100	–	–	–	mAdc	–	–	–	–	–	–	–	–	–	–	8	–	–	–	6,16
Input Current	I_{INH1}	12	–	–	–	100	200	–	–	µAdc	12	–	–	–	–	–	–	–	–	–	8	–	–	–	16
	I_{INH2}	1 11 13	– – –	– – –	– – –	40 40 40	100 100 100	– – –	– – –	µAdc	1 11 13	– – –	– – –	– – –	– – –	– – –	– – –	– – –	– – –	– – –	8 8 8	– – –	– – –	– – –	16 16 16
	I_{INH3}	9 10	– –	– –	– –	– –	40 40	– –	– –	µAdc	– –	– –	– –	– –	– –	– –	9 10	– –	– –	– –	8 8	– –	– –	– –	16 16
	I_{INH4}	4 5	– –	– –	3.5 3.5	– –	5.5 5.5	– –	– –	mAdc mAdc	5 5	4 4	– –	– –	– –	– –	– –	– –	– –	– –	8 8	– –	– –	– –	6 6
	I_{INL1} (Leakage Current)	1 11 12 13	– – – –	– – – –	– – – –	– – – –	2.0 ↓ ↓ ↓	– – – –	– – – –	µAdc ↓ ↓ ↓	– – – –	– – – –	– – – –	– – – –	– – – –	– – – –	– – – –	– – – –	– – – –	– – – –	1.8 8,11 8,12 8,13	– ↓ ↓ ↓	– ↓ ↓ ↓	– ↓ ↓ ↓	16 ↓ ↓ ↓
	I_{INL2}	9 10	– –	– –	1.1 1.1	– –	2.2 2.2	– –	– –	mAdc mAdc	– –	– –	– –	– –	9 10	– –	– –	– –	– –	– –	8 8	– –	– –	– –	16 16
	I_{INL3}	4 5	– –	– –	3.8 2.0	– –	6.5 4.0	– –	– –	mAdc mAdc	4 4	5 5	– –	– –	– –	– –	– –	– –	– –	– –	8 8	– –	– –	– –	16 16
Logic "1" Output Voltage	V_{OH1} ②	2 3 14 15	-1.000 ↓ ↓ ↓	-0.840 ↓ ↓ ↓	-0.960 ↓ ↓ ↓	– – – –	-0.810 ↓ ↓ ↓	-0.900 ↓ ↓ ↓	-0.720 ↓ ↓ ↓	Vdc ↓ ↓ ↓	– – – –	11,13 11,13 – –	– – – –	– – – –	9,10 9,10 – –	– – – –	– – – –	– – – –	– – – –	– – – –	8 ↓ ↓ ↓	2 3 14 15	– – – –	– – – –	16 ↓ ↓ ↓
	V_{OH2}	7	-2.800	–	-2.800	–	–	-2.800	–	Vdc	5	4	–	–	–	–	–	–	–	–	8	–	–	7	6
Logic "0" Output Voltage	V_{OL1} ②	2 3 14 15	-1.870 ↓ ↓ ↓	-1.635 ↓ ↓ ↓	-1.850 ↓ ↓ ↓	– – – –	-1.620 ↓ ↓ ↓	-1.830 ↓ ↓ ↓	-1.595 ↓ ↓ ↓	Vdc ↓ ↓ ↓	– – – –	11,13 11,13 – –	– – – –	– – – –	9,10 9,10 – –	– – – –	– – – –	– – – –	– – – –	– – – –	8 ↓ ↓ ↓	2 3 14 15	– – – –	– – – –	16 ↓ ↓ ↓
	V_{OL2}	7	–	-4.700	–	–	-4.700	–	-4.700	Vdc	4	5	–	–	–	–	–	–	–	–	8	–	7	–	6
Logic "1" Threshold Voltage	V_{OHA}	2 ③ 3 ③ 14 ④ 15 ④	-1.020 ↓ ↓ ↓	– – – –	-0.980 ↓ ↓ ↓	– – – –	– – – –	-0.920 ↓ ↓ ↓	– – – –	Vdc ↓ ↓ ↓	– – – –	– – – –	11,13 11,13 – –	– – – –	– – – –	– – – –	– – – –	– – – –	9,10 9,10 – –	– – – –	8 ↓ ↓ ↓	2 3 14 15	– – – –	– – – –	16 ↓ ↓ ↓
Logic "0" Threshold Voltage	V_{OLA}	2 ⑤ 3 ⑤ 14 ④ 15 ④	– – – –	-1.615 ↓ ↓ ↓	– – – –	– – – –	-1.600 ↓ ↓ ↓	– – – –	-1.575 ↓ ↓ ↓	Vdc ↓ ↓ ↓	– – – –	– – – –	– – – –	11,13 11,13 – –	– – – –	– – – –	– – – –	– – – –	– – – –	9,10 9,10 –	8 ↓ ↓ ↓	2 3 14 15	– – – –	– – – –	16 ↓ ↓ ↓
Short Circuit Current	I_{OS}	7	-20	-65	-20	–	-65	-20	-65	mAdc	5	4	–	–	–	–	–	–	–	–	8	–	–	–	6

ELECTRICAL CHARACTERISTICS

Supply Voltage +5.0 V

Characteristic	Symbol	Pin Under Test	MC12012 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: Volts V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{HT}	V_{LT}	V_{CC}	mA I_L	I_{OL}	I_{OH}	V_{EE} Gnd
Power Supply Drain Current	I_E	8	–	–	–	95	200	–	–	mAdc	12	–	–	–	–	–	–	–	–	–	16	–	–	–	8
Input Current	I_{INH1}	12	–	–	–	100	200	–	–	µAdc	12	–	–	–	–	–	–	–	–	–	16	–	–	–	8
	I_{INH2}	1 11 13	–	–	–	40 40 40	100 100 100	–	–	µAdc	1 11 13	–	–	–	–	–	–	–	–	–	16 16 16	–	–	–	8 8 8
	I_{INH3}	9 10	–	–	–	–	40 40	–	–	µAdc	–	–	–	–	–	–	9 10	–	–	–	16 16	–	–	–	8 8
	I_{INH4}	4 5	–	–	–	3.5 3.5	5.5 5.5	–	–	mAdc mAdc	5 5	4 4	–	–	–	–	–	–	–	–	6 6	–	–	–	8 8
	I_{INL1} Leakage Current	1 11 12 13	–	–	–	–	2.0	–	–	µAdc	–	–	–	–	–	–	–	–	–	–	16	–	–	–	13 8, 11 8, 12 8, 13
	I_{INL2}	9 10	–	–	–	1.1 1.1	2.2 2.2	–	–	mAdc mAdc	–	–	–	–	9 10	–	–	–	–	–	16 16	–	–	–	8 8
	I_{INL3}	4 5	–	–	–	3.8 2.0	6.5 4.0	–	–	mAdc mAdc	4 4	5 5	–	–	–	–	–	–	–	–	6 6	–	–	–	8 8
Logic "1" Output Voltage ②	V_{OH1}	2 3 14 15	4.000	4.160	4.040	–	–	4.100	4.280	Vdc	–	11.13 11.13	–	9.10 9.10	–	–	–	–	–	–	16	2 3 14 15	–	–	8
	V_{OH2}	7	2.400	–	2.400	–	–	2.400	–	Vdc	5	4	–	–	9 10	–	–	–	–	–	16	–	–	–	8
Logic "0" Output Voltage ②	V_{OL1}	2 3 14 15	3.190	3.430	3.210	–	–	3.440	3.470	Vdc	–	11.13 11.13	–	9.10 9.10	–	–	–	–	–	–	16	2 3 14 15	–	–	8
	V_{OL2}	7	–	0.500	–	–	0.500	–	0.500	Vdc	4	5	–	–	–	–	–	–	–	–	6	–	–	–	7
Logic "1" Threshold Voltage	V_{OHA}	2 ③ 3 ③ 14 ④ 15 ④	3.980	–	4.020	–	–	4.080	–	Vdc	–	–	11.13 11.13	–	–	–	–	–	–	–	16	2 3 14 15	–	–	8
Logic "0" Threshold Voltage	V_{OLA}	2 ⑤ 3 ⑤ 14 ④ 15 ④	–	3.450	–	–	3.460	–	3.490	Vdc	–	–	–	11.13 11.13	–	–	–	–	9.10 9.10	9.10 9.10	16	2 3 14 15	–	–	8
Short Circuit Current	I_{OS}	7	-20	-65	-20	–	-65	-20	-65	mAdc	5	4	–	–	–	–	–	–	–	–	6	–	–	–	8

@ Test Temperature
0°C
25°C
75°C

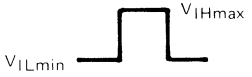
V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IL}	V_{IH}	V_{IHH}	V_R	V_{HT}	V_{LT}	V_{CC}	I_L	I_{OL}	I_{OH}
-4.160	-3.130	+3.855	-3.510	+0.5	+2.4	+5.5	+4.5	+2.0	+0.8	+5.0	-2.5	16	-1.6
-4.190	-3.150	+3.895	-3.525	+0.5	+2.4	+5.5	+4.5	+2.0	+0.8	+5.0	-2.5	16	-1.6
-4.280	-3.170	+3.955	-3.550	+0.5	+2.4	+5.5	+4.5	+2.0	+0.8	+5.0	-2.5	16	-1.6

Characteristic	Symbol	Pin Under Test	MC12012 0°C Min	MC12012 0°C Max	MC12012 +25°C Min	MC12012 +25°C Typ	MC12012 +25°C Max	MC12012 +75°C Min	MC12012 +75°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse Gen. 1	Pulse Gen. 2	Pulse Gen. 3	V_{IHmin} +1.100	V_{ILmin} +0.130	V_R +0.000	V_F -3.0 V	V_{EE} -3.0 or -3.2	V_{CC} +2.0
Propagation Delay (See Figures 3 and 4)	t_{12+2+}	12,2	—	—	2.0	3.0	4.0	—	—	ns	12	—	—	—	11,13	—	9,10	8	6,16
	t_{12+3+}	12,3	—	—	↓	3.0	↓	—	—	↓	↓	—	—	—	11,13	—	9,10	↓	↓
	t_{12+}	12,2	—	—		2.8		—	—			—	—	—	11,13	—	9,10		
	t_{12+3-}	12,3	—	—		2.8		—	—			—	—	—	11,13	—	9,10		
	t_{1+14+}	1,14	—	—		3.0		—	—		1	—	—	—	—	—	—		
	t_{1+15+}	1,15	—	—		3.0		—	—		↓	—	—	—	—	—	—		
	t_{1+14-}	1,14	—	—		2.8		—	—			—	—	—	—	—	—		
	t_{1+15-}	1,15	—	—		2.8	↓	—	—			—	—	—	—	—	—		
	t_{5+7+}	5,7	—	—		8.0	12.0	—	—		A	—	—	—	—	—	—		
	t_{5-7-}	5,7	—	—	↓	5.0	10.0	—	—	↓	A	—	—	—	—	—	—	↓	↓
Output Rise Time (See Figure 4)	t_{2+}	2	—	—	—	2.0	—	—	—	ns	12	—	—	—	11,13	—	9,10	8	6,16
	t_{3+}	3	—	—	—	2.0	—	—	—	↓	12	—	—	—	11,13	—	9,10	↓	↓
	t_{14+}	14	—	—	—	2.0	—	—	—		1	—	—	—	—	—	—		
	t_{15+}	15	—	—	—	2.0	—	—	—	↓	1	—	—	—	—	—	—	↓	↓
Output Fall Time (See Figure 4)	t_{2-}	2	—	—	—	2.0	—	—	—	ns	12	—	—	—	11,13	—	9,10	8	6,16
	t_{3-}	3	—	—	—	2.0	—	—	—	↓	12	—	—	—	11,13	—	9,10	↓	↓
	t_{14-}	14	—	—	—	2.0	—	—	—		1	—	—	—	—	—	—		
	t_{15-}	15	—	—	—	2.0	—	—	—	↓	1	—	—	—	—	—	—	↓	↓
Setup Time (See Figure 5)	t_{setup1}	11,13	—	4.0	—	2.4	3.0	—	4.0	ns	12	11/13	—	—	13/11	—	9,10	8	6,16
	t_{setup2}	9,10	—	7.0	—	5.0	7.0	—	8.5	ns	12	—	9/10	—	11,13	—	10/9	8	6,16
Release Time (See Figure 5)	t_{rel1}	11,13	—	2.5	—	1.2	2.0	—	2.0	ns	12	11/13	—	—	13/11	—	9,10	8	6,16
	t_{rel2}	9,10	—	4.0	—	2.5	3.5	—	2.0	ns	12	—	9/10	—	11,13	—	10/9	8	6,16
Toggle Frequency	f_{max}									MHz									
Figure 6 (÷5)		2	—	—	175	200	—	—	—		—	—	—	11	13	—	9,10	8	16
(÷6)		2	—	—	↓	↓	—	—	—		—	—	—	—	11,13	—	9,10	↓	↓
(÷2)		14	—	—			—	—	—		—	—	—	—	—	—	—		
Figure 7 (÷10 or 11)	↓	14	—	—	↓	↓	—	—	—	↓	—	—	—	—	—	—	—	↓	↓

① All MECL outputs (2,3,14,15) are terminated to V_{EE} through an externa 510 Ω resistor during the DC tests.

② Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is

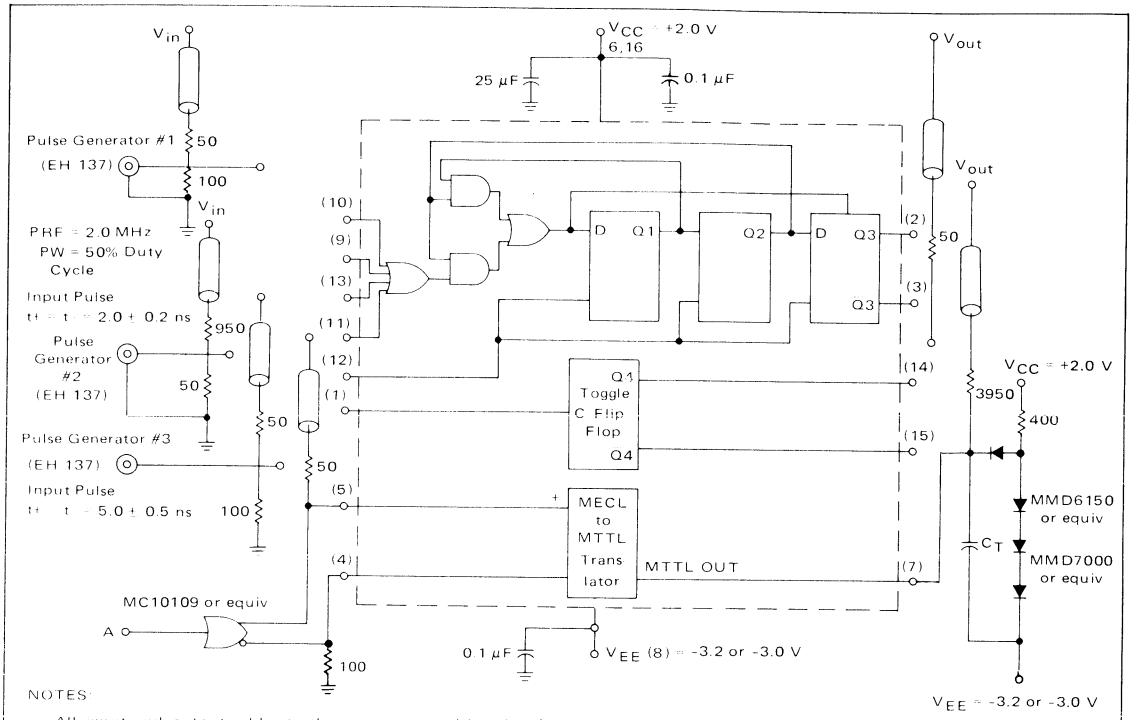
③ In addition to meeting the output levels specified, the device must divide by 5 during this test. The clock input is



④ In addition to meeting the output levels specified the device must divide by 2 with a clock input of

⑤ In addition to meeting the output levels specified, the device must divide by 6 during this test. The clock input is

FIGURE 3 – AC TEST CIRCUIT



NOTES:

All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.

All unused cables must be terminated with 50 ohms.

All resistors are ± 1%.

C_T = 15 pF = total parasitic capacitance which includes probe, wiring, and load capacitance.

The 950 ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe.

The 50 ohm resistor and the scope termination impedance constitute a 2:1 attenuator probe.

FIGURE 4 – AC VOLTAGE WAVEFORMS

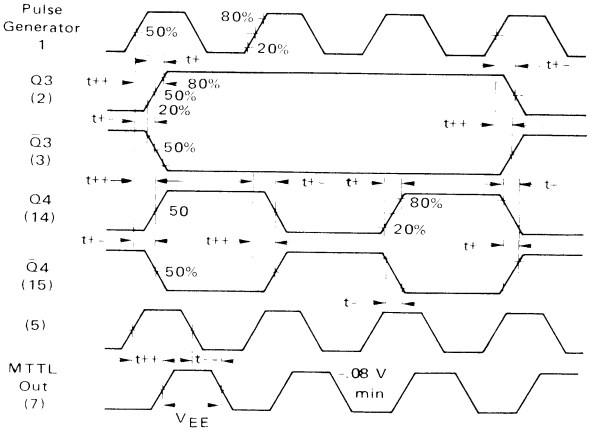


FIGURE 5 – SETUP AND RELEASE TIME WAVEFORMS

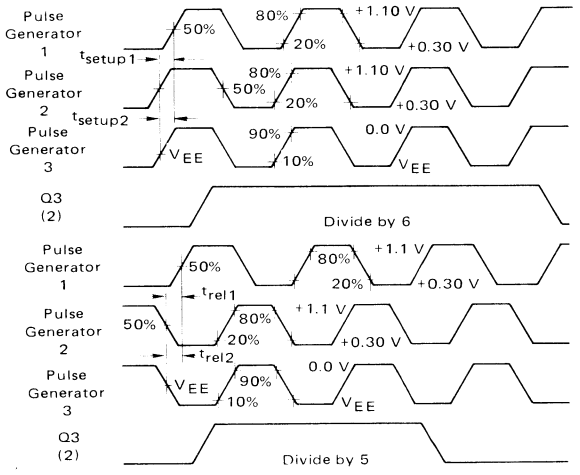
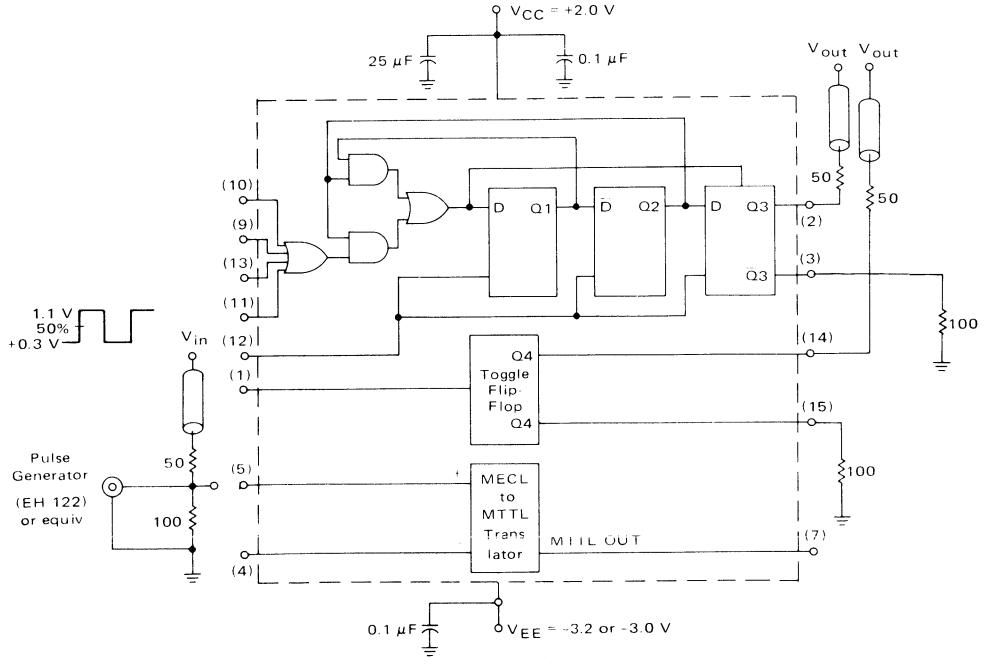
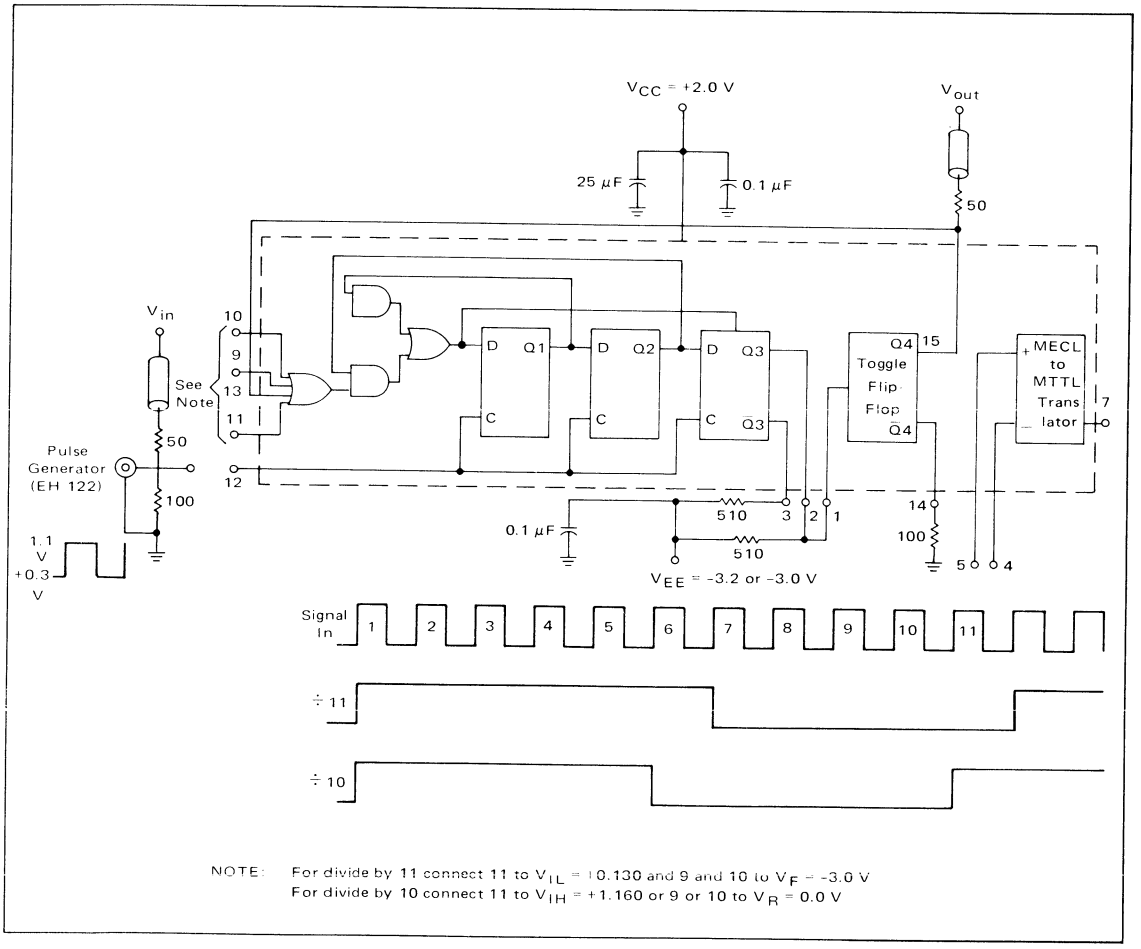


FIGURE 6 – MAXIMUM FREQUENCY TEST CIRCUIT



NOTE: Output Waveforms are same as shown in Figures 4 and 5.

FIGURE 7 – MAXIMUM FREQUENCY TEST CIRCUIT



NOTE: For divide by 11 connect 11 to V_{IL} = +0.130 and 9 and 10 to V_F = -3.0 V
For divide by 10 connect 11 to V_{IH} = +1.160 or 9 or 10 to V_R = 0.0 V

FIGURE 8 – STATE DIAGRAMS

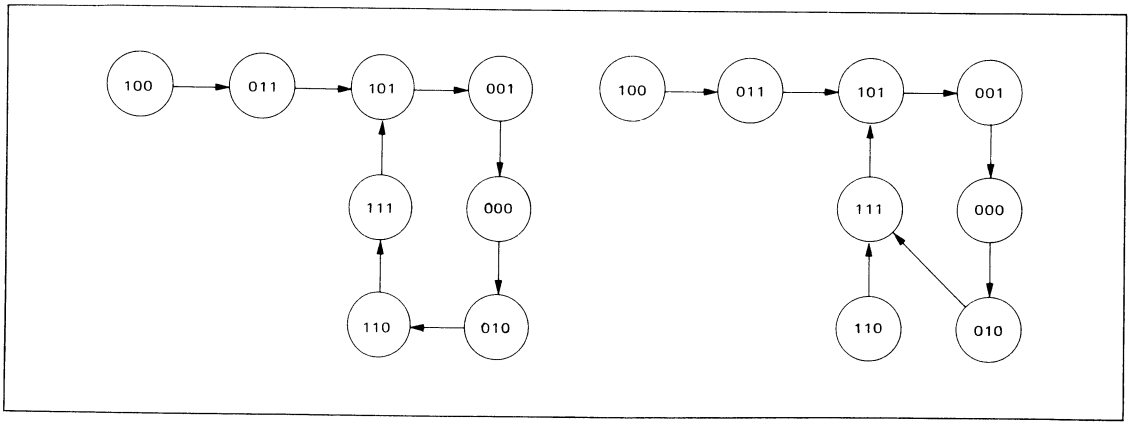
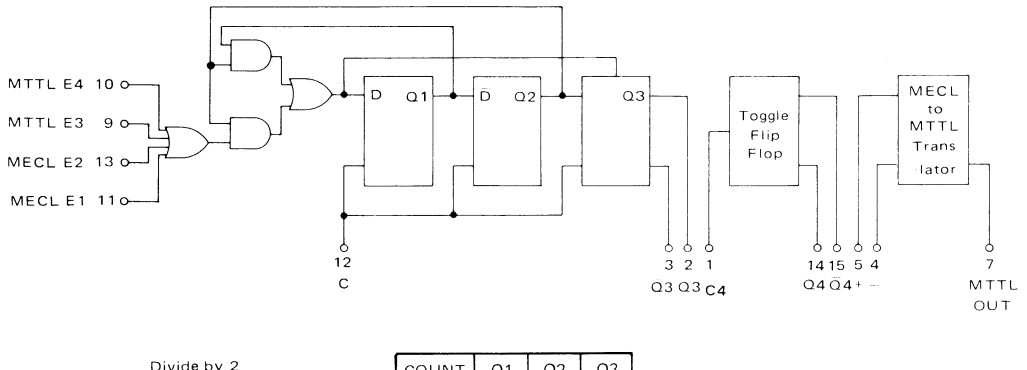


FIGURE 9 – ÷5/6



Divide by 2 use Toggle Flip-Flop

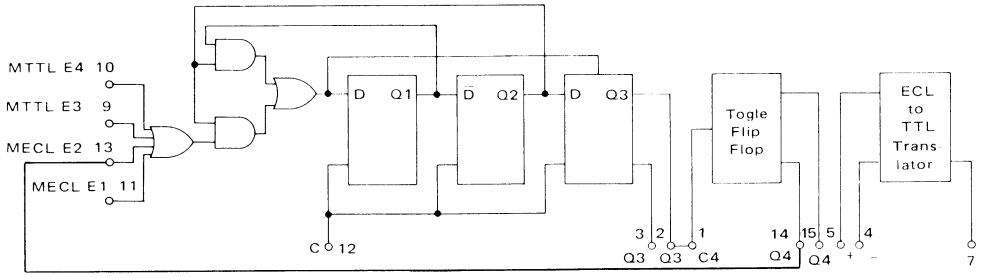
COUNT	Q1	Q2	Q3
6	0	1	1
7	1	1	1
5	1	0	1
1	1	0	0
0	0	0	0
2	0	1	0

E1 + E2 + E3 + E4 = 1

E1 + E2 + E3 + E4 = 0

To obtain a MTTL output connect 5 and 4 to 2 and 3 or 14 and 15 respectively.

FIGURE 10 – ÷10/11



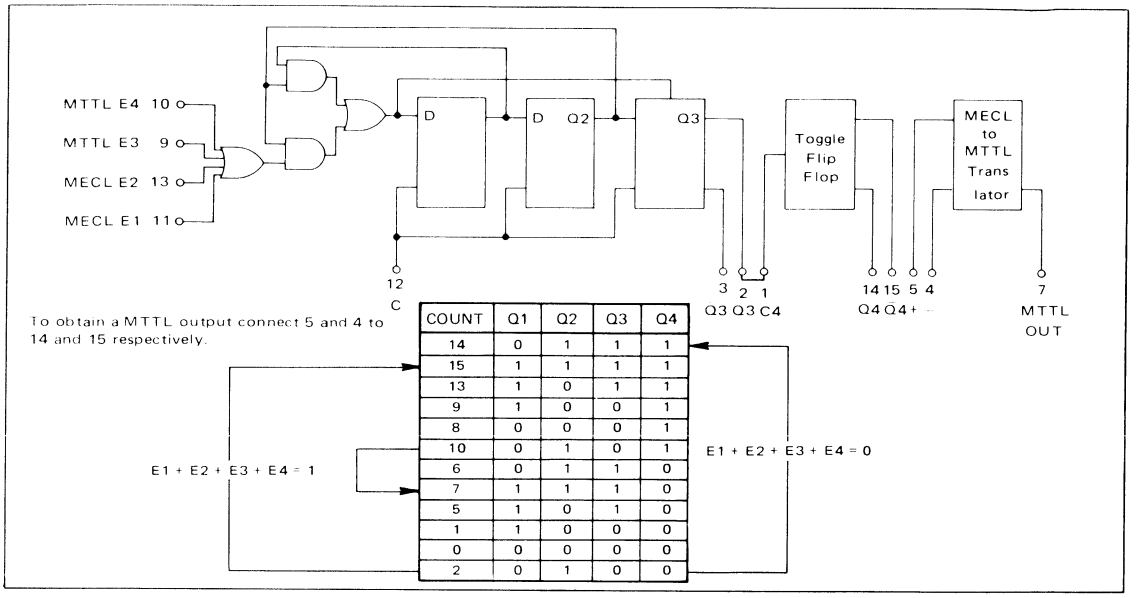
COUNT	Q1	Q2	Q3	Q4
14	0	1	1	1
15	1	1	1	1
13	1	0	1	1
9	1	0	0	1
8	0	0	0	1
10	0	1	0	1
7	1	1	1	0
5	1	0	1	0
1	1	0	0	0
0	0	0	0	0
2	0	1	0	0

E1 + E3 + E4 = 1

E1 + E3 + E4 = 0

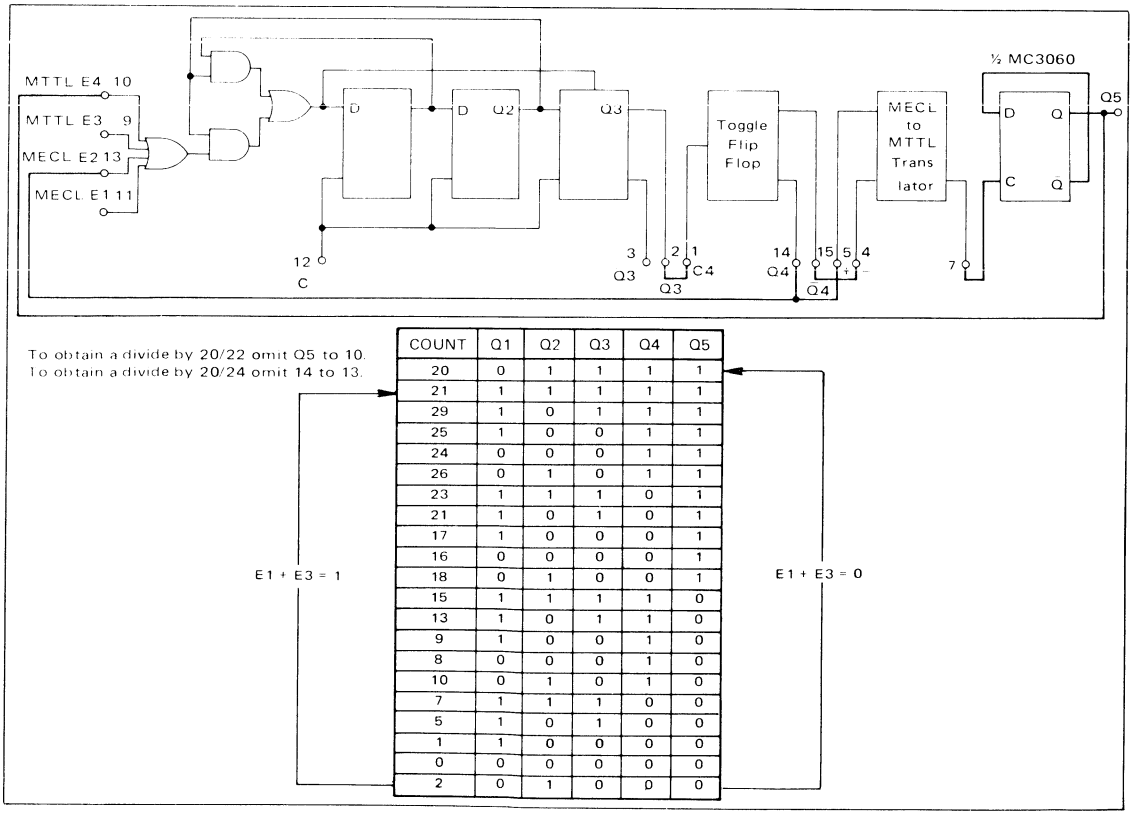
To obtain a MTTL output connect 5 and 4 to 14 and 15 respectively.

FIGURE 11 – ÷ 10/12



COUNT	Q1	Q2	Q3	Q4
14	0	1	1	1
15	1	1	1	1
13	1	0	1	1
9	1	0	0	1
8	0	0	0	1
10	0	1	0	1
6	0	1	1	0
7	1	1	1	0
5	1	0	1	0
1	1	0	0	0
0	0	0	0	0
2	0	1	0	0

FIGURE 12 – ÷ 20/21



COUNT	Q1	Q2	Q3	Q4	Q5
20	0	1	1	1	1
21	1	1	1	1	1
29	1	0	1	1	1
25	1	0	0	1	1
24	0	0	0	1	1
26	0	1	0	1	1
23	1	1	1	0	1
21	1	0	1	0	1
17	1	0	0	0	1
16	0	0	0	0	1
18	0	1	0	0	1
15	1	1	1	1	0
13	1	0	1	1	0
9	1	0	0	1	0
8	0	0	0	1	0
10	0	1	0	1	0
7	1	1	1	0	0
5	1	0	1	0	0
1	1	0	0	0	0
0	0	0	0	0	0
2	0	1	0	0	0

FUNCTION DESCRIPTION

INTRODUCTION

The MC12012 is one part of a variable modulus (divisor) prescaling subsystem used in certain Digital Phase-Locked Loops (PLL).

More often than not, the feedback loop of any PLL contains a counter-divider. Many methods are available for building a divider, but not all are simple, economical, or convenient in a particular application.

The technique and system described here offer a new approach to the construction of a phase-locked loop divider. In addition to using the MC12012 variable modulus prescaler, this system requires an MC12014 Counter Control Logic function, together with suitable programmable counters (e.g. MC4016s). Data sheets for these additional devices should be consulted for their particular functional descriptions.

THE MC12012 TWO MODULUS PRESCALER

Three functional blocks are contained in the MC12012 variable modulus prescaler: 1) a controllable ÷5/÷6 prescaler; 2) a ÷ 2 prescaler; and 3) an ECL to TTL translator (for single power supply operation).

Selection of division by 5 or by 6 is made by inputs to E1 through E4. If all E inputs are low before the transition of the clock pulse driving Q3 high, Q3 will stay high for 3 clock pulses, then will go low for 3 clock pulses. This provides a divide by 6 function.

On the other hand, if any one or all of the E inputs are high prior to the positive transition of the clock pulse driving Q3 high, Q3 will stay high for only 2 clock pulses, then will go low for 3 clock pulses. The result is division by 5.

For the ÷5 operation, at least one of the E inputs must go high sometime before the clock pulse. This time is referred to as the "setup time." Specifications for setup time are given in the electrical characteristics table: t_{setup1} and t_{setup2} for E1 and E2 (MECL inputs), and E3 and E4 (MTTL inputs).

For the divide by 6 operation all E inputs must be low for some time prior to the clock pulse. This time is referred to as the "release time." Data for release time is given in the electrical characteristics table; t_{re1} and t_{re2} for E1, E2, E3, E4.

The data given in the tables for setup and release times are referenced to the positive transition of the clock pulse causing Q3 to go high. If it is necessary to reference the setup and release times to the positive transition of Q3, add t++ (specified for Q3) to the setup/release times given. It should be noted that the logic states for the enable inputs are important only for only one clock pulse which causes Q3 to go high (within the limits specified by setup and release times).

The ÷ 5/÷ 6 prescaler may be connected externally to the ÷ 2 prescaler to form a ÷ 10/÷ 11 prescaler (Figure 10) or a ÷ 10/÷ 12 prescaler (Figure 11).

By way of an example showing how a ÷ 10/÷ 11 prescaler operates, note that if E1, E3, and E4 (Figure 10) are held in a low state, the counter divides by 11. To do this, a feedback connection is established from Q4 to E2 (or to E1). With this feedback, the ÷ 5/÷ 6 prescaler divides by 5 when Q4 is high, and by 6 when Q4 is low.

Since Q4 changes state with each positive transition of Q3, the prescaler alternates between ÷ 5 and ÷ 6 resulting in a ÷ 11 at Q4.

If any one or all of the E inputs are high (Figure 10), the 5/6 prescaler always divides by 5 and a divide by 10 results at Q4.

With the addition of external flip-flops and counters (MECL or MTTL) various other modulus prescalers may be produced (20/21, 20/22, 20/24, 40/41, 50/51, 100/101, etc.).

THE TECHNIQUE OF DIRECT PROGRAMMING BY UTILIZING A TWO MODULUS PRESCALER (MC12012)

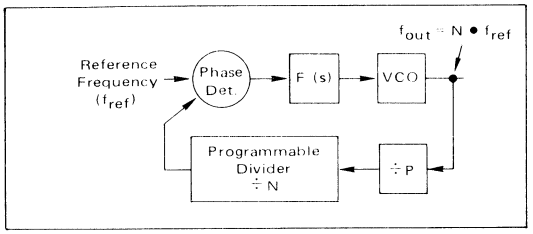
The disadvantage of using a fixed modulus (÷ P) for frequency division in high frequency phase-locked loops (PLL) is that it requires dividing the desired reference frequency by P also (desired reference frequency equals channel spacing.)

The MC12012 is specially designed for use with a technique called "variable modulus prescaling". This technique allows a simple MECL two-modulus prescaler (MC12012) to be controlled by a relatively slow MTTL programmable counter. The use of this technique permits direct high-frequency prescaling without any sacrifice in resolution since it is no longer necessary to divide the reference frequency by the modulus of the high frequency prescaler.

The theory of "variable modulus prescaling" may be explained by considering the system shown in Figure 13. For the loop shown:

$$f_{out} = N \bullet P \bullet f_{ref} \quad (1)$$

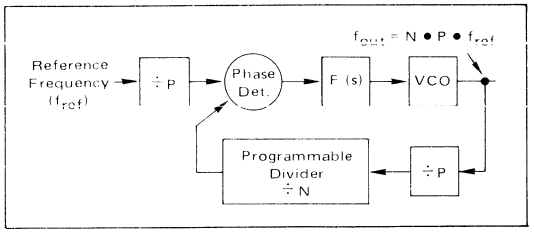
FIGURE 13 – FREQUENCY SYNTHESIS BY PRESCALING



where P is fixed and N is variable. For a change of 1 in N, the output frequency changes by $P \bullet f_{ref}$. If f_{ref} equals the desired channel spacing, then only every P channel may be programmed using this method. A problem remains: how to program intermediate channels.

One solution to this problem is shown in Figure 14.

FIGURE 14 – FREQUENCY SYNTHESIS BY PRESCALING



A ÷ P is placed in series with the desired channel spacing to give a reference frequency: channel spacing/P.

Another solution is found by considering the defining equation (1) for f_{out} of Figure 13. From the equation it may be seen that only every P channel can be programmed simply, because N is always an integer. To obtain intermediate channels, P must be multiplied by an integer plus a fraction. This fraction would be of the form: A/P. If N is defined to be an integer number, Np, plus a fraction, A/P, N may be expressed as:

$$N = Np + A/P.$$

Substituting this expression for N in equation 1 gives:

$$f_{out} = (Np + A/P) \bullet P \bullet f_{ref} \quad (2)$$

or:

$$f_{out} = (Np\ P + A) \bullet f_{ref} \quad (3)$$

$$f_{out} = Np \bullet P \bullet f_{ref} + A \bullet f_{ref}. \quad (4)$$

Equation 4 shows that all channels can be obtained directly if N can take on fractional values. Since it is difficult to multiply by a fractional number, equation 4 must be synthesized by some other means.

Taking equation 3 and adding ±AP to the coefficient of f_{ref}, the equation becomes:

$$f_{out} = (Np \bullet P + A + A \bullet P - A \bullet P)\ f_{ref}. \quad (5)$$

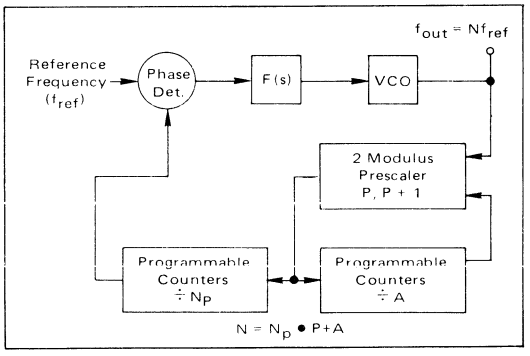
Collecting terms and factoring gives:

$$f_{out} = [(Np - A)\ P + A\ (P + 1)]\ f_{ref} \quad (6)$$

From equation 6 it becomes apparent that the fractional part of N can be synthesized by using a two-modulus counter (P and P + 1) and dividing by the upper modulus, A times, and the lower modulus (Np - A) times.

This equation (6) suggests the circuit configuration in Figure 15. The A counter shown must be the type that

FIGURE 15 – FREQUENCY SYNTHESIS BY TWO MODULUS PRESCALING



counts from the programmed state (A) to the enable state, and remains in this state until divide by Np is completed in the programmable counter.

In operation, the prescaler divides by P + 1, A times. For every P + 1 pulse into the prescaler, both the A counter and Np counter are decremented by 1. The prescaler divides by P + 1 until the A counter reaches the zero state. At the end of (P + 1) • A pulses, the state of the Np counter equals (Np - A). The modulus of the prescaler then changes to P. The variable modulus counter divides by P until the remaining count, (Np - A) in the Np counter, is decremented to zero. Finally, when this is completed, the A and Np counters are reset and the cycle repeats.

To further understand this prescaling technique, consider the case with P = 10. Equation 6 becomes:

$$f_{out} = (A + 10\ Np) \bullet f_{ref} \quad (7)$$

If Np consists of 2 decades of counters then:

$$Np = 10\ Np_0 + Np_1$$

(Np_0 is the most significant digit),

and equation 7 becomes:

FIGURE 16 – DIRECT PROGRAMMING UTILIZING TWO-MODULUS PRESCALER

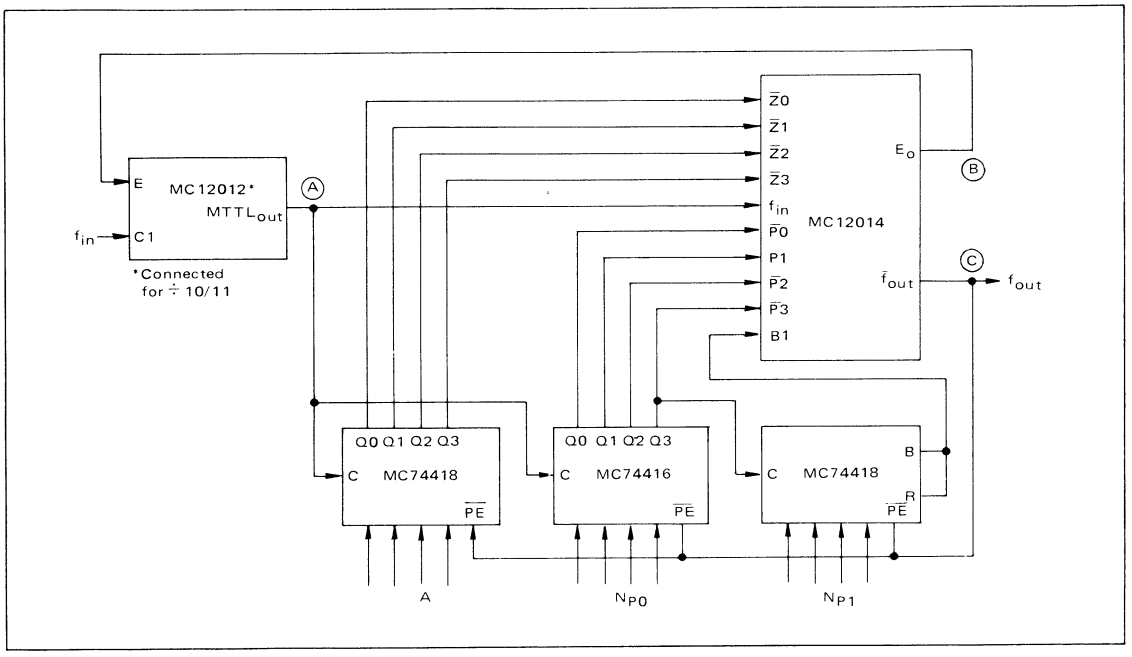


FIGURE 17 – WAVEFORMS FOR DIVIDE BY 43

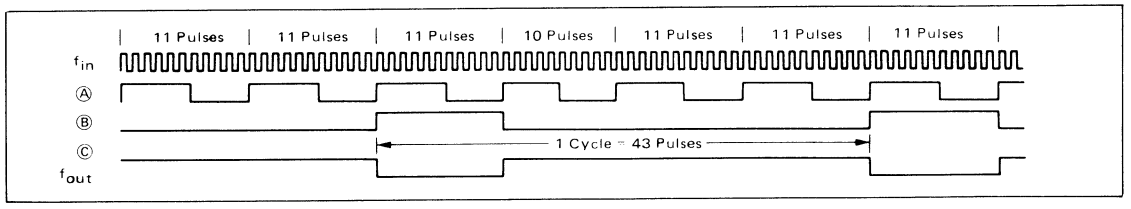


FIGURE 18 – WAVEFORMS FOR DIVIDE BY 42

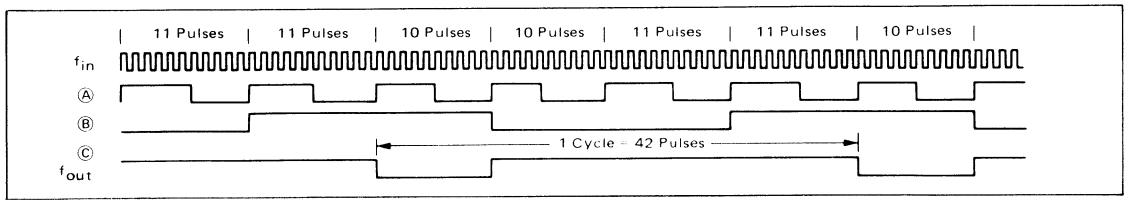
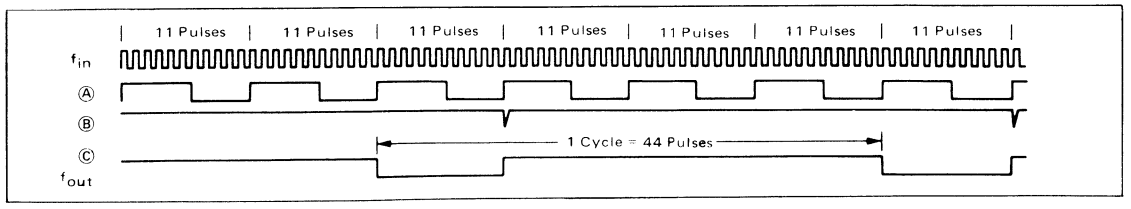


FIGURE 19 – WAVEFORMS FOR DIVIDE BY 44



$$f_{out} = (100\ N_{P0} + 10\ N_{P1} + A)\ f_{ref}.$$

To do variable modulus prescaling using the MC12012 and programmable divide by N counters (MC74416, MC74418, one additional part is required: the MC12014 (Counter Control Logic).

In variable modulus prescaling the MC12014 serves a dual purpose: it detects the terminal (zero) count of the A counter, to switch the modulus of the MC12012; and it extends the maximum operating frequency of the programmable counters to above 25 MHz. (See the MC12014 data sheet for a detailed description of the Counter Control Logic).

Figure 16 shows the method of interconnecting the MC12012, MC12014, and MC74416 (or MC74418) for variable modulus prescaling. To understand the operation of the circuit shown in Figure 16, consider division by 43. Division by 43 is done by programming $N_{P0} = 0$, $N_{P1} = 4$, and $A = 3$.

Waveforms for various points in the circuit are shown in Figure 17 for this division. From the waveforms it may be seen that the two-modulus prescaler starts in the divide by 11 mode, and the first input pulse causes point A to go high. This positive transition decrements the N_P counter to 3, and counter A to 2.

After 11 pulses, point Ⓐ again goes high; the N_P counter decrements to 2 and the A counter to 1. The "2" contained in the N_P counter enables the inputs to the frequency extender portion of the MC12014. After 11 more pulses point Ⓐ goes high again.

With this position transition at Ⓐ, the output (f_{out}) of the MC12014 goes low, the N_P counter goes to 1, and the A counter goes to 0. The zero state of the A counter is detected by the MC12014, causing point Ⓑ to go to 1 and changing the modulus of the MC12012 to 10 at the start of the cycle.

When f_{out} goes low, the programmable counters are reset to the programmed number. After 11 pulses (the enable went high after the start of the cycle and therefore doesn't change the modulus until the next cycle), point Ⓐ makes another positive transition. This positive transition causes f_{out} to return high, release the preset on the counter, and generates a pulse to clear the latch (return point Ⓑ to 0).

After 10 pulses the cycle begins again (point Ⓑ was high prior to point Ⓐ going high). The number of input pulses that have occured during this entire operation is: 11 + 11 + 11 + 10 = 43. Figures 18 and 19 show the waveforms for divide by 42 and divide by 44 respectively.

The variable modulus prescaling technique may be used in any application as long as the number in the N_P counter is greater than or equal to the number in the A counter. Failure to observe this rule will result in erroneous results. (For example, for the system shown in Figure 16 if the number 45 is programmed, the circuit actually will divide by 44. This is not a serious restriction since N_P is greater than A in most applications).

It is important to note that the A counter has been composed of only one counter for discussion only; where required, the A counter may be made as large as needed by cascading several programmable counters. Figure 20 shows the method of interconnecting counters. Operation is previously described. The number of stages in the A counter should not exceed the number of stages for the

FIGURE 20 – METHOD OF INTERCONNECTING COUNTERS

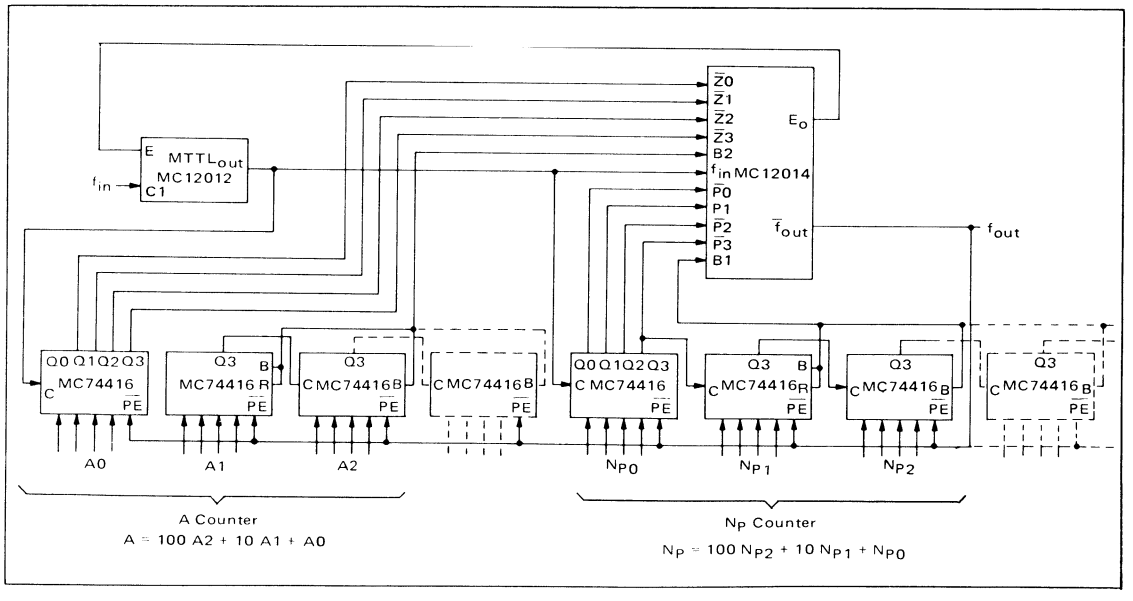


FIGURE 21 – DIRECT PROGRAMMING 100-200 MHz SYNTHESIZER IN 50 kHz STEPS

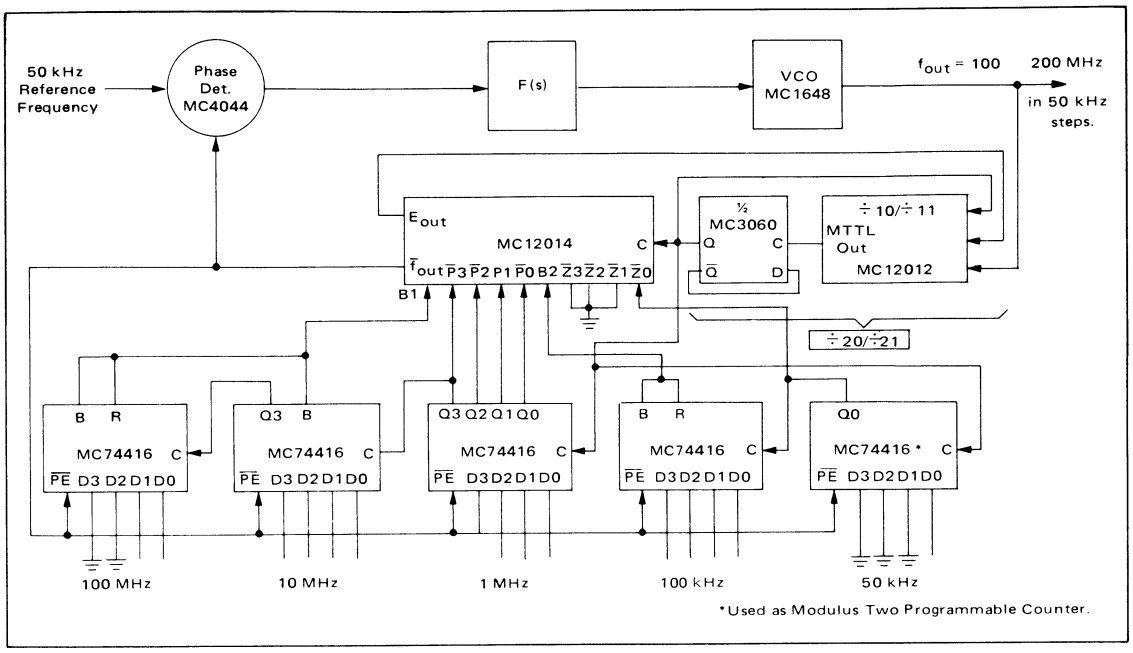
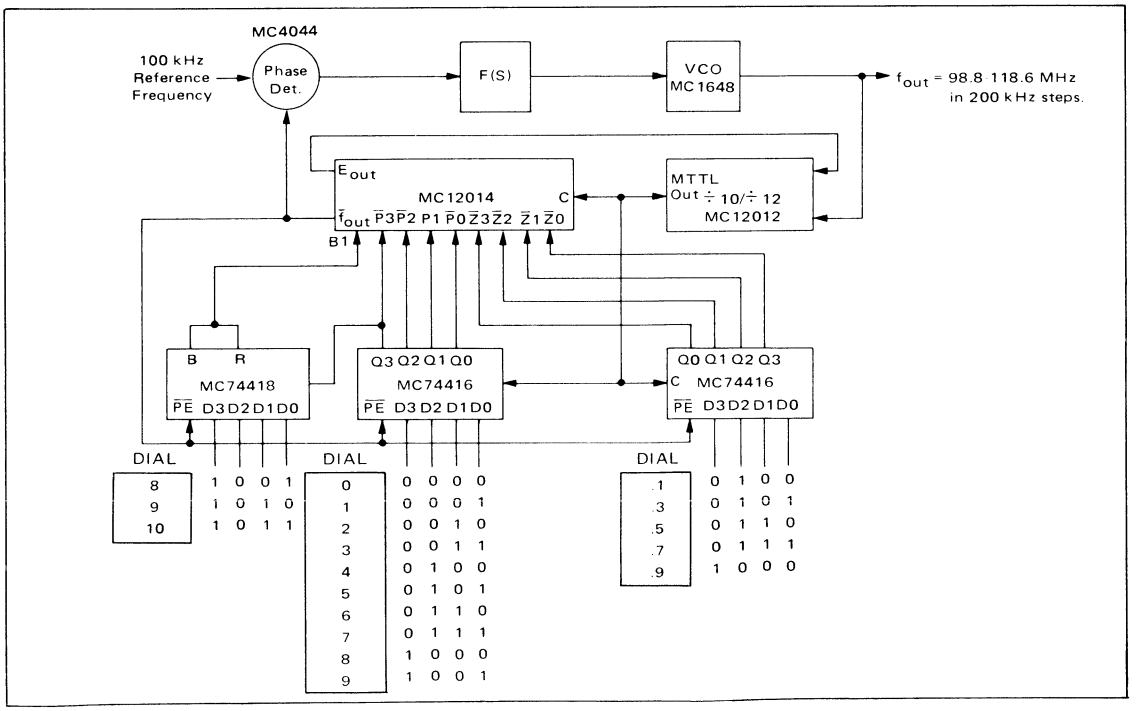


FIGURE 22 – FM BAND SYNTHESIZER WITH 10.7 MHz I.F. OFFSET



Np counters. As many counters as desired may be cascaded, as long as fan-in and fan-out rules for each part are observed.

The theory of "variable modulus prescaling" developed above, examined a case in which the upper modulus of the two-modulus prescaler was 1 greater than the lower modulus. However, the technique described is by no means limited to this one special case. There are applications in which it is desirable to use moduli other than P/(P + 1).

It can be shown that for a general case in which the moduli of the two-modulus prescaler are P and P + M, equation 6 becomes:

$$f_{out} = [(Np - A)\,P + A\,(P + M)] \bullet f_{ref}$$

or

$$f_{out} = [Np \bullet P + M \bullet A] \bullet f_{ref}. \qquad (8)$$

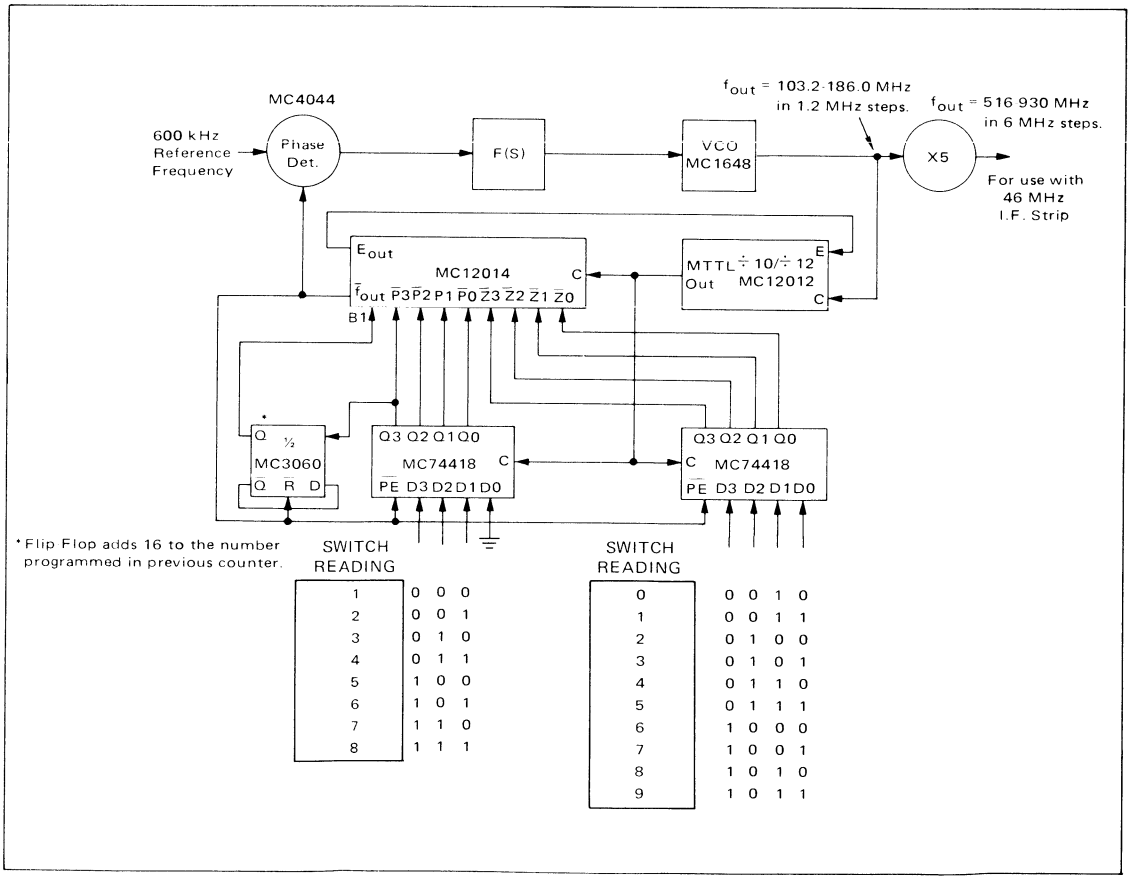
From equation 8 it may be seen that the upper modulus of the two-modulus prescaler has no effect on the Np counter, and that the number programmed in the A counter is simply multiplied by M.

APPLICATIONS

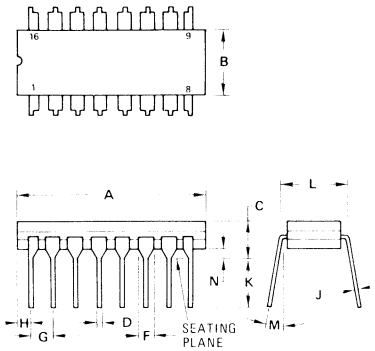
There is no one procedure which will always yield the best counter configuration for all possible MC12012 applications. Each designer will develop his own special design for the counter portion of his PLL system.

An insight into some of the various possible counter schemes may be obtained by considering the various PLL systems shown in Figures 21, 22, and 23. These examples were chosen to show some of the moduli that may be obtained by using the MC12012.

FIGURE 23 – UHF SYNTHESIZER USING 10/12 COUNTER



OUTLINE DIMENSIONS



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.99	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.31	0.008	0.012
K	3.18	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15^0	–	15^0
N	0.51	1.02	0.020	0.040

CASE 620

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE
2. AT MAXIMUM MATERIAL CONDITION.
   PKG. INDEX: NOTCH IN LEAD
   NOTCH IN CERAMIC OR INK DOT.
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

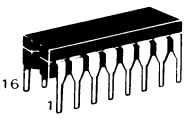
TWO-MODULUS PRESCALER

MC12013
MC12513

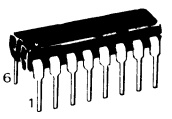
ISSUE

Advance Information

The MC12013/MC12513 is a two-modulus prescaler which will divide by 10 and 11. A MECL-to-MTTL translator is provided to interface directly with the MC12014 Counter Control Logic. In addition, the MC12013/MC12513 provides a buffered clock input and MECL bias voltage source. Details of operation are on the MC12012 data sheet.



L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

- 600 MHz (typ) Toggle Frequency
- ÷10/11
- MECL to MTTL Translator on Chip
- MECL and MTTL Enable Inputs
- +5.0 or -5.2 V Operation*
- Buffered Clock Input
- V_{BB} Reference Voltage
- 310 Milliwatts (typ)

*When using +5.0 V supply, apply +5.0 V to pin 1 (V_{CCO}), pin 6 (MTTL V_{CC}), pin 16 (V_{CC}), and ground pin 8 (V_{EE}). When using -5.2 V supply, ground pin 1 (V_{CCO}), pin 6 (MTTL V_{CC}), and pin 16 (V_{CC}) and apply -5.2 V to pin 8 (V_{EE}). If the translator is not required, pin 6 may be left open to conserve dc power drain.

PIN ASSIGNMENT

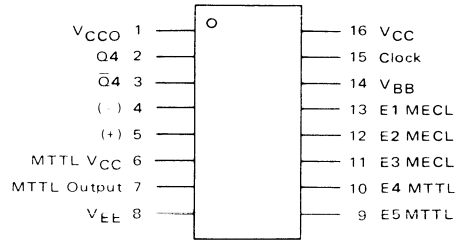


FIGURE 1 – LOGIC DIAGRAM

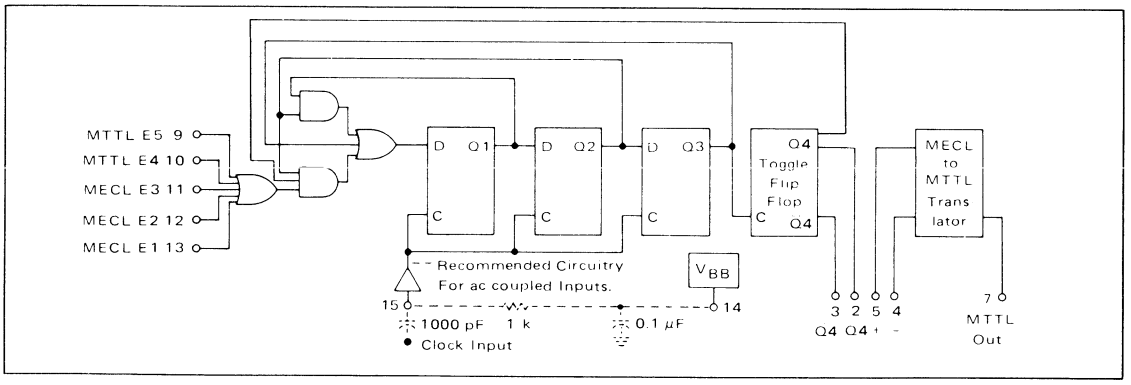
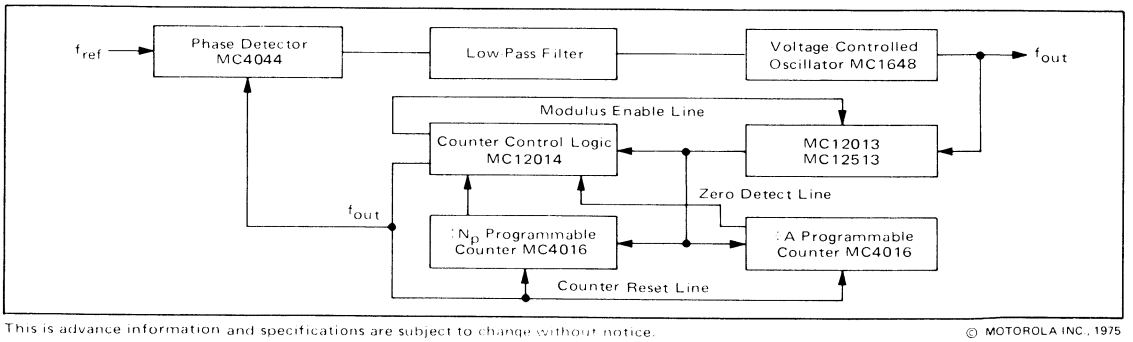


FIGURE 2 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Ratings above which device life may be impaired.			
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8.0	Vdc
Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{ILmin}	Vdc
Output Source Current	I_O		mAdc
Continuous		-50	
Surge		-100	
Storage Temperature Range	T_{stg}	-65 to +175	°C
Recommended maximum ratings above which performance may be degraded			
Operating Temperature Range	T_A	-30 to +85	°C
DC Fan-Out* (Gates and Flip-Flops)	n	70	--

*AC fan-out is limited by desired system performance.

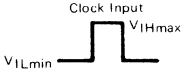
ELECTRICAL CHARACTERISTICS
Supply Voltage -5.2 V

The MC12013 has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50-ohm resistor to -2.0 Vdc.

@Test Temperature	TEST VOLTAGE/CURRENT VALUES: Volts V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{EE}	mA I_L	I_{OL}	I_{OH}
-30°C	-0.890	-1.990	-1.205	-1.500	-2.8	-4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40
+25°C	-0.810	-1.950	-1.105	-1.475	-2.8	-4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40
+85°C	-0.700	-1.925	-1.035	-1.440	-2.8	-4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40

Characteristic	Symbol	Pin Under Test	MC12013 -30°C Min	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}	Gnd
Power Supply Drain Current	I_{CC1}	8			-80	-62				mAdc									8				1,16
	I_{CC2}	6					5.2			mAdc	4	5							8				6
Input Current	I_{INH1}	15					250			μAdc	15								8				1,16
		11									11												
		12									12												
		13									13												
	I_{INH2}	4			2.0		5.0			mAdc	5	4							8				6
		5			2.0		5.0			mAdc	5	4							8				6
	I_{INH3}	5			1.0		2.5			mAdc	4	5							8				6
	I_{INH4}	9					100			μAdc					9				8				1,16
		10					100			μAdc					10				8				1,16
Leakage Current	I_{INL1}	15			-10					μAdc									8,15				1,16
		11																	8,11				
		12																	8,12				
		13																	8,13				
	I_{INL2}	9	-1.6		-1.6			-1.6		mAdc									8				1,16
		10	-1.6		-1.6			-1.6		mAdc									8				1,16
Reference Voltage	V_{BB}	14			-1.360		-1.160			Vdc									8	14			1,16
Logic "1" Output Voltage	V_{OH1} ①	2	-1.100	-0.890	-1.000		-0.810	-0.930	-0.700	Vdc		11,12,13				9,10			8				1,16
		3	-1.100	-0.890	-1.000		-0.810	-0.930	-0.700	Vdc		11,12,13				9,10			8				1,16
	V_{OH2}	7	-2.8		-2.6			-2.4		Vdc	5	4							8			7	6
Logic "0" Output Voltage	V_{OL1} ①	2	-1.990	-1.675	-1.950		-1.650	-1.925	-1.615	Vdc		11,12,13				9,10			8				1,16
		3	-1.990	-1.675	-1.950		-1.650	-1.925	-1.615	Vdc		11,12,13				9,10			8				1,16
	V_{OL2}	7		-4.26			-4.40		-4.48	Vdc	4	5							8		7		6
Logic "1" Threshold Voltage ②	V_{OHA}	2	-1.120		-1.020			-0.950		Vdc			11,12,13			9,10			8				1,16
		3	-1.120		-1.020			-0.950		Vdc			11,12,13			9,10			8				1,16
Logic "0" Threshold Voltage ③	V_{OLA}	2		-1.655			-1.630		-1.595	Vdc				11,12,13				9,10	8				1,16
		3		-1.655			-1.630		-1.595	Vdc				11,12,13				9,10	8				1,16
Short Circuit Current	I_{OS}	7	-65	-20	-65		-20	-65	-20	mAdc	5	4				7			8				6

① Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.
② In addition to meeting the output levels specified, the device must divide by 10 during this test. The clock input is the waveform shown.
③ In addition to meeting the output levels specified, the device must divide by 11 during this test. The clock input is the waveform shown.



ELECTRICAL CHARACTERISTICS

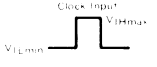
Supply Voltage +5.0 V

The MC12513 has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 100-ohm resistor to +3.0 Vdc.

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES												
	Volts									mA			
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}	
-55°C	+4.120	+3.040	+3.745	+3.500	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40	
+25°C	+4.220	+3.110	+3.895	+3.525	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40	
+125°C	+4.370	+3.140	+4.000	+3.560	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40	

Characteristic	Symbol	Pin Under Test	MC12513 -55°C Min	MC12513 -55°C Max	MC12513 +25°C Min	MC12513 +25°C Typ	MC12513 +25°C Max	MC12513 +125°C Min	MC12513 +125°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}	(V_{EE}) Gnd
Power Supply Drain Current	I_{CC1}	8			-80	-62				mAdc									1,16				8
	I_{CC2}	6					5.2			mAdc	4	5							6				8
Input Current	I_{INH1}	15					250			μAdc	15								1,16				8
		11									11												
		12									12												
		13									13												
	I_{INH2}	4			2.0		5.0			mAdc	4,5								6				8
		5			2.0		5.0			mAdc	4,5								6				8
	I_{INH3}	5			1.0		2.5			mAdc	4	5							6				8
	I_{INH4}	9					100			μAdc					9				1,16				8
		10					100			μAdc					10				1,16				8
Leakage Current	I_{INL1}	15			-10					μAdc									1,16				8,15
		11																					8,11
		12																					8,12
		13																					8,13
	I_{INL2}	9	-1.6		-1.6			-1.6		mAdc						9			1,16				8
		10	-1.6		-1.6			-1.6		mAdc						10			1,16				8
Reference Voltage	V_{BB}	14			3.67		3.87			Vdc									1,16	14			8
Logic "1" Output Voltage	V_{OH1} ①	2	3.880	4.120	4.030		4.220	4.135	4.370	Vdc		11,12,13				9,10			1,16				8
		3	3.880	4.120	4.030		4.220	4.135	4.370	Vdc		11,12,13				9,10			1,16				8
	V_{OH2}	7	2.4		2.7			3.0		Vdc	5	4							6			7	8
Logic "0" Output Voltage	V_{OL1} ①	2	3.040	3.405	3.110		3.440	3.140	3.515	Vdc		11,12,13				9,10			1,16				8
		3	3.040	3.405	3.110		3.440	3.140	3.515	Vdc		11,12,13				9,10			1,16				8
	V_{OL2}	7		1.00			0.80		0.66	Vdc	4	5							6		7		8
Logic "1" Threshold Voltage	V_{OHA} ②	2	3.860		4.010			4.115		Vdc			11,12,13				9,10		1,16				8
		3	3.860		4.010			4.115		Vdc			11,12,13				9,10		1,16				8
Logic "0" Threshold Voltage	V_{OLA} ③	2		3.425			3.460		3.535	Vdc				11,12,13				9,10	1,16				8
		3		3.425			3.460		3.535	Vdc				11,12,13				9,10	1,16				8
Short Circuit Current	I_{OS}	7	-65	-20	-65		-20	-65	-20	mAdc	5	4				7			6				8

① Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.
② In addition to meeting the output levels specified, the device must divide by 10 during this test. The clock input is the waveform shown.
③ In addition to meeting the output levels specified, the device must divide by 11 during this test. The clock input is the waveform shown.



MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Ratings above which device life may be impaired:			
Power Supply Voltage (V_{CC} = 0)	V_{EE}	-8.0	Vdc
Input Voltage (V_{CC} = 0)	V_{in}	0 to V_{ILmin}	Vdc
Output Source Current Continuous Surge	I_O	 - 50 - 100	mAdc
Storage Temperature Range	T_{stg}	-65 to +175	°C
Recommended maximum ratings above which performance may be degraded:			
Operating Temperature Range	T_A	-55 to +125	°C
DC Fan-Out* (Gates and Flip-Flops)	n	70	–

*AC fan-out is limited by desired system performance.

ELECTRICAL CHARACTERISTICS

Supply Voltage -5.2 V

The MC12513 has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 100-ohm resistor to -2.0 Vdc.

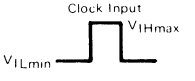
	TEST VOLTAGE/CURRENT VALUES											
	Volts									mA		
@Test Temperature	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}
-55°C	-0.880	-2.020	-1.255	-1.500	-2.8	-4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40
+25°C	-0.780	-1.950	-1.105	-1.475	-2.8	-4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40
+125°C	-0.630	-1.920	-1.000	-1.400	-2.8	-4.7	-3.2	-4.4	-5.2	-0.25	16	-0.40

			MC12513								TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:											
		Pin Under	-55°C		+25°C			+125°C														
Characteristic	Symbol	Test	Min	Max	Min	Typ	Max	Min	Max	Unit	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{EE}	I_L	I_{OL}	I_{OH}	Gnd
Power Supply Drain Current	I_{CC1}	8	–	–	-80	-62		–	–	mAdc	–	–	–	–	–	–	–	–	8	–	–	–	1,16
	I_{CC2}	6	–	–	–	–	5.2	–	–	mAdc	4	5	–	–	–	–	–	–	8	–	–	–	6
Input Current	I_{INH1}	15	–	–	–	–	250			μAdc	15	–	–	–	–	–	–		8	–	–	–	1,16
		11	–	–	–	–	↓	–	–	↓	11	–	–	–	–	–	–	–	↓	–	–	–	↓
		12	–	–		–		–	–		12	–	–	–	–	–	–	–		–	–	–	
		13	–	–	–	–		–	–		13	–	–	–	–	–	–	–		–	–	–	
	I_{INH2}	4	–	–	2.0	–	5.0	–	–	mAdc	5	4		–	–	–	–	–	8	–	–	–	6
		5	–	–	2.0	–	5.0	–	–	mAdc	5	4	–	–	–	–	–	–	8	–	–	–	6
	I_{INH3}	5	–	–	1.0	–	2.5	–	–	mAdc	4	5	–	–	–	–	–	–	8		–	–	6
	I_{INH4}	9	–	–	–	–	100	–	–	μAdc	–	–	–	–	9	–	–	–	8	–	–	–	1,16
		10	–	–	–	–	100	–	–	μAdc	–	–	–	–	10	–	–	–	8	–	–	–	1,16
Leakage Current	I_{INL1}	15	–	–	-10	–	–	–	–	μAdc	–	–	–	–	–	–	–	–	8,15	–	–	–	1,16
		11	–	–	↓	–	–	–	–	↓	–	–	–	–	–	–	–	–	8,11	–	–	–	↓
		12	–	–		–	–	–	–		–	–	–	–	–	–	–	–	8,12	–	–	–	
		13	–	–	–	–	–	–	–		–	–	–	–	–	–	–	–	8,13	–	–	–	
	I_{INL2}	9	-1.6	–	-1.6	–		-1.6	–	mAdc	–	–	–	–	–	9	–	–	8	–	–	–	1,16
		10	-1.6	–	-1.6	–		-1.6	–	mAdc	–	–	–	–	–	10	–	–	8	–	–	–	1,16
Reference Voltage	V_{BB}	14	–	–	-1.360	–	-1.160	–	–	Vdc	–	–	–	–	–	–	–	–	8	14	–	–	1,16
Logic "1" Output Voltage	V_{OH1}	2	-1.120	-0.880	-0.970	–	-0.780	-0.865	-0.630	Vdc	–	11,12,13	–	–	–	9,10	–	–	8	–	–	–	1,16
	①	3	-1.120	-0.880	-0.970	–	-0.780	-0.865	-0.630	Vdc	–	11,12,13	–	–	–	9,10	–	–	8	–	–	–	1,16
	V_{OH2}	7	-2.8	–	-2.5	–	–	-2.2	–	Vdc	5	4	–	–	–	–	–	–	8	–	–	7	6
Logic "0" Output Voltage	V_{OL1}	2	-2.020	-1.655	-1.950	–	-1.620	-1.920	-1.545	Vdc	–	11,12,13	–	–	–	9,10	–	–	8	–	–	–	1,16
	①	3	-2.020	-1.655	-1.950	–	-1.620	-1.920	-1.545	Vdc	–	11,12,13	–	–	–	9,10	–	–	8	–	–	–	1,16
	V_{OL2}	7	–	-4.20	–	–	-4.40	–	-4.54	Vdc	4	5	–	–	–	–	–	–	8	–	7	–	6
Logic "1" Threshold Voltage	V_{OHA}	2	-1.140	–	-0.990	–	–	-0.885	–	Vdc	–	–	11,12,13	–	–	–	9,10	–	8	–	–	–	1,16
	②	3	-1.140	–	-0.990	–	–	-0.885	–	Vdc	–	–	11,12,13	–	–	–	9,10	–	8	–	–	–	1,16
Logic "0" Threshold Voltage	V_{OLA}	2	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	–	11,12,13	–	–	–	9,10	8	–	–	–	1,16
	③	3	–	-1.635	–	–	-1.600	–	-1.525	Vdc	–	–	–	11,12,13	–	–	–	9,10	8	–	–	–	1,16
Short Circuit Current	I_{OS}	7	-65	-20	-65	–	-20	-65	-20	mAdc	5	4	–	–	–	7	–	–	8	–	–	–	6

① Test outputs of the device must be tested by sequencing through the truth table. All input, power supplya nd ground voltages must be maintained between tests. The clock input is the waveform shown.

② In addition to meeting the output levels specified, the device must divide by 10 during this test. The clock input is the waveform shown.

③ In addition to meeting the output levels specified, the device must divide by 11 during this test. The clock input is the waveform shown.



ELECTRICAL CHARACTERISTICS

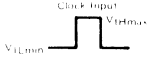
Supply Voltage +5.0 V

The MC12013 has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50-ohm resistor to +3.0 Vdc.

@ Test Temperature	TEST VOLTAGE/CURRENT VALUES											
	Volts									mA		
	V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}
-30°C	+4.110	+3.070	+3.795	+3.500	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40
+25°C	+4.190	+3.110	+3.895	+3.525	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40
+85°C	+4.300	+3.135	+3.965	+3.560	+2.4	+0.5	+2.0	+0.8	+5.0	-0.25	16	-0.40

Characteristic	Symbol	Pin Under Test	MC12013 -30°C Min	MC12013 -30°C Max	MC12013 +25°C Min	MC12013 +25°C Typ	MC12013 +25°C Max	MC12013 +85°C Min	MC12013 +85°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW: V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IH}	V_{IL}	V_{IHT}	V_{ILT}	V_{CC}	I_L	I_{OL}	I_{OH}	(V_{EE}) Gnd
Power Supply Drain Current	I_{CC1}	8			-80	-62				mAdc									1,16				8
	I_{CC2}	6					52			mAdc	4	5							6				8
Input Current	I_{INH1}	15					250			μAdc	15								1,16				8
		11					↓			↓	11								↓				↓
		12									12												
		13									13												
	I_{INH2}	4			20		50			mAdc	4.5	–	–						6				8
		5			20		50			mAdc	4.5	–	–						6				8
	I_{INH3}	5			10		25			mAdc	4	5							6				8
	I_{INH4}	9					100			μAdc					9				1,16				8
		10					100			μAdc					10				1,16				8
Leakage Current	I_{INL1}	15			-10					μAdc		–							1,16				8,15
		11			↓					↓									↓				8,11
		12																					8,12
		13																					8,13
	I_{INL2}	9	-1.6		-1.6			-1.6		mAdc						9			1,16				8
		10	-1.6		-1.6			-1.6		mAdc						10			1,16				8
Reference Voltage	V_{BB}	14			3.67		3.87			Vdc									1,16	14			8
Logic "1" Output Voltage	V_{OH1} ①	2	3.900	4.110	4.000		4.190	4.070	4.300	Vdc		11,12,13				9,10			1,16				8
		3	3.900	4.110	4.000		4.190	4.070	4.300	Vdc		11,12,13				9,10			1,16				8
	V_{OH2}	7	2.4		2.6			2.8		Vdc	5	4							6			7	8
Logic "0" Output Voltage	V_{OL1} ①	2	3.070	3.385	3.110		3.410	3.135	3.445	Vdc		11,12,13				9,10			1,16				8
		3	3.070	3.385	3.110		3.410	3.135	3.445	Vdc		11,12,13				9,10			1,16				8
	V_{OL2}	7		0.94			0.80		0.72	Vdc	4	5							6		7		8
Logic "1" Threshold Voltage	V_{OHA} ②	2	3.880		3.980			4.050		Vdc			11,12,13				9,10		1,16				8
		3	3.880		3.980			4.050		Vdc			11,12,13				9,10		1,16				8
Logic "0" Threshold Voltage	V_{OLA} ③	2		3.405			3.430		3.465	Vdc				11,12,13				9,10	1,16				8
		3		3.405			3.430		3.465	Vdc				11,12,13				9,10	1,16				8
Short Circuit Current	I_{OS}	7	-65	-20	-65		-20	-65	-20	mAdc	5	4				7			6				8

① Test outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests. The clock input is the waveform shown.
② In addition to meeting the output levels specified, the device must divide by 10 during this test. The clock input is the waveform shown.
③ In addition to meeting the output levels specified, the device must divide by 11 during this test. The clock input is the waveform shown.



SWITCHING CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC12013 -30°C Min	-30°C Typ	-30°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Typ	+85°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse Gen. 1	Pulse Gen. 2	Pulse Gen. 3	V_{IHmin} †	V_{ILmin} †	V_F -3.0 V	V_{EE} -3.0 V	V_{CC} +2.0
Propagation Delay (See Figures 3 and 5)	t_{15+2+}	2					5.3	8.1				ns	15				11,12,13	9,10	8	1,6,16
	t_{15+2-}	2					5.0	7.5					15				11,12,13	9,10	8	1,6,16
	t_{5+7+}	7					5.7	8.1					A						8	1,6,16
	t_{5-7-}	7					4.1	6.5					A						8	1,6,16
Setup Time (See Figures 4 and 5)	t_{setup1}	11				5.0	1.5					ns	15	*			*	9,10	8	1,6,16
	t_{setup2}	9				5.0	2.0					ns	15		*		11,12,13	*	8	1,6,16
Release Time (See Figures 4 and 5)	t_{rel1}	11				5.0	1.5					ns	15	*			*	9,10	8	1,6,16
	t_{rel2}	9				5.0	2.0					ns	15		*		11,12,13	*	8	1,6,16
Toggle Frequency (Figure 6 11)	f_{max}	2		600		550	600			550		MHz				11			8	16

*Test inputs sequentially, with Pulse Generator 2 or 3 as indicated connected to input under test, and the voltage indicated applied to the other input(s) of the same type (i.e., MECL or MTTL).

†	-30°C	+25°C	+85°C	
V_{IHmin}	+1.03	+1.115	+1.20	Vdc
† V_{ILmin}	+0.175	+0.200	+0.235	Vdc

SWITCHING CHARACTERISTICS

Characteristic	Symbol	Pin Under Test	MC12513 -55°C Min	-55°C Typ	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Typ	+125°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse Gen. 1	Pulse Gen. 2	Pulse Gen. 3	V_{IHmin} †	V_{ILmin} †	V_F -3.0 V	V_{EE} -3.0 V	V_{CC} +2.0
Propagation Delay (See Figures 3 and 5)	t_{15+2+}	2					5.3	8.1				ns	15				11,12,13	9,10	8	1,6,16
	t_{15+2-}	2					5.0	7.5					15				11,12,13	9,10	8	1,6,16
	t_{5+7+}	7					5.7	8.1					A						8	1,6,16
	t_{5-7-}	7					4.1	6.5					A						8	1,6,16
Setup Time (See Figures 4 and 5)	t_{setup1}	11				5.0	1.5					ns	15	*			*	9,10	8	1,6,16
	t_{setup2}	9				5.0	2.0					ns	15		*		11,12,13	*	8	1,6,16
Release Time (See Figures 4 and 5)	t_{rel1}	11				5.0	1.5					ns	15	*			*	9,10	8	1,6,16
	t_{rel2}	9				5.0	2.0					ns	15		*		11,12,13	*	8	1,6,16
Toggle Frequency (Figure 6 11)	f_{max}	2		600		550	600			550		MHz				11			8	16

*Test inputs sequentially, with Pulse Generator 2 or 3 as indicated connected to input under test, and the voltage indicated applied to the other input(s) of the same type (i.e., MECL or MTTL).

†	-55°C	+25°C	+125°C	
V_{IHmin}	+1.02	+1.15	+1.27	Vdc
† V_{ILmin}	+0.165	+0.215	+0.260	Vdc

FIGURE 3 – AC VOLTAGE WAVEFORMS

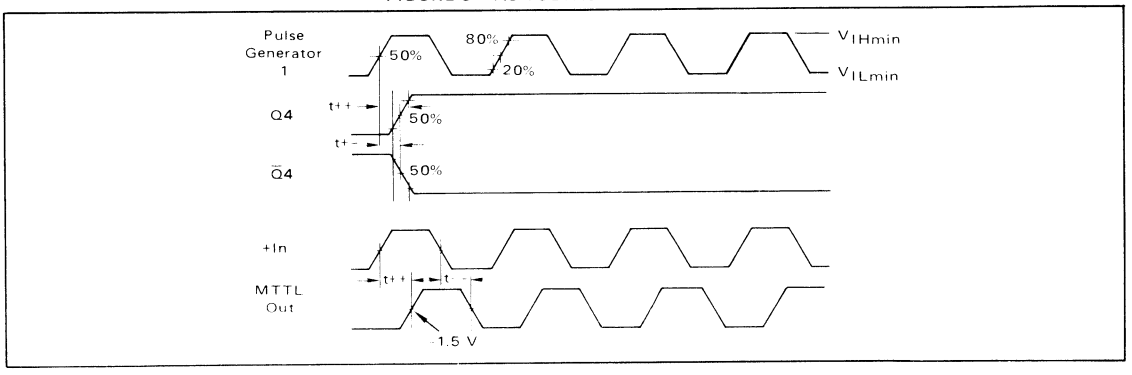


FIGURE 4 – SETUP AND RELEASE TIME WAVEFORMS

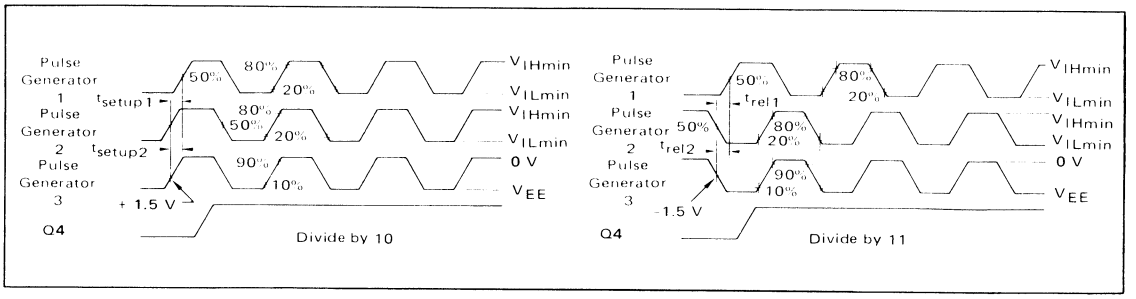


FIGURE 5 – AC TEST CIRCUIT

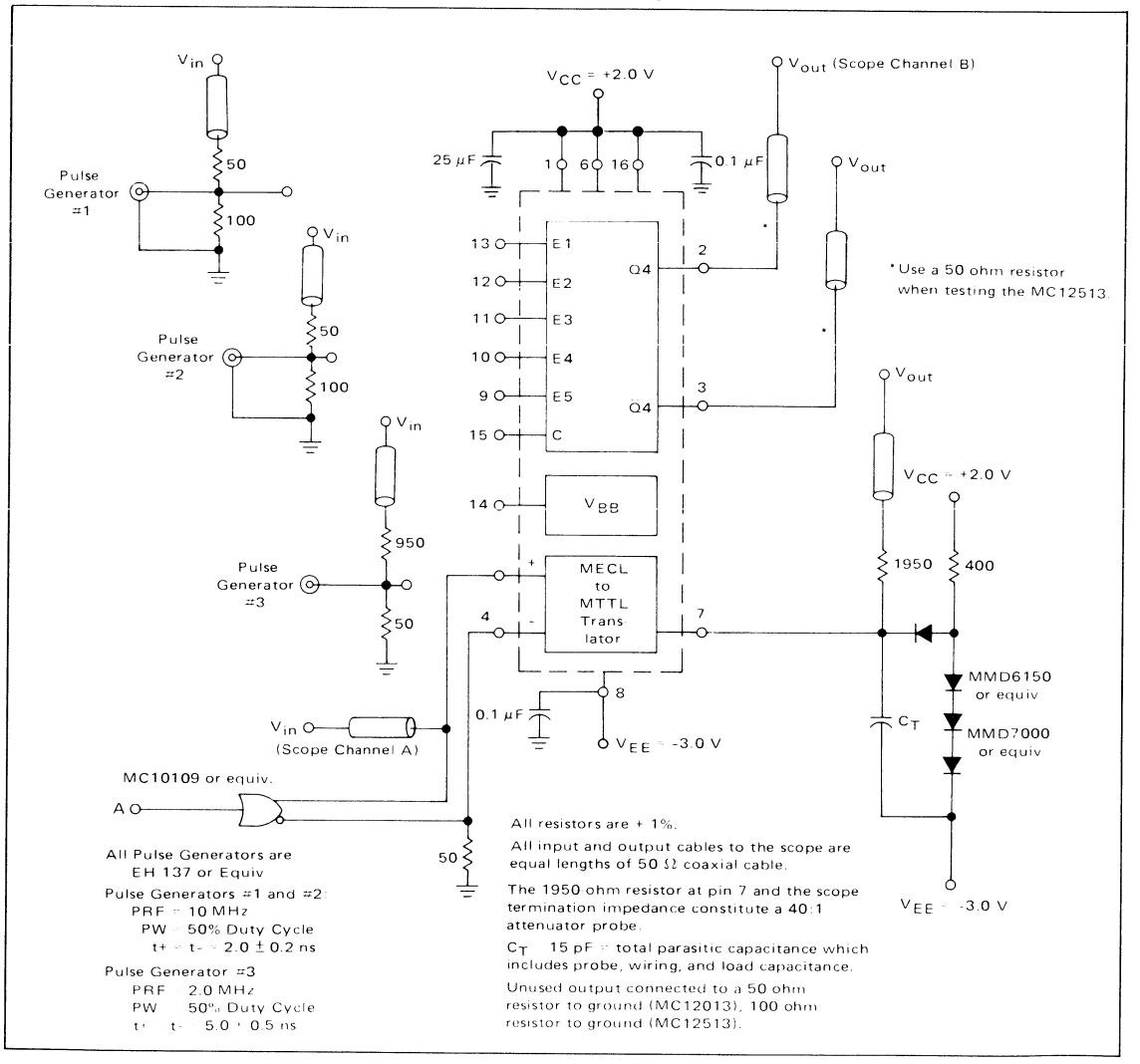


FIGURE 6 – MAXIMUM FREQUENCY TEST CIRCUIT (÷ 11)

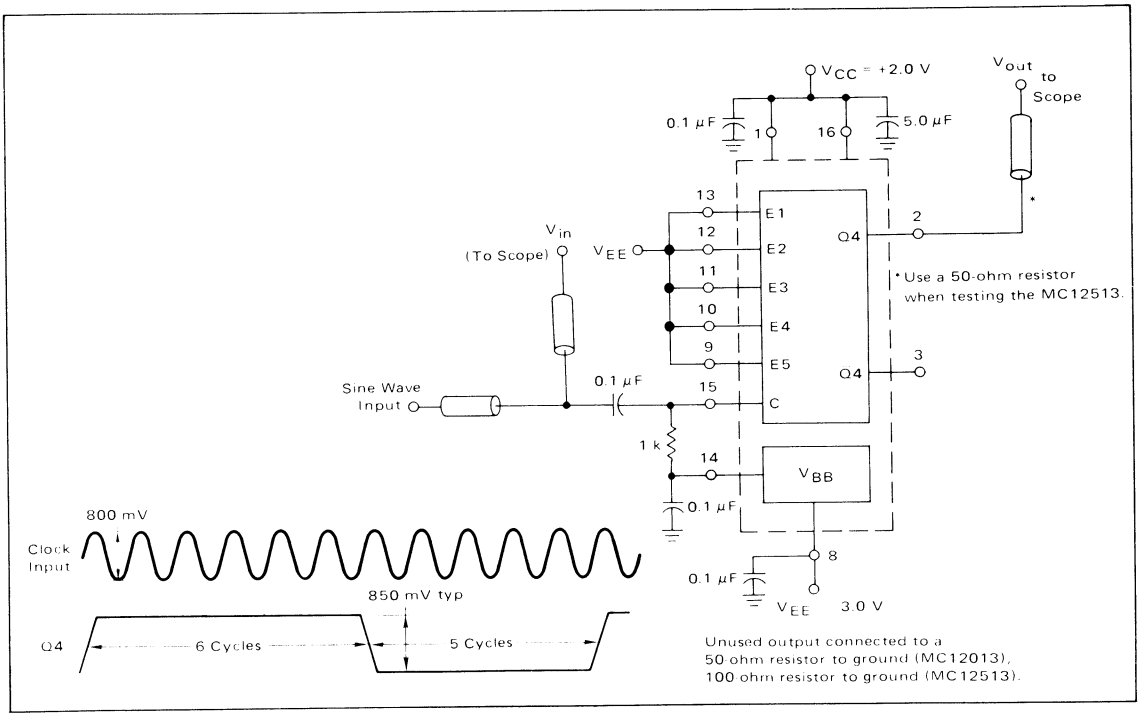
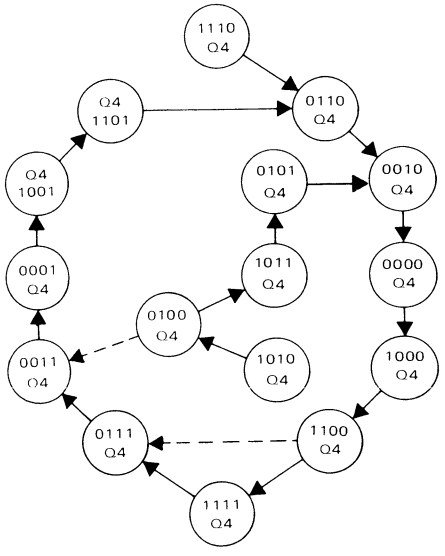


FIGURE 7 – STATE DIAGRAM

Q1	Q2	Q3	Q4
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
1	0	0	1
1	1	0	1
0	1	1	0
0	0	1	0
0	0	0	0
1	0	0	0
1	1	0	0

Enable 0

Enable 1



NOTES:

Enable 1.

The State of the Enable is important only for the positive Clock Transition when the counter is in state 1100.

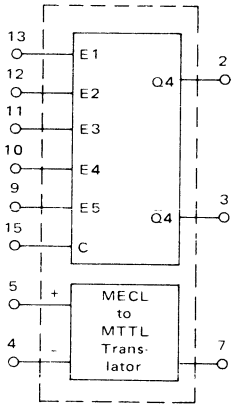
APPLICATIONS INFORMATION

The primary application of the MC12013/MC12513 is as a high speed variable modulus prescaler in the divide by N section of a phase locked loop synthesizer used as the local oscillator of two way radios. The theory and advantages of variable modulus prescaling, along with typical applications, are covered in detail on the data sheet for the MC12012.

Proper VHF termination techniques should be followed when the clock is separated from the prescaler by any appreciable distance.

In its basic form, the MC12013/MC12513 will divide by 10 or 11. Division by 10 occurs when anyone or all of the five gate inputs E1 through E5 are high. Division by 11 occurs when all inputs E1 through E5 are low. (Unconnected MTTL inputs are normally high, unconnected MECL inputs are normally low.) With the addition of extra parts, many different division configurations may be obtained (20/21, 40/41, 50/51, 100/101, etc.). A few of the many configurations are shown below.

FIGURE 8 – ÷ 10/11

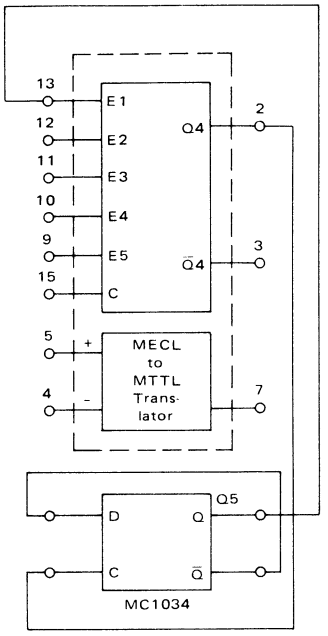


Q1	Q2	Q3	Q4
1	1	1	1
0	1	1	1
0	0	1	1
0	0	0	1
1	0	0	1
1	1	0	1
0	1	1	0
0	0	1	0
0	0	0	0
1	0	0	0
1	1	0	0

Enable = 0

Enable = 1

FIGURE 9 – ÷ 20/21



COUNT	Q1	Q2	Q3	Q4	Q4
31	1	1	1	1	1
30	0	1	1	1	1
28	0	0	1	1	1
24	0	0	0	1	1
25	1	0	0	1	1
27	1	1	0	1	1
22	0	1	1	0	1
20	0	0	1	0	1
16	0	0	0	0	1
17	1	0	0	0	1
19	1	1	0	0	1
14	0	1	1	1	0
12	0	0	1	1	0
8	0	0	0	1	0
9	1	0	0	1	0
11	1	1	0	1	0
6	0	1	1	0	0
4	0	0	1	0	0
0	0	0	0	0	0
1	1	0	0	0	0
3	1	1	0	0	0

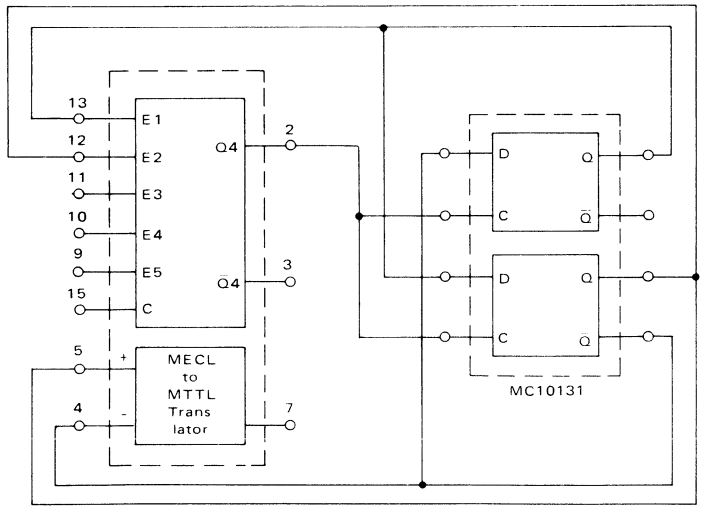
E2 + E3 + E4 + E5 = 0

E2 + E3 + E4 + E5 = 1

To obtain an MTTL output, connect pins 5 and 4 to pins 2 and 3 respectively. Termination resistors for the MECL outputs are not shown, but are required except for the flip-flop driving the translator section.

The ÷ 20/21 counter may also be built using an MTTL flip-flop by connecting pins 5 and 4 to pins 2 and 3 respectively, and driving the MTTL flip-flop with pin 7. MC12013 inputs E4 and E5 are used rather than E1 With E1 + E2 + E3 = 0, operation remains as shown.

FIGURE 10 – ÷ 40/41



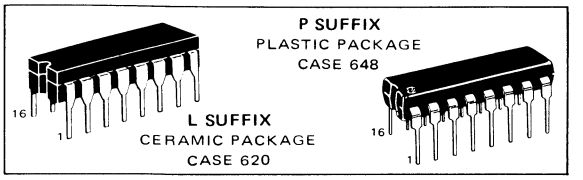
For ÷ 40: E4 + E5 = 1
For ÷ 41: E4 + E5 = 0

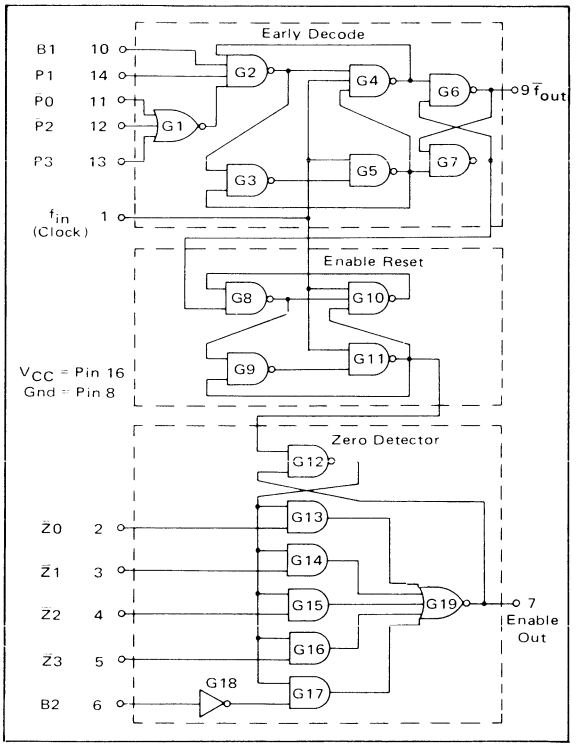
Termination resistors for MECL outputs are not shown, but are required except for the flip-flop driving the translator section.

COUNTER CONTROL LOGIC

MC12014
MC12514

The MC12014/MC12514 monolithic counter control logic unit is designed for use with the MC12012 Two-Modulus Prescaler and the MC4016 Programmable Counter to accomplish direct high-frequency programming. The MC12014/MC12514 consists of a zero detector which controls the modulus of the MC12012, and an early decode function which controls the MC4016. The early decode feature also increases the useful frequency range of the MC4016 from 8.0 MHz to 25 MHz.

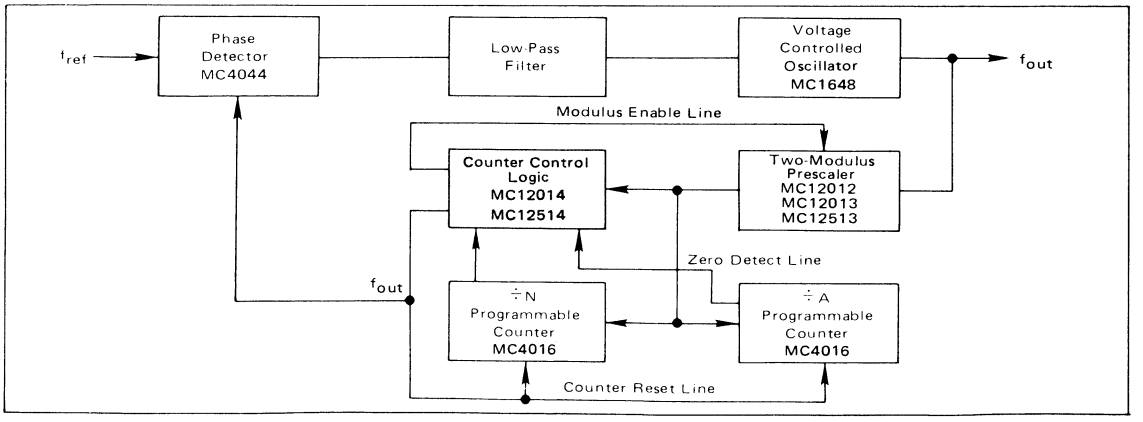




MAXIMUM RATINGS

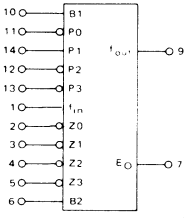
Rating	Symbol	Unit
Supply Operating Voltage Range	4.75 to 5.25	Vdc
Supply Voltage	+7.0	Vdc
Input Voltage	+5.5	Vdc
Output Voltage	+5.5	Vdc
Operating Temperature Range	0 to +75	°C
Storage Temperature Range	-65 to +150	°C
Maximum Junction Temperature	+150	°C
Thermal Resistance - Junction to Case (θ_{JC})	0.05	°C/mW
Thermal Resistance - Junction to Ambient (θ_{JA})	0.15	°C/mW

FIGURE 1 – TYPICAL FREQUENCY SYNTHESIZER APPLICATION



ELECTRICAL CHARACTERISTICS

Test procedures are shown for the f_{in}, $\overline{Z}0$, B1 and P1 inputs. All other inputs are tested in the same manner as the $\overline{Z}0$ input.



	TEST CURRENT/VOLTAGE VALUES (All Temperatures)									
	mA			Volts						
	I_{OL}	I_{OH}	I_{IC}	V_{IL}	V_{IH}	V_{IHH}	V_{RH}	V_{CC}	V_{CCL}	V_{CCH}
MC12514	16	-0.4	-10	0.5	2.4	5.5	4.5	5.0	4.5	5.5
MC12014	16	-0.4	-10	0.5	2.4	5.5	4.5	5.0	4.75	5.25

Characteristic	Symbol	Pin Under Test	MC12514 Test Limits -55 to +125°C Min	Max	Unit	MC12014 Test Limits 0 to +75°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{IC}	V_{IL}	V_{IH}	V_{IHH}	V_{RH}	V_{CC}	V_{CCL}	V_{CCH}	Gnd
Input																			
Forward Current	I_{IL}	1	-6.4	–	mAdc	-6.4	–	mAdc	–	–	–	1	–	–	–	–	–	16	8,10
		2	-1.6	–	↓	-1.6	–	↓	–	–	–	2	–	–	–	–	–	↓	8
		10	-1.6	–		-1.6	–		–	–	–	10	–	–	–	–	–		1,8,11,12,13
		14	-1.6	–		-1.6	–		–	–	–	14	–	–	–	–	–		1,8,11,12,13
Leakage Current	I_{IH}	1	–	160	μAdc	–	160	μAdc	–	–	–	–	1	–	–	–	–	16	8,10
		2	–	40	↓	–	40	↓	–	–	–	–	2	–	–	–	–	↓	8
		10	–	↓		–	↓		–	–	–	–	10	–	–	–	–		1,8,11,12,13
		14	–			–			–	–	–	–	14	–	–	–	–		1,8,11,12,13
	I_{IHH}	1	–	1.0	mAdc	–	1.0	mAdc	–	–	–	–	–	1	–	–	–	16	8
		2	–	↓	↓	–	↓	↓	–	–	–	–	–	2	–	–	–	↓	8
		10	–			–			–	–	–	–	–	10	–	–	–		1,8,11,12,13
		14	–			–			–	–	–	–	–	14	–	–	–		1,8,11,12,13
Clamp Voltage	V_{IC}	1	–	-1.2	Vdc	–	-1.2	Vdc	–	–	1	–	–	–	–	–	16	–	8
		2	–	↓	↓	–	↓	↓	–	–	2	–	–	–	–	–	↓	–	↓
		10	–			–			–	–	10	–	–	–	–	–		–	
		14	–			–			–	–	14	–	–	–	–	–		–	
Output																			
Output Voltage	V_{OL}*	7	–	0.5	Vdc	–	0.5	Vdc	7	–	–	11,12,13	–	–	2,3,4,5,10	–	16	–	8
		9	–	0.5	Vdc	–	0.5	Vdc	9	–	–	11,12,13	–	–	10,14	–	16	–	8
	V_{OH}	7	2.4	–	Vdc	2.4	–	Vdc	–	7	–	2,3,4,5	–	–	6	–	16	–	8
		9**	2.4	–	Vdc	2.4	–	Vdc	–	9	–	–	–	–	11,12,13	–	16	–	8
Short-Circuit Current	I_{OS}	7	-65	-20	Vdc	-65	-20	Vdc	–	–	–	2,3,4,5	–	–	6	16	–	–	7,8
		9**	-65	-20	Vdc	-65	-20	Vdc	–	–	–	–	–	–	11,12,13	16	–	–	8,9
Power Requirements																			
Power Supply Drain	I_{CC}	16†	–	35	mAdc	–	35	mAdc	–	–	–	–	–	–	–	16	–	–	6,8,10

*Output level to be measured after waveform 1 is applied to f_{in}, pin 1.
**Output level to be measured after waveform 2 is applied to f_{in}, pin 1.
†Current to be measured after waveform 1 is applied to f_{in}, pin 1.

Waveform 1: 

Waveform 2: 

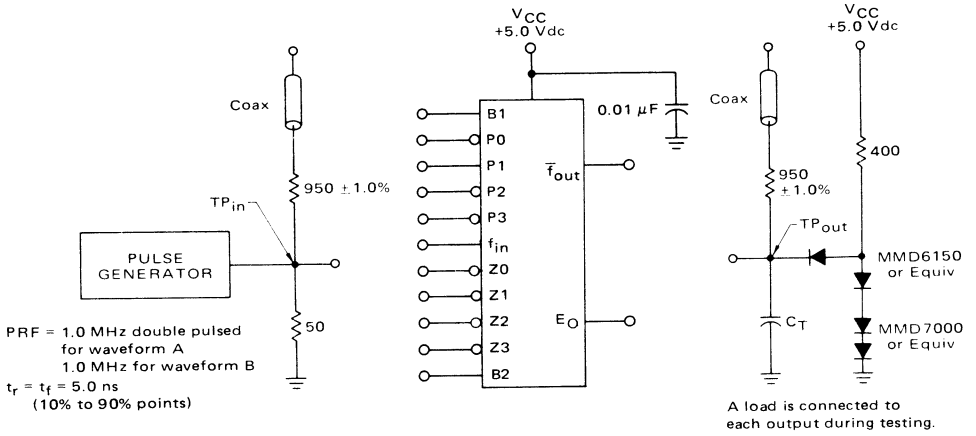
AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, waveform letters refer to waveforms on next page.)

Characteristic	Symbol	Pin Under Test		MC12514 Test Limits (ns)							Pulse Gen. 1		Pulse Gen. 2		Pulse Out		Voltage Applied to Pins Listed Below	
				-55°C		+25°C			+125°C									
		In	Out	Min	Max	Min	Typ	Max	Min	Max	Wave-form	Pin	Wave-form	Pin	Wave-form	Pin	V_{IL} = 0.5 V	V_{IH} = 2.4 V
Propagation Delay	t_{PLH1}	1	9	–	16	–	10	15	–	19	A	1	J	10	K	9	11,12,13	14
	t_{PHL1}	1	9	–	17	–	11	16	–	18	A	1	J	10	K	9	11,12,13	14
	t_{PLH2}	2	7	–	12	–	8.5	12	–	17	A	1	H	2	L	7	3,4,5,11,12,13	6,10,14
		3	↓	–	↓	–	↓	↓	–	↓	↓	↓	↓	3	↓	↓	2,4,5,11,12,13	↓
		4		–		–			–					4			2,3,5,11,12,13	
		5		–		–			–					5			2,3,4,11,12,13	
	t_{PHL2}	1	7	–	17	–	11	16	–	19	A	1	H	2	L	7	3,4,5,11,12,13	6,10,14
	t_{PLH3}	6	7	–	17	–	11	16	–	20	A	1	J	6	L	7	2,3,4,5,11,12,13	10,14
Setup Time	t_{setup}"1"	10	–	–	–	–	1.0	2.0	–	–	A	1	B	10	G	9	11,12,13	14
		11	–	–	–	–	7.0	12	–	–	↓	↓	↓	11	F	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12	↓		11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	1.0	2.0	–	–				14	G		11,12,13	10
	t_{setup}"0"	10	–	–	–	–	4.5	8.0	–	–	A	1	C	10	F	9	11,12,13	14
		11	–	–	–	–	5.0	9.0	–	–	↓	↓	↓	11	G	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12	↓		11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	4.5	8.0	–	–				14	F		11,12,13	10
Hold Time	t_{hold}"1"	10	–	–	–	–	4.0	8.0	–	–	A	1	D	10	G	9	11,12,13	14
		11	–	–	–	–	5.0	10	–	–	↓	↓	↓	11	F	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12	↓		11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	4.0	8.0	–	–				14	G		11,12,13	10
	t_{hold}"0"	10	–	–	–	–	1.0	2.0	–	–	A	1	E	10	F	9	11,12,13	14
		11	–	–	–	–	7.5	14	–	–	↓	↓	↓	11	G	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12	↓		11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	1.0	2.0	–	–				14	F		11,12,13	10

AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, waveform letters refer to waveforms on next page.)

Characteristic	Symbol	Pin Under Test		MC12014 Test Limits (ns)							Pulse Gen. 1		Pulse Gen. 2		Pulse Out		Voltage Applied to Pins Listed Below	
				0°C		+25°C			+75°C									
		In	Out	Min	Max	Min	Typ	Max	Min	Max	Wave-form	Pin	Wave-form	Pin	Wave-form	Pin	V_{IL} = 0.5 V	V_{IH} = 2.4 V
Propagation Delay	t_{PLH1}	1	9	–	15	–	10	15	–	17	A	1	J	10	K	9	11,12,13	14
	t_{PHL1}	1	9	–	16	–	11	16	–	18	A	1	J	10	K	9	11,12,13	14
	t_{PLH2}	2	7	–	12	–	8.5	12	–	14	A	1	H	2	L	7	3,4,5,11,12,13	6,10,14
		3	↓	–	↓	–	↓	↓	–	↓	↓	↓	↓	3	↓	↓	2,4,5,11,12,13	↓
		4		–		–			–					4			2,3,5,11,12,13	
		5		–		–			–					5			2,3,4,11,12,13	
	t_{PHL2}	1	7	–	16	–	11	16	–	18	A	1	H	2	L	7	3,4,5,11,12,13	6,10,14
	t_{PLH3}	6	7	–	16	–	11	16	–	18	A	1	J	6	L	7	2,3,4,5,11,12,13	10,14
Setup Time	t_{setup}"1"	10	–	–	–	–	1.0	2.0	–	–	A	1	B	10	G	9	11,12,13	14
		11	–	–	–	–	7.0	12	–	–	↓	↓	↓	11	F	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12	↓		11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	1.0	2.0	–	–				14	G		11,12,13	10
	t_{setup}"0"	10	–	–	–	–	4.5	8.0	–	–	A	1	C	10	F	9	11,12,13	14
		11	–	–	–	–	5.0	9.0	–	–	↓	↓	↓	11	G	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12	↓		11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	4.5	8.0	–	–				14	F		11,12,13	10
Hold Time	t_{hold}"1"	10	–	–	–	–	4.0	8.0	–	–	A	1	D	10	G	9	11,12,13	14
		11	–	–	–	–	5.0	10	–	–	↓	↓	↓	11	F	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12	↓		11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	4.0	8.0	–	–				14	G		11,12,13	10
	t_{hold}"0"	10	–	–	–	–	1.0	2.0	–	–	A	1	E	10	F	9	11,12,13	14
		11	–	–	–	–	7.5	14	–	–	↓	↓	↓	11	G	↓	12,13	10,14
		12	–	–	–	–	↓	↓	–	–				12	↓		11,13	↓
		13	–	–	–	–			–	–				13			11,12	
		14	–	–	–	–	1.0	2.0	–	–				14	F		11,12,13	10

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS

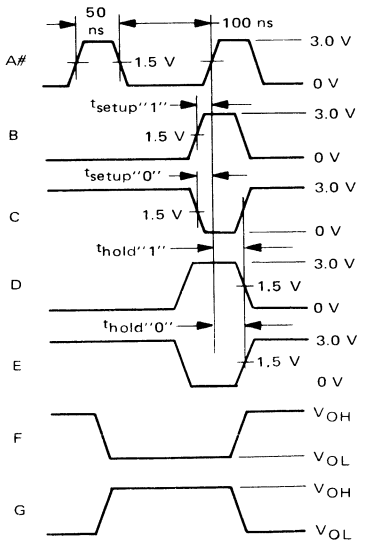


Two pulse generators are required and must be slaved together to provide the waveforms shown.

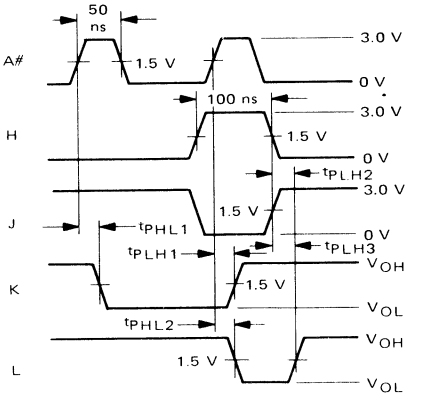
C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched. The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

SETUP AND HOLD TIMES



PROPAGATION DELAY TIMES

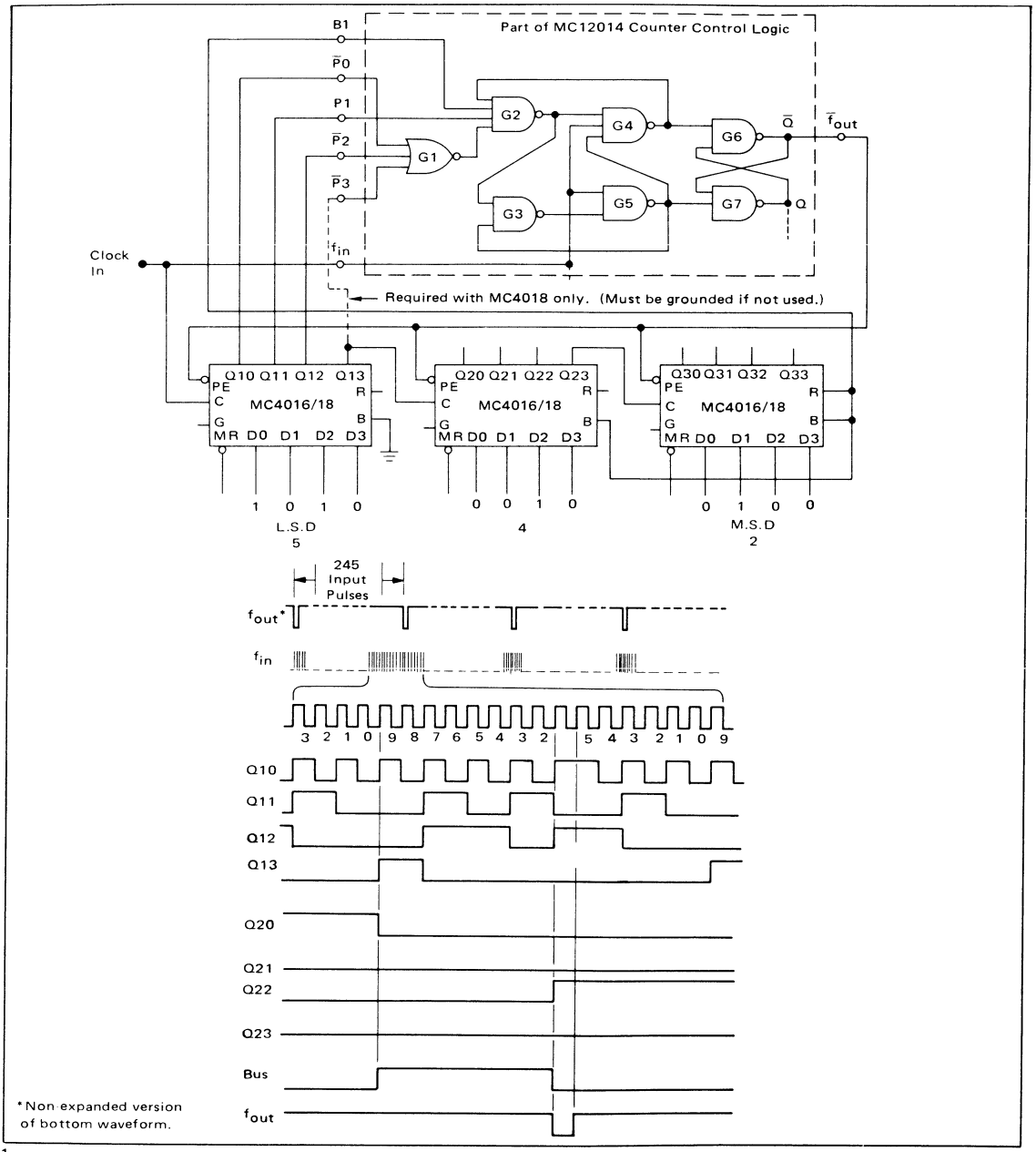


#Pulse A (f_{in}) used with all tests.

APPLICATIONS INFORMATION

The MC12014/MC12514 Counter Control Logic incorporates two features for enhancing operation of the MC4016/MC4018 Programmable Counters.[1] Maximum operating frequency of the counters is limited by the time required for re-programming at the end of each count-down cycle. Operation can be extended to approximately 25 MHz by using the "early decode" feature included in the MC12014. The appropriate connections are shown in

FIGURE 2 – INCREASING THE OPERATING RANGE OF MC4016/MC4018 PROGRAMMABLE COUNTERS USING MC12014/MC12514



[1] See the MC4016/4018 data sheet for additional information.

Figure 2. Only three counter stages are shown; however, up to eight stages can be satisfactorily cascaded. Note the following differences between this and the non-extended method: the counter gate inputs are not connected to the input clock; all parallel enables are connected to the $\overline{Q}$ output (f_{out}) of a type-D flip-flop formed by gates G2 through G7 in the MC12014 package; the bus terminal of the least significant stage is grounded; all other bus terminals and one internal resistor, R, are connected together and serve as a data input, B1, to the flip-flop. Four additional data inputs, $\overline{P0}$ through $\overline{P3}$, serve to decode the "two" state of the least significant counter stage. Circuit operation is illustrated in waveforms of Figure 2, where the timing for the end of a count-down cycle is shown in expanded form. The counter parallel inputs are assumed to have N = 245 programmed. Timing is not shown for the third stage since it has already been counted down to the all zero state. As the next-to-least significant stage reaches zero, the common bus line goes high. Count down of the least significant stage continues until the "two" state is reached, causing the remaining data inputs to the flip-flop to go high. The next-to-last clock pulse of the cycle then triggers the flip-flop $\overline{Q}$ output low. This takes the parallel enables of all three counter stages low, resetting the programmed data to the outputs. The next input pulse clocks $\overline{Q}$ back to the high state since the data inputs to the flip-flop are no longer all high. The resulting negative output pulse at f_{out} is one input clock period in duration. Note that division by N equal to 001 or 002 is not available using this method.

The frequency synthesizer shown in Figure 8 requires that the programmable counters be quickly stopped after reaching their terminal (zero) count. This can be simply accomplished by taking the master reset of all stages low at the appropriate time. The bus output of the counters could be used for this function since a transition there signals the end of a count-down sequence. However, due to the relatively long delay between the last positive clock transition and the bus transition a faster method is required in this application.

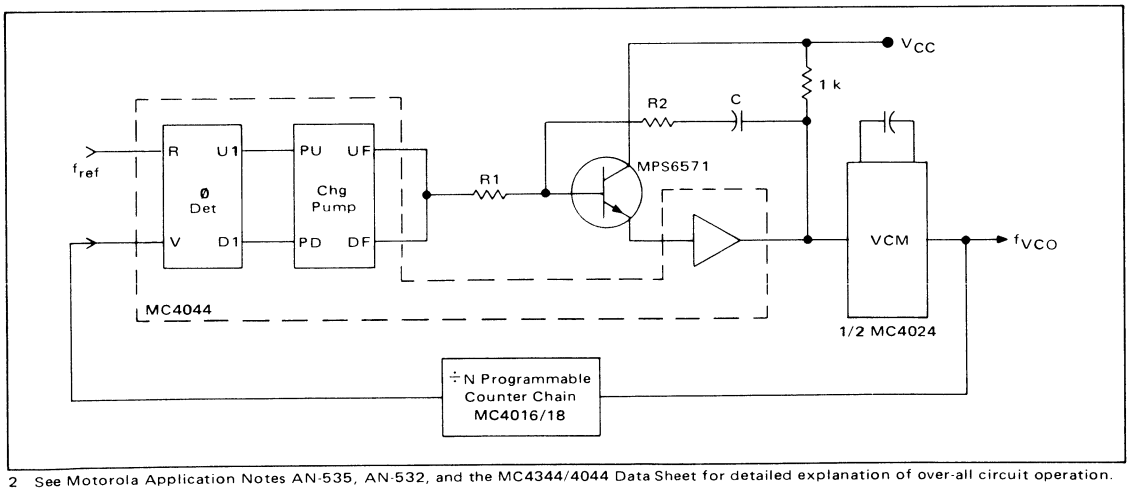
The "zero detection" feature of the MC12014 provides a convenient means of implementing a faster method. Gates G12 through G19 form a latch whose output goes high if B2 is high and low logic levels are applied to the Z0 thru Z3 inputs. When once set to a one by appropriate input conditions, the output of G19 remains high until it is reset by the circuit comprised of gates G8 through G11. Note that since the required information is stored, the counter can be allowed to continue cycling.

The G8-G11 circuit monitors the G7 output of the "early decode" type D flip-flop. When the counter stage connected to the $\overline{P0}$ thru $\overline{P3}$ inputs has counted down to its two state the output of G7 goes high; this enables the G8-G11 circuitry and the next positive clock transition causes the output of G11 to go high, resetting the output of G19 to zero.

Operation of the Counter Control Logic can be further clarified by considering a typical system application for programmable counters illustrated in the frequency synthesizer shown in Figure 3. There the counter provides a means of digitally selecting some integral multiple of a stable reference frequency. The circuit phase locks the output, f_{VCO}, of a voltage controlled oscillator to a reference frequency, f_{ref}.[2] Circuit operation is such that $f_{VCO} = Nf_{ref}$, where N is the divider ratio of the feedback counter, permitting frequency selection by means of thumbwheel switches.

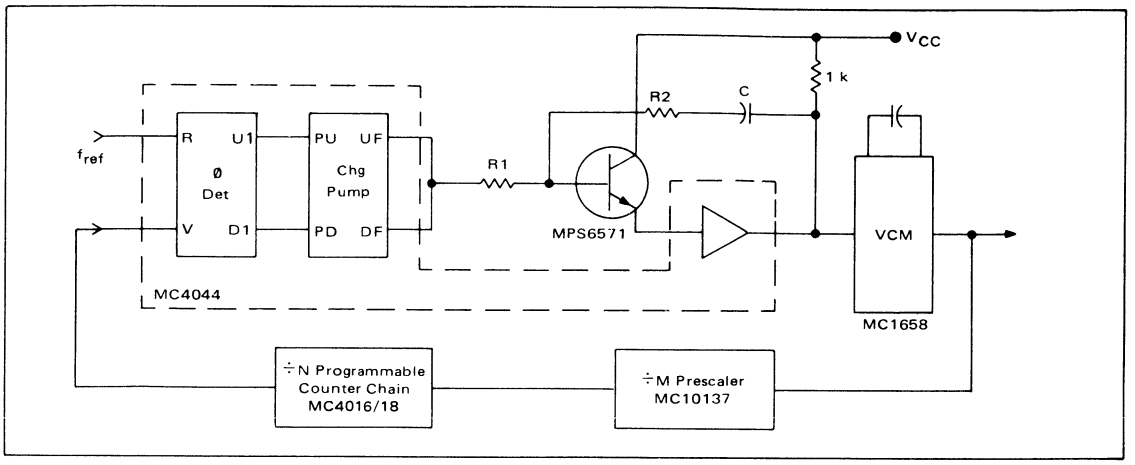
In many synthesizer applications the VCO is operated at VHF frequencies too high for direct division by TTL counters. In these cases the VCO output is usually prescaled by using a suitable fixed divide-by-M ECL circuit as shown in Figure 4. For this configuration, $f_{VCO} = NMf_{ref}$, where N is variable (programmable) and M is fixed. Design of the optimum loop filter requires that the input reference frequency be as high as possible where the upper limit is established by the required channel

FIGURE 3 – MTTL PHASE-LOCKED LOOP



2 See Motorola Application Notes AN-535, AN-532, and the MC4344/4044 Data Sheet for detailed explanation of over-all circuit operation.

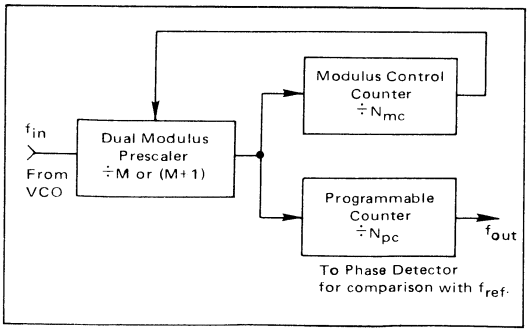
FIGURE 4 – MTTL-MECL PHASE-LOCKED LOOP



spacing. Since $f_{VCO} = Nf_{ref}$ in the non-prescaled case, if N is changed by one, the VCO output changes by f_{ref}, or the synthesizer channel spacing is just equal to f_{ref}. When the prescaler is used as in Figure 4, $f_{VCO} = NMf_{ref}$, and a change of one in N results in the VCO changing by Mf_{ref}, i.e., if f_{ref} is set equal to the minimum permissible channel spacing as is desirable, then only every M channels in a given band can be selected. One solution is to set f_{ref} = channel spacing/M but this leads to more stringent loop filter requirements.

An alternate approach that avoids this problem is provided by the counter configuration shown in Figure 5. It too uses a prescaler ahead of a programmable counter, however the modulus of the prescaler is now controlled by a third counter, causing it to alternate between M and M + 1. Operation is best explained by assuming that all three counters have been set for the beginning of a cycle: the prescaler for division by (M + 1), the modulus control counter for division by N_{mc}, and the programmable counter for division by N_{pc}. The prescaler will divide by (M +1) until the modulus control counter has counted down to zero; at this time, the all zero state is detected and causes the prescaler to divide by M until the programmable counter has also counted down to zero. When this occurs, a cycle is complete and each counter is reset to its original modulus in readiness for the next cycle.

FIGURE 5 – FEEDBACK COUNTERS WITH DUAL MODULUS PRESCALER



To determine the relationship between f_{out} and f_{in}, let T_1 be the time required for the modulus control counter to reach its terminal count and let T_2 be the remainder of one cycle. That is, T_2 is the time between terminal count in the modulus control counter and terminal count in the programmable counter. When the modulus control counter reaches zero, N_{mc} pulses will have entered it at a rate given by $f_{in}/(M + 1)$ pulses/second or T_1 is:

$$T_1 = \frac{(M + 1)}{f_{in}} \bullet N_{mc} \qquad (1)$$

At this time, N_{mc} pulses have also entered the programmable counter and it will reach its terminal counter after $(N_{pc} - N_{mc})$ more pulses have entered. The rate of entry is now f_{in}/M pulses/second since the prescaler is now dividing by M. From this T_2 is given by:

$$T_2 = \frac{M}{f_{in}} \bullet (N_{pc} - N_{mc}) \qquad (2)$$

Since $f = \frac{1}{T}$:

$$f_{out} = \frac{1}{T_{total}} = \frac{1}{T_1 + T_2} = \frac{1}{\frac{(M + 1)N_{mc}}{f_{in}} + \frac{M(N_{pc} - N_{mc})}{f_{in}}} \qquad (3)$$

$$f_{out} = \frac{f_{in}}{(M+1)N_{mc} + M(N_{pc}-N_{mc})}$$

$$= \frac{f_{in}}{MN_{mc}+N_{mc}+MN_{pc}-MN_{mc}}$$

$$= \frac{f_{in}}{MN_{pc}+N_{mc}}$$

In terms of the synthesizer application, $f_{VCO} = (MN_{pc} + N_{mc})\, f_{ref}$ and channels can be selected every f_{ref} by letting N_{pc} and N_{mc} take on suitable integer values, including zero.

A simplified example of this technique is shown in Figure 6. The MC12012 Dual Modulus Prescaler divides by either 10 or 11 when connected as shown in Figure 6. If the E3 and E4 Enable inputs are high at the start of a prescaler cycle, division by 10 results; if the Enable inputs are low at the beginning of the cycle, division by 11 results. The zero detection circuitry of the MC12014 Counter Control Logic is connected to monitor the outputs of the modulus control counter; this provides a suitable enable signal at E0 as the modulus control counter reaches its terminal (zero) count. The remainder of the MC12014 is connected to extend the operating frequency of the programmable counter chain. Appropriate waveforms for division by 43 are shown in Figure 7a.

The beginning of the timing diagram indicates circuit status just prior to the end of a countdown cycle, i.e., the modulus control counter has been counted down to one and the programmable counter is in the two state. The next positive transition from the prescaler (f1 in the timing diagram) then initiates the following sequence of events. Since the two state of the programmable counter enables the early decode circuitry in the MC12014, the positive f1 transition causes f_{out} to go low. Since f_{out} is connected to the Parallel Enables of all the MC4016 counters this low signal will re-program the counters in readiness for another cycle. However, due to the propagation time through the decode circuitry, the programmable and modulus control counters are briefly decremented to one and zero, respectively, before re-programming occurs. The momentary zero state of the modulus control counter is detected, setting E_O of the MC12014 high, enabling the MC12012 for division by ten during its next cycle. After eleven more f_{in} pulses (E_O went high after the beginning of the prescaler cycle and so doesn't change the modulus until the next prescaler cycle), f1 again goes high, causing f_{out} to return to the one state. This releases the Parallel Enables and simultaneously resets E_O to zero. However, since E_O was high when the current prescaler cycle began, the next positive f1 transition occurs only ten f_{in} pulses later. Subsequent f1 transitions now decrement the MC4016 counters down through another cycle with the prescaler dividing by eleven. From the waveforms, 11 + 10 + 11 + 11 = 43 input pulses occur for each output pulse.

Division by 42 is shown in Figure 7b. Operation is similar except that the modulus control counter reaches its terminal count one f1 cycle earlier than before. Since

FIGURE 6 – FREQUENCY DIVISION: $f_O = f_{in}/(MN_{pc} + N_{mc})$

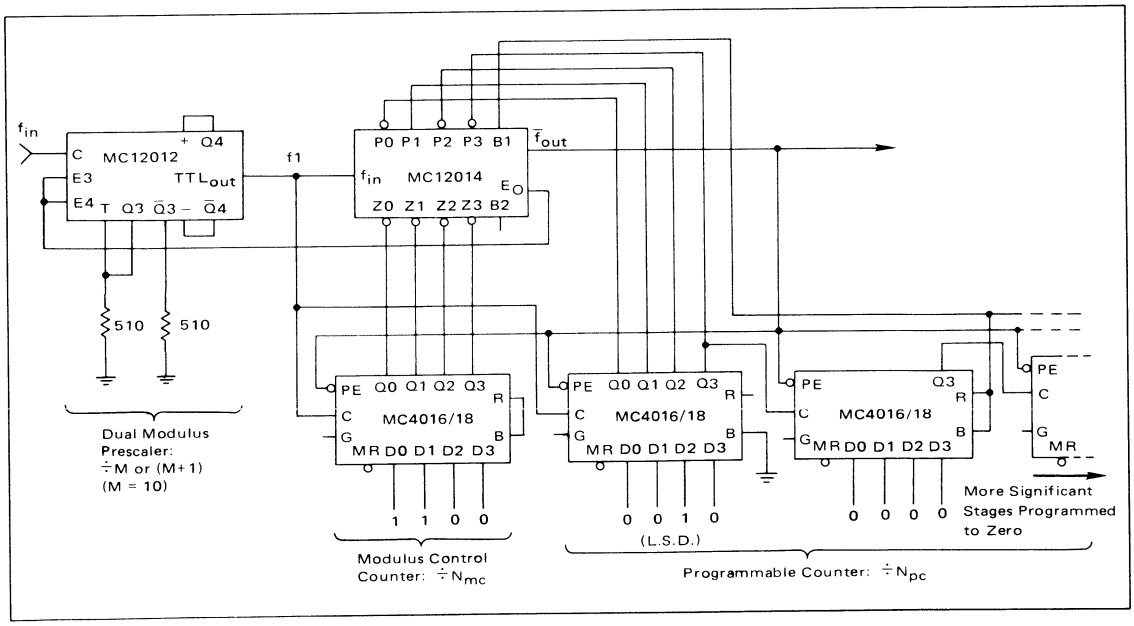


FIGURE 7a – DIVISION BY 43

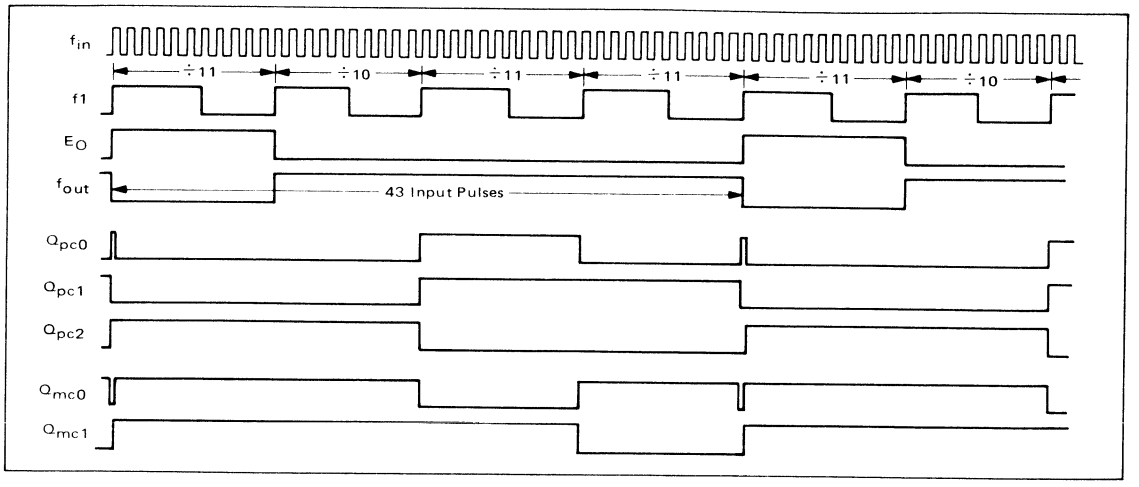
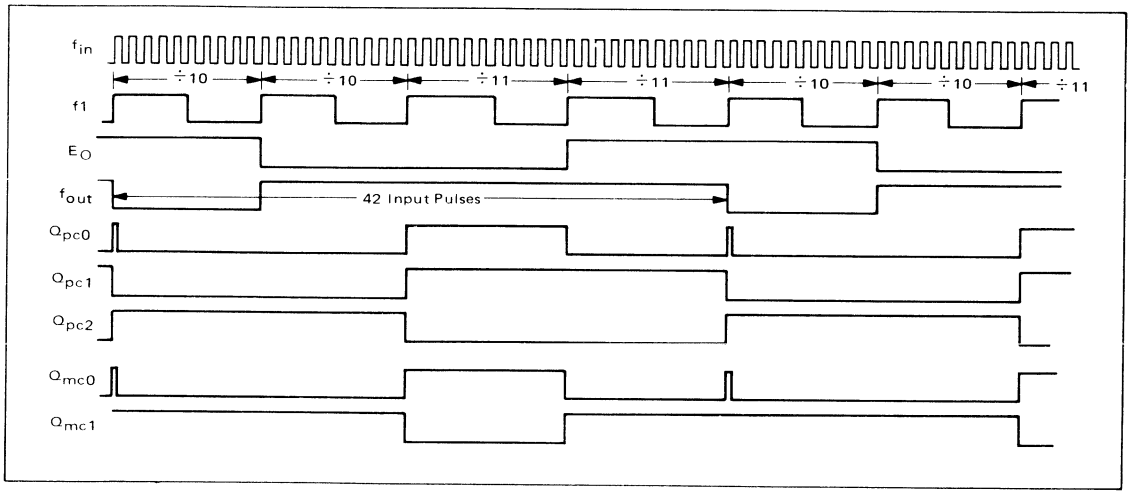


FIGURE 7b – DIVISION BY 42



E_O is reset by the trailing edge of the f_{out} pulse, E_O now remains high for two prescaler cycles leading to 10 + 10 + 11 + 11 = 42 input pulses for each output pulse.

Other combinations lead to similar results, however note that N_{pc} must be greater than or equal to N_{mc} for operation as described. If N_{mc} is greater than N_{pc} erroneous results are obtained, however this is not a serious restriction since N_{pc} is greater than N_{mc} in most practical applications.

The synthesizer shown in Figure 8 generates frequencies in the range from 144 to 178 MHz with 30 kHz channel spacing. It uses the dual modulus prescaler approach discussed earlier. General synthesizer design considerations are detailed in the publications listed in footnote 2, hence only the feedback counter is discussed here. Requirements for the feedback divider are determined from:

$$\text{Minimum Divider Ratio} = N_{Tmin} = \frac{144.00\ \text{MHz}}{30\ \text{kHz}} = 4800$$

$$\text{Maximum Divider Ratio} = N_{Tmax} = \frac{177.99\ \text{MHz}}{30\ \text{kHz}} = 5933$$

If the prescaler divides by at least ten, the maximum input frequency to the TTL counters will be 17.799 MHz, allowing use of MC4016 Programmable Counters with the MC12014 frequency extension feature.

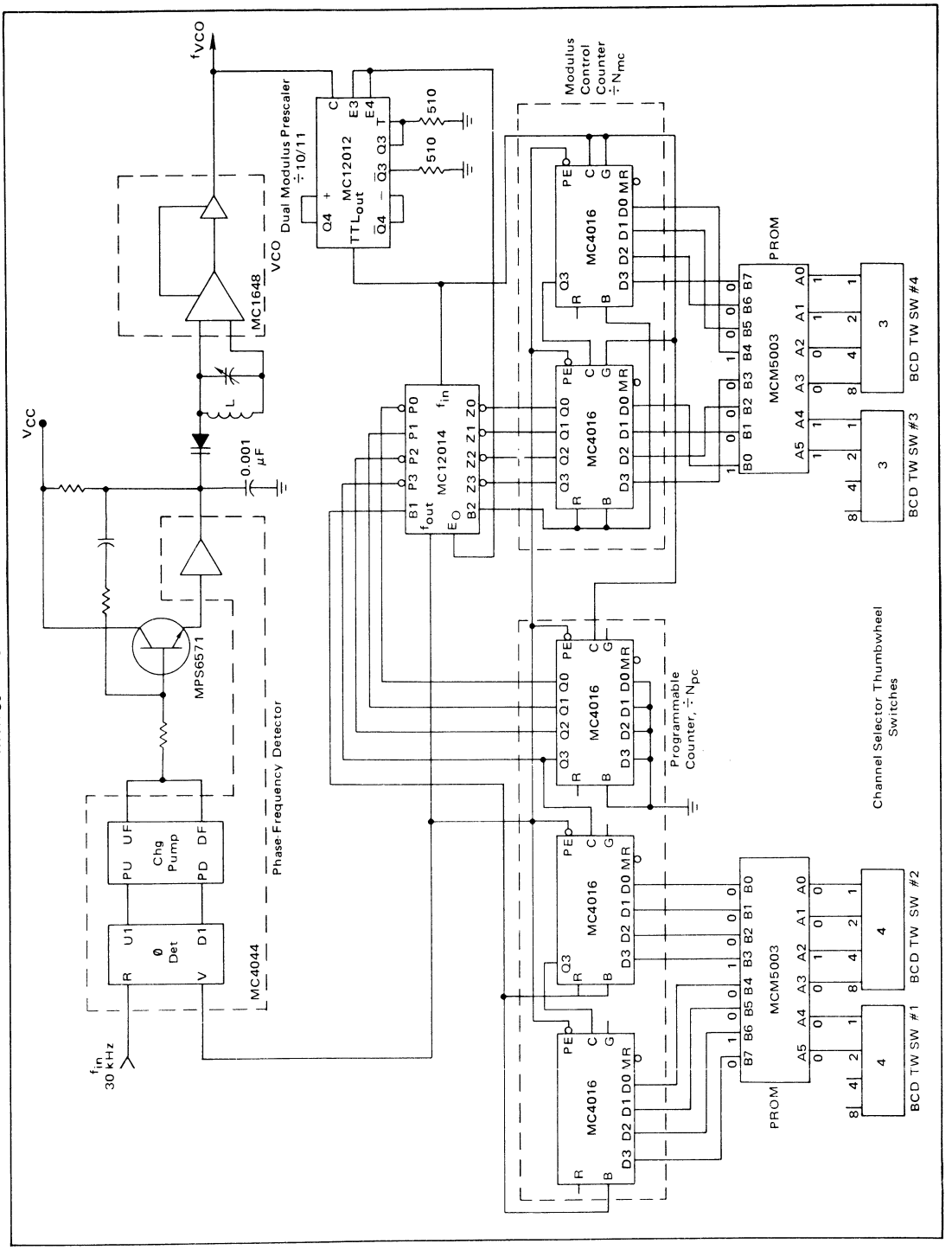


FIGURE 8 – 144 TO 178 MHz FREQUENCY SYNTHESIZER WITH 30 kHz CHANNEL SPACING

FIGURE 9 – N_{pc} PROM PROGRAMMING

	SW #1	SW #2	SW #1 A5 A4	SW #2 A3 A2 A1 A0	PROM WORD	PROM OUTPUT M.S.B.	PROM OUTPUT L.S.B.	N_{pc}	
(144 MHz)	44		0 1 0 0	0 1 0 0	4	0 1 0 0	1 0 0 0	48	480
	45		0 1 0 0	0 1 0 1	5	0 1 0 0	1 0 0 0	48	
	46		0 1 0 0	0 1 1 0	6	0 1 0 0	1 0 0 0	48	
	47		0 1 0 0	0 1 1 1	7	0 1 0 0	1 0 0 1	49	
	48		0 1 0 0	1 0 0 0	8	0 1 0 0	1 0 0 1	49	
	49		0 1 0 0	1 0 0 1	9	0 1 0 0	1 0 0 1	49	
	50		0 1 0 1	0 0 0 0	16	0 1 0 1	0 0 0 0	50	
	51		0 1 0 1	0 0 0 1	17	0 1 0 1	0 0 0 0	50	
	52		0 1 0 1	0 0 1 0	18	0 1 0 1	0 0 0 0	50	
	53		0 1 0 1	0 0 1 1	19	0 1 0 1	0 0 0 1	51	
	54		0 1 0 1	0 1 0 0	20	0 1 0 1	0 0 0 1	51	
	55		0 1 0 1	0 1 0 1	21	0 1 0 1	0 0 0 1	51	
	56		0 1 0 1	0 1 1 0	22	0 1 0 1	0 0 1 0	52	
	57		0 1 0 1	0 1 1 1	23	0 1 0 1	0 0 1 0	52	
	58		0 1 0 1	1 0 0 0	24	0 1 0 1	0 0 1 0	52	
	59		0 1 0 1	1 0 0 1	25	0 1 0 1	0 0 1 1	53	
	60		0 1 1 0	0 0 0 0	32	0 1 0 1	0 0 1 1	53	
	61		0 1 1 0	0 0 0 1	33	0 1 0 1	0 0 1 1	53	
	62		0 1 1 0	0 0 1 0	34	0 1 0 1	0 1 0 0	54	
	63		0 1 1 0	0 0 1 1	35	0 1 0 1	0 1 0 0	54	
	64		0 1 1 0	0 1 0 0	36	0 1 0 1	0 1 0 0	54	
	65		0 1 1 0	0 1 0 1	37	0 1 0 1	0 1 0 1	55	
	66		0 1 1 0	0 1 1 0	38	0 1 0 1	0 1 0 1	55	
	67		0 1 1 0	0 1 1 1	39	0 1 0 1	0 1 0 1	55	
	68		0 1 1 0	1 0 0 0	40	0 1 0 1	0 1 1 0	56	
	69		0 1 1 0	1 0 0 1	41	0 1 0 1	0 1 1 0	56	
	70		0 1 1 1	0 0 0 0	48	0 1 0 1	0 1 1 0	56	
	71		0 1 1 1	0 0 0 1	49	0 1 0 1	0 1 1 1	57	
	72		0 1 1 1	0 0 1 0	50	0 1 0 1	0 1 1 1	57	
	73		0 1 1 1	0 0 1 1	51	0 1 0 1	0 1 1 1	57	
	74		0 1 1 1	0 1 0 0	52	0 1 0 1	1 0 0 0	58	
	75		0 1 1 1	0 1 0 1	53	0 1 0 1	1 0 0 0	58	
	76		0 1 1 1	0 1 1 0	54	0 1 0 1	1 0 0 0	58	
(177 MHz)	77		0 1 1 1	0 1 1 1	55	0 1 0 1	1 0 0 1	59	590

WORD	BIT 7	6	5	4	3	2	1	0
0	–				–			
1	–				–			
2	–				–			
3	–				–			
4	0	1	0	0	1	0	0	0
5	0	1	0	0	1	0	0	0
6	0	1	0	0	1	0	0	0
7	0	1	0	0	1	0	0	1
8	0	1	0	0	1	0	0	1
9	0	1	0	0	1	0	0	1
10	–		–	–	–	–	–	–
11	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–
13	–	–	–	–	–	–	–	–
14	–	–	–	–	–	–	–	–
15	–	–	–	–	–	–	–	–
16	0	1	0	1	0	0	0	0
17	0	1	0	1	0	0	0	0
18	0	1	0	1	0	0	0	0
19	0	1	0	1	0	0	0	1
20	0	1	0	1	0	0	0	1
21	0	1	0	1	0	0	0	1
22	0	1	0	1	0	0	1	0
23	0	1	0	1	0	0	1	0
24	0	1	0	1	0	0	1	0
25	0	1	0	1	0	0	1	1
26	–	–	–	–	–	–	–	–
27	–	–	–	–	–	–	–	–
28	–	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–	–
32	0	1	0	1	0	0	1	1
33	0	1	0	1	0	0	1	1
34	0	1	0	1	0	1	0	0
35	0	1	0	1	0	1	0	0
36	0	1	0	1	0	1	0	0
37	0	1	0	1	0	1	0	1
38	0	1	0	1	0	1	0	1
39	0	1	0	1	0	1	0	1
40	0	1	0	1	0	1	1	0
41	0	1	0	1	0	1	1	0
42	–	–	–	–	–	–	–	–
43	–	–	–	–	–	–	–	–
44	–	–	–	–	–	–	–	–
45	–	–	–	–	–	–	–	–
46	–	–	–	–	–	–	–	–
47	–	–	–	–	–	–	–	–
48	0	1	0	1	0	1	1	0
49	0	1	0	1	0	1	1	1
50	0	1	0	1	0	1	1	1
51	0	1	0	1	0	1	1	1
52	0	1	0	1	1	0	0	0
53	0	1	0	1	1	0	0	0
54	0	1	0	1	1	0	0	0
55	0	1	0	1	1	0	0	1
56	–	–	–	–	–	–	–	–
57	–	–	–	–	–	–	–	–
58	–	–	–	–	–	–	–	–
59	–	–	–	–	–	–	–	–
60	–	–	–	–	–	–	–	–
61	–	–	–	–	–	–	–	–
62	–	–	–	–	–	–	–	–
63	–	–	–	–	–	–	–	–

The required divider range, 4800 to 5933, is obtained in the following manner: the MC12012 Dual Modulus Prescaler is connected in the divide by 10/11 mode; the modulus control counter uses two MC4016 stages with N_{mc} ranging from 00 to 99, establishing the two least significant digits of N_T. The remaining two digits of N_T are obtained from a three stage programmable counter generating N_{pc}. The least significant stage of the N_{pc} counter is fixed programmed to zero. The required programming for all remaining stages is derived from four channel selector BCD thumbwheel switches. The relationship between N_T and the counters is given by $N_T = MN_{pc} + N_{mc}$; for a typical channel, say 144.33 MHz, $N_T = 4811$ requires that M = 10, $N_{pc} = 480$, and $N_{mc} = 11$, or $N_T = (10)(480) + 11 = 4811$.

A general problem associated with synthesizer design arises from the fact that there is not always a one-to-one correspondence between the code provided by the channel selector switches and the code required for proper programming of the counters. For instance, in the example above where 144.33 MHz was selected, the channel selector switches are set to 44.33 while the required divider ratio is 4811. There are numerous solutions for a given translation requirement, however the method shown here using read only memories offers a straight-forward design method. While field programmable read only memories (PROMs)[3] are shown, they would normally be used only during development; suitable fixed ROMs are more economical in production quantities. The design procedure for the code conversion is illustrated in Figure 9. The required pro-

3 See the MCM5003 data sheet and AN-550 for details of operation; briefly, one of 64 eight-bit output words is selected by a six-bit address applied to the input. The word located at each address can be field programmed by the user.

FIGURE 10 – N_{mc} PROM # 1 PROGRAMMING

	SW #3	SW #4	SW #3 A5 A4	SW #4 A3 A2 A1 A0	PROM WORD	PROM OUTPUT M.S.B	PROM OUTPUT L.S.B.	N_{mc}
(144)		.00	0 0	0 0 0 0	0	0 0 0 0	0 0 0 0	00
		.03	0 0	0 0 1 1	3	0 0 0 0	0 0 0 1	01
		.06	0 0	0 1 1 0	6	0 0 0 0	0 0 1 0	02
		.09	0 0	1 0 0 1	9	0 0 0 0	0 0 1 1	03
		.12	0 0	0 0 1 0	18	0 0 0 0	0 1 0 0	04
		.15	0 0	0 1 0 1	21	0 0 0 0	0 1 0 1	05
		.18	0 0	1 0 0 0	24	0 0 0 0	0 1 1 0	06
		.21	0 0	0 0 0 1	33	0 0 0 0	0 1 1 1	07
		.24	0 0	1 0 0 0	36	0 0 0 0	1 0 0 0	08
		.27	0 0	0 1 1 1	39	0 0 0 0	1 0 0 1	09
		.30	0 0	0 0 0 0	48	0 0 0 1	0 0 0 0	10
		.33	0 0	0 0 1 1	51	0 0 0 1	0 0 0 1	11
		.36	0 0	0 1 1 0	54	0 0 0 1	0 0 1 0	12
		.39	0 0	1 0 0 1	57	0 0 0 1	0 0 1 1	13
		.42	0 1	0 0 1 0	2	0 0 0 1	0 1 0 0	14
		.45	0 1	0 0 0 1	5	0 0 0 1	0 1 0 1	15
		.48	0 1	0 0 0 0	8	0 0 0 1	0 1 1 0	16
		.51	0 1	0 0 0 1	17	0 0 0 1	0 1 1 1	17
		.54	0 1	0 1 0 0	20	0 0 0 1	1 0 0 0	18
		.57	0 1	0 1 1 1	23	0 0 0 1	1 0 0 1	19
		.60	0 1	1 0 0 0	32	0 0 1 0	0 0 0 0	20
		.63	0 1	1 0 0 1	35	0 0 1 0	0 0 0 1	21
		.66	0 1	1 0 1 0	38	0 0 1 0	0 0 1 0	22
		.69	0 1	1 0 1 1	41	0 0 1 0	0 0 1 1	23
		.72	0 1	1 1 0 0	49	0 0 1 0	0 1 0 0	24
		.75	0 1	1 1 0 1	53	0 0 1 0	0 1 0 1	25
		.78	0 1	1 1 1 0	56	0 0 1 0	0 1 1 0	26
		.81	1 0	0 0 0 1	1	0 0 1 0	0 1 1 1	27
		.84	1 0	0 0 1 0	4	0 0 1 0	1 0 0 0	28
		.87	1 0	0 0 1 1	7	0 0 1 0	1 0 0 1	29
		.90	1 0	0 1 0 0	16	0 0 1 1	0 0 0 0	30
		.93	1 0	0 1 0 1	19	0 0 1 1	0 0 0 1	31
		.96	1 0	0 1 1 0	22	0 0 1 1	0 0 1 0	32
(144)		.99	1 0	0 1 1 1	25	0 0 1 1	0 0 1 1	33

Use with frequency ranges

144.00 – 144.99	162.00 – 162.99
147.00 – 147.99	165.00 – 165.99
150.00 – 150.99	168.00 – 168.99
153.00 – 153.99	171.00 – 171.99
156.00 – 156.99	174.00 – 174.99
159.00 – 159.99	177.00 – 177.99

WORD	BIT 7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	1	1	1
2	0	0	0	1	0	1	0	0
3	0	0	0	0	0	0	0	1
4	0	0	1	0	1	0	0	0
5	0	0	0	1	0	1	0	1
6	0	0	0	0	0	0	1	0
7	0	0	1	0	1	0	0	1
8	0	0	0	1	0	1	1	0
9	0	0	0	0	0	0	1	1
10	–	–	–	–	–	–	–	–
11	–	–	–	–	–	–	–	–
12	–	–	–	–	–	–	–	–
13	–	–	–	–	–	–	–	–
14	–	–	–	–	–	–	–	–
15	–	–	–	–	–	–	–	–
16	0	0	1	1	0	0	0	0
17	0	0	0	1	0	1	1	1
18	0	0	0	0	0	1	0	0
19	0	0	1	1	0	0	0	1
20	0	0	0	1	1	0	0	0
21	0	0	0	0	0	1	0	1
22	0	0	1	1	0	0	1	0
23	0	0	0	1	1	0	0	1
24	0	0	0	0	0	1	1	0
25	0	0	1	1	0	0	1	1
26	–	–	–	–	–	–	–	–
27	–	–	–	–	–	–	–	–
28	–	–	–	–	–	–	–	–
29	–	–	–	–	–	–	–	–
30	–	–	–	–	–	–	–	–
31	–	–	–	–	–	–	–	–
32	0	0	1	0	0	0	0	0
33	0	0	0	0	0	1	1	1
34	–	–	–	–	–	–	–	–
35	0	0	1	0	0	0	0	1
36	0	0	0	0	1	0	0	0
37	–	–	–	–	–	–	–	–
38	0	0	1	0	0	0	1	0
39	0	0	0	0	1	0	0	1
40	–	–	–	–	–	–	–	–
41	0	0	1	0	0	0	1	1
42	–	–	–	–	–	–	–	–
43	–	–	–	–	–	–	–	–
44	–	–	–	–	–	–	–	–
45	–	–	–	–	–	–	–	–
46	–	–	–	–	–	–	–	–
47	–	–	–	–	–	–	–	–
48	0	0	0	1	0	0	0	0
49	0	0	1	0	0	1	0	0
50	–	–	–	–	–	–	–	–
51	0	0	0	1	0	0	0	1
52	–	–	–	–	–	–	–	–
53	0	0	1	0	0	1	0	1
54	0	0	0	1	0	0	1	0
55	–	–	–	–	–	–	–	–
56	0	0	1	0	0	1	1	0
57	0	0	0	1	0	0	1	1
58	–	–	–	–	–	–	–	–
59	–	–	–	–	–	–	–	–
60	–	–	–	–	–	–	–	–
61	–	–	–	–	–	–	–	–
62	–	–	–	–	–	–	–	–
63	–	–	–	–	–	–	–	–

gramming for the two most significant digits of N_{pc} is shown versus the code provided by switches #1 and #2 of the channel selector. If the four outputs of switch #2 and the two least significant outputs of switch #1 are regarded as address bits A0 through A5 for an MCM5003 PROM, a memory location can be associated with each switch setting. The required N_{pc} programming for each switch setting is then set into the appropriate memory location by the user. In Figure 9, the required programming has been transferred into a truth table to be used while programming the PROM. A similar result for the N_{mc} programming is shown in Figure 10. Note that the PROM shown, N_{mc} PROM #1, selects only N_{mc} numbers 00 through 33. This means that the synthesizer as shown in Figure 8 selects only the adjacent channels in a one megahertz slice of the total band. The frequency ranges that can be selected using N_{mc} PROM #1 are summarized in Figure 10. For other ranges, N_{mc} PROM #1 must be replaced by one of two additional PROMs required for generating the remaining N_{mc} numbers. Appropriate truth tables along with the ranges they can be used with are shown in Figures 11 and 12.

FIGURE 11 – N_{mc} PROM #2 TRUTH TABLE

WORD	BIT 7	6	5	4	3	2	1	0
0	0	1	1	0	0	0	0	0
1	0	1	0	0	0	1	1	1
2	0	0	1	1	0	1	0	0
3	0	1	1	0	0	0	0	1
4	0	1	0	0	1	0	0	0
5	0	0	1	1	0	1	0	1
6	0	1	1	0	0	0	1	0
7	0	1	0	0	1	0	0	1
8	0	0	1	1	0	1	1	0
9	0	1	1	0	0	0	1	1
10								
11								
12								
13								
14								
15								
16	0	1	0	1	0	0	0	0
17	0	0	1	1	0	1	1	1
18	0	1	1	0	0	1	0	0
19	0	1	0	1	0	0	0	1
20	0	0	1	1	1	0	0	0
21	0	1	1	0	0	1	0	1
22	0	1	0	1	0	0	1	0
23	0	0	1	1	1	0	0	1
24	0	1	1	0	0	1	1	0
25	0	1	0	1	0	0	1	1
26								
27								
28								
29								
30								
31								
32	0	1	0	0	0	0	0	0
33								
34	0	1	0	1	0	1	0	0
35	0	1	0	0	0	0	0	1
36								
37	0	1	0	1	0	1	0	1
38	0	1	0	0	0	0	1	0
39								
40	0	1	0	1	0	1	1	0
41	0	1	0	0	0	0	1	1
42								
43								
44								
45								
46								
47								
48								
49	0	1	0	1	0	1	1	1
50	0	1	0	0	0	1	0	0
51								
52	0	1	0	1	1	0	0	0
53	0	1	0	0	0	1	0	1
54								
55	0	1	0	1	1	0	0	1
56	0	1	0	0	0	1	1	0
57								
58								
59								
60								
61								
62								
63								

Use with frequency ranges

145.02	145.98	163.02	163.98
148.02	148.98	166.02	166.98
151.02	151.98	169.02	169.98
154.02	154.98	172.02	172.98
157.02	157.98	175.02	175.98
160.02	160.98		

FIGURE 12 – N_{mc} PROM #3 TRUTH TABLE

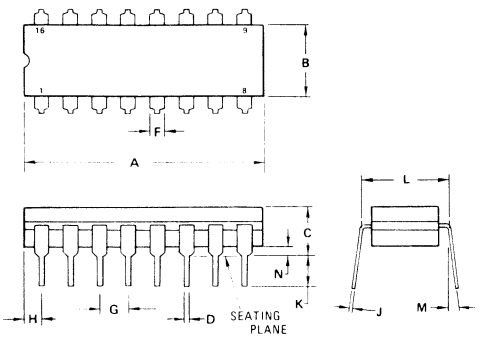
WORD	BIT 7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	0	0
1	0	1	1	0	0	1	1	1
2	1	0	0	1	0	1	0	0
3	1	0	0	0	0	0	0	1
4	0	1	1	0	1	0	0	0
5	1	0	0	1	0	1	0	1
6	1	0	0	0	0	0	1	0
7	0	1	1	0	1	0	0	1
8	1	0	0	1	0	1	1	0
9	1	0	0	0	0	0	1	1
10								
11								
12								
13								
14								
15								
16	0	1	1	1	0	0	0	0
17	1	0	0	1	0	1	1	1
18	1	0	0	0	0	1	0	0
19	0	1	1	1	0	0	0	1
20	1	0	0	1	1	0	0	0
21	1	0	0	0	0	1	0	1
22	0	1	1	1	0	0	1	0
23	1	0	0	1	1	0	0	1
24	1	0	0	0	0	1	1	0
25	0	1	1	1	0	0	1	1
26								
27								
28								
29								
30								
31								
32								
33	1	0	0	0	0	1	1	1
34	0	1	1	1	0	1	0	0
35								
36								
37	0	1	1	1	0	1	0	1
38	1	0	0	0	1	0	0	0
39	1	0	0	0	1	0	0	1
40	0	1	1	1	0	1	1	0
41								
42								
43								
44								
45								
46								
47								
48	1	0	0	1	0	0	0	0
49	0	1	1	1	0	1	1	1
50								
51	1	0	0	1	0	0	0	1
52	0	1	1	1	1	0	0	0
53								
54	1	0	0	1	0	0	1	0
55	0	1	1	1	1	0	0	1
56								
57	1	0	0	0	0	0	1	1
58								
59								
60								
61								
62								
63								

Use with frequency ranges:

146.01	146.97	164.01	164.97
149.01	149.97	167.01	167.97
152.01	152.97	170.01	170.97
155.01	155.97	173.01	173.97
158.01	158.97	176.01	176.97
161.01	161.97		

OUTLINE DIMENSIONS

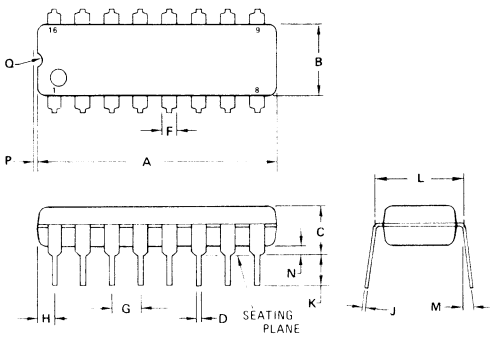
CASE 620-02



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2. PKG. INDEX: NOTCH IN LEAD NOTCH IN CERAMIC OR INK DOT
3. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.31	0.008	0.012
K	3.18	0.30	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15^0	–	15^0
N	0.51	1.02	0.020	0.040

CASE 648-03



NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10^0	–	10^0
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

MC12020 • MC12520

OFFSET CONTROL

MC12021 • MC12521

OFFSET PROGRAMMER

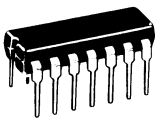
MC12020 • MC12520

The MC12020/520 is an IF offset control block that provides a digital means of producing automatic IF offset generation for synthesizer tuned transceivers when used in conjunction with the MC12021 or MC12521. It is a modified D-type flip-flop that is capable of two modes of operation. The mode of operation is controlled by the receive/transmit input. When the R/T input is at a logical one level, the part becomes simply a toggle flip-flop and divides by two at both Q and $\overline{Q}$ outputs. With the R/T input at a logical zero level, the Q output becomes a buffer gate that follows the clock input and the $\overline{Q}$ output produces a constant one level. An inverter gate is provided which can be used to invert the clock polarity. This option is to ensure the device can always be clocked on the same edge that clears the counter presets. This device was designed for low frequency operation which allows low power operation. Its maximum current drain is 9.6 mA over temperature.

MC12021 • MC12521

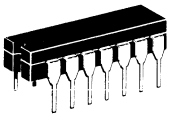
The MC12021/521 is an IF offset programmer that provides a means of producing automatic IF offset generation for synthesizer tuned transceivers when used in conjunction with the MC12020 or the MC12520 control block. The part is an eight-input, four-output data selector. It is the logic implementation of a four-pole, two position switch with the switch position controlled by the enable input. One set of input codes determine the frequency of transmission and is programmable with either switches or circuitry; the other code determines the IF offset frequency. The enable input is controlled by the $\overline{Q}$ output of the MC12020/520. This device was designed for low frequency operation which allows for low power operation. Maximum current drain is 9.4 mA over temperature.

MC12020, MC12520



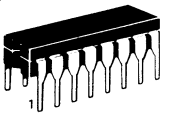
L SUFFIX
CERAMIC PACKAGE
CASE 632

MC12020



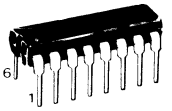
P SUFFIX
PLASTIC PACKAGE
CASE 646

MC12021, MC12521



L SUFFIX
CERAMIC PACKAGE
CASE 620

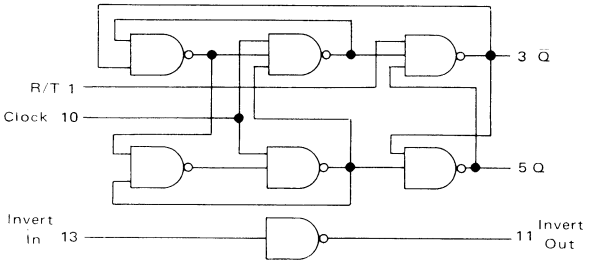
MC12021



P SUFFIX
PLASTIC PACKAGE
CASE 648

LOGIC DIAGRAMS

MC12020 • MC12520

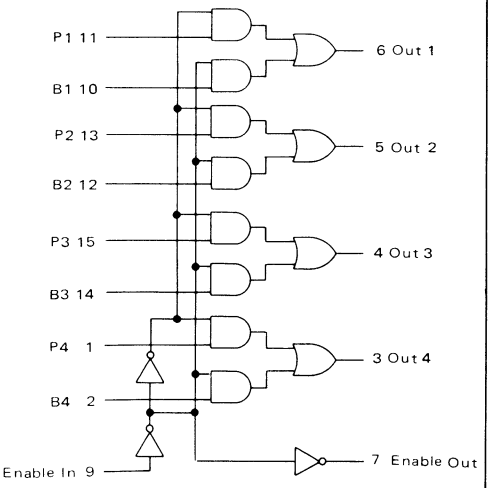


MC12020 • MC12520

Functional Truth Table			
Input		Output	
R/T	Clock	Q	$\overline{Q}$
0	0	0	1
0	1	1	1
1	1	1	0
1	0	1	0
1	1	0	1

V_{CC} = Pin 14 = +5.0 Vdc
Gnd = Pin 7
0 @ Clock, R/T = +0.5 Vdc
1 @ Clock, R/T = +4.0 Vdc

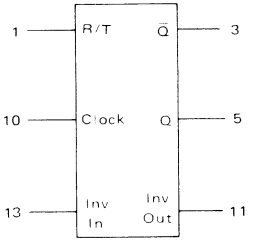
MC12021 • MC12521



ELECTRICAL CHARACTERISTICS

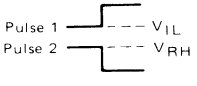
Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.

*The device must be tested by sequencing through the tests maintaining power supply and ground voltages between tests. Procedures with (**) are necessary to get device into proper state for testing.



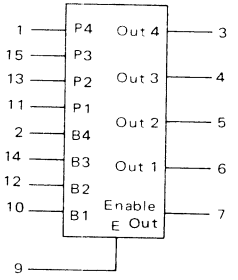
	TEST CURRENT/VOLTAGE VALUES (All Temperatures)											
	mA			Volts								
	I_{OL}	I_{OH}	I_{IC}	V_{IL}	V_{IH}	V_{IHH}	V_{RH}	V_{ILT}	V_{IHT}	V_{CCL}	V_{CCH}	
MC12520	8.0	0.2	-10	0.5	2.4	5.5	4.0	0.7	2.0	4.5	5.5	
MC12020	8.0	0.2	-10	0.5	2.4	5.5	4.0	0.7	2.0	4.75	5.25	

Characteristic	Symbol	Pin Under Test	MC12520 Test Limits -55 to +125°C Min	Max	Unit	MC12020 Test Limits -30 to +85°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL}	I_{OH}	I_{IC}	V_{IL}	V_{IH}	V_{IHH}	V_{RH}	V_{ILT}	V_{IHT}	V_{CCL}	V_{CCH}	Pulse 1	Pulse 2	Gnd
Input																						
Forward Current	I_{IL}	1	-1.0	--	mAdc	-1.0	--	mAdc	--	--	--	1	--	--	10	--	--	--	14	--	--	7
		10	-0.75	--	mAdc	-0.75	--	mAdc	--	--	--	1,10	--	--	--	--	--	--	14	--	--	7
		13	-1.0	--	mAdc	-1.0	--	mAdc	--	--	--	13	--	--	--	--	--	--	14	--	--	7
Leakage Current*	I_{IH}	10	--	150	µAdc	--	150	µAdc	--	--	--	1	10	--	--	--	--	--	14	10	--	7
		1	--	↓	µAdc	--	↓	µAdc	--	--	--	--	1	--	10	--	--	--	14	--	--	7
		13	--		µAdc	--		µAdc	--	--	--	--	13	--	--	--	--	--	14	--	--	7
	I_{IHH}	10	--	1.0	mAdc	--	1.0	mAdc	--	--	--	1	--	10	--	--	--	--	14	10	--	7
		**	--	--	--	--	--	--	--	--	--	10	--	--	1	--	--	--	14	--	10	7
		1	--	1.0	mAdc	--	1.0	mAdc	--	--	--	--	--	1	10	--	--	--	14	--	--	7
		13	--	1.0	mAdc	--	1.0	mAdc	--	--	--	--	--	13	--	--	--	--	14	--	--	7
Clamp Voltage	V_{IC}	1	-1.5	--	Vdc	-1.5	--	Vdc	--	--	1	--	--	--	10	--	--	14	--	--	--	7
		10	-1.5	--	Vdc	-1.5	--	Vdc	--	--	10	--	--	--	1	--	--	14	--	--	--	7
		13	-1.5	--	Vdc	-1.5	--	Vdc	--	--	13	--	--	--	--	--	--	14	--	--	--	7
Output	V_{OL}	3	--	0.5	Vdc	--	0.5	Vdc	5	--	--	--	--	--	--	1,10	--	14	--	--	--	7
Output Voltage*		**	--	--	--	--	--	--	--	--	--	--	--	--	--	1	--	14	--	10	--	7
		3	--	0.5	Vdc	--	0.5	Vdc	3	--	--	--	--	--	--	--	1,10	14	--	--	--	7
		11	--	0.5	Vdc	--	0.5	Vdc	11	--	--	--	--	--	--	--	13	14	--	--	--	7
	V_{OH}	3	2.4	--	Vdc	2.4	--	Vdc	--	3	--	--	--	--	--	1,10	--	14	--	--	--	7
		5	2.4	--	Vdc	2.4	--	Vdc	--	5	--	--	--	--	--	1	10	14	--	--	--	7
		11	2.4	--	Vdc	2.4	--	Vdc	--	11	--	--	--	--	--	13	--	14	--	--	--	7
Short Circuit Current*	I_{OS}	3	-38	--	mAdc	-38	--	mAdc	--	--	--	1	--	--	10	--	--	--	14	10	--	3,7
		5	-38	--	mAdc	-38	--	mAdc	--	--	--	1	--	--	10	--	--	--	14	--	--	5,7
		11	-38	--	mAdc	-38	--	mAdc	--	--	--	13	--	--	--	--	--	--	14	--	--	7,11
Power Requirements (Total Device)																						
Power Supply	I_{PD}	14	--	96	mAdc	--	96	mAdc	--	--	--	--	--	--	--	--	--	--	14	--	--	7



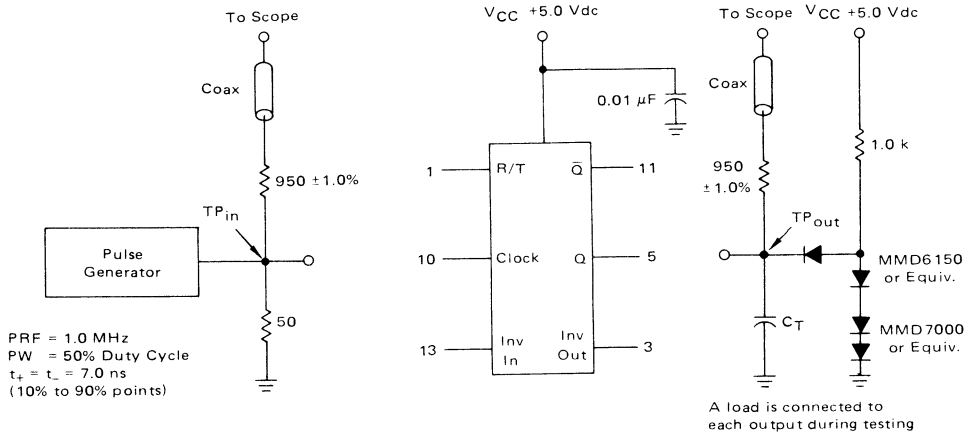
ELECTRICAL CHARACTERISTICS

Test procedures are shown only for selected inputs and outputs. Other inputs and outputs are tested in a similar manner.



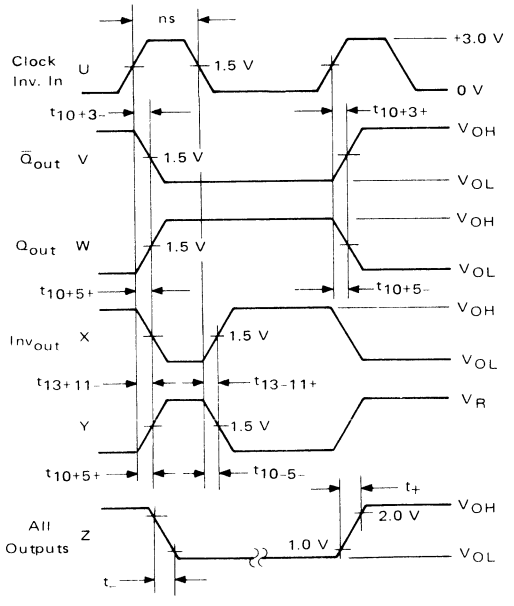
			TEST CURRENT/VOLTAGE VALUES (All Temperatures)														
			mA					Volts									
			I_{OL1}	I_{OL2}	I_{OH1}	I_{OH2}	I_{IC}	V_{IL}	V_{IH}	V_{IHH}	V_{RH}	V_{ILT}	V_{IHT}	V_{CCL}	V_{CCH}		
		MC12521	13	16	0.4	0.1	10	0.5	2.4	5.5	4.0	0.7	2.0	4.5	5.5		
		MC12021	13	16	0.4	0.1	10	0.5	2.4	5.5	4.0	0.7	2.0	4.75	5.25		
Characteristic	Symbol	Pin Under Test	MC12521 Test Limits 55 to +125°C Min	Max	Unit	MC12021 Test Limits -30 to +85°C Min	Max	Unit	TEST CURRENT/VOLTAGE APPLIED TO PINS LISTED BELOW: I_{OL1}	I_{OL2}	I_{OH1}	I_{OH2}	I_{IC}	V_{IL}	V_{IH}	V_{IHH}	V_{RH}	V_{ILT}	V_{IHT}	V_{CCL}	V_{CCH}	Gnd
Input																					
Forward Current	I_{IL}	1	-0.12		mAdc	-0.12		mAdc						1			9				8
		2	-0.12		mAdc	-0.12		mAdc						2,9			-			16	8
		9	-0.12		mAdc	-0.12		mAdc						9						16	8
Leakage Current	I_{IH}	1		40	µAdc		40	µAdc						9	1					16	8
		2		40	µAdc		40	µAdc							2		9			16	8
		9		40	µAdc		40	µAdc							9					16	8
	I_{IHH}	1		1.0	mAdc		1.0	mAdc						9		1				16	8
		2		1.0	mAdc		1.0	mAdc								2	9			16	8
		9		1.0	mAdc		1.0	mAdc								9				16	8
Clamp Voltage	V_{IC}	1	-1.5		Vdc	-1.5		Vdc					1						16		8
		2	-1.5		Vdc	-1.5		Vdc					2						16		8
		9	-1.5		Vdc	-1.5		Vdc					9						16		8
Output																					
Output Voltage	V_{OL}	6		0.5	Vdc		0.5	Vdc		6								9,10	1,2,11,12, 13,14,15	16	8
		7		0.5	Vdc		0.5	Vdc	7									9	1,2,10,11, 12,13,14,15	16	8
	V_{OH}	6	2.4		Vdc	2.4		Vdc				6						1,13,15	2,9,10,11, 12,14	16	8
		7	2.4		Vdc	2.4		Vdc			7							1,11,13,15	2,9,10, 12,14	16	8
Short Circuit Current	I_{OS}	6	-8.0		mAdc	-8.0		mAdc										1,13,15	2,9,10,11, 12,14		16	6,8
		7	-70		mAdc	-70		mAdc										1,11,13,15	2,9,10,12, 14		16	7,8
Power Requirements (Total Device)																					
Power Supply	I_{PDL}	16		94	mAdc		94	mAdc						1,2,9,10, 11,12,13, 14,15						16	8

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS FOR MC12020, MC12520



C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.
The coax delays from input to scope and output to scope must be matched.
The scope must be terminated in 50-ohm impedance. The 950-ohm resistor and the scope termination impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

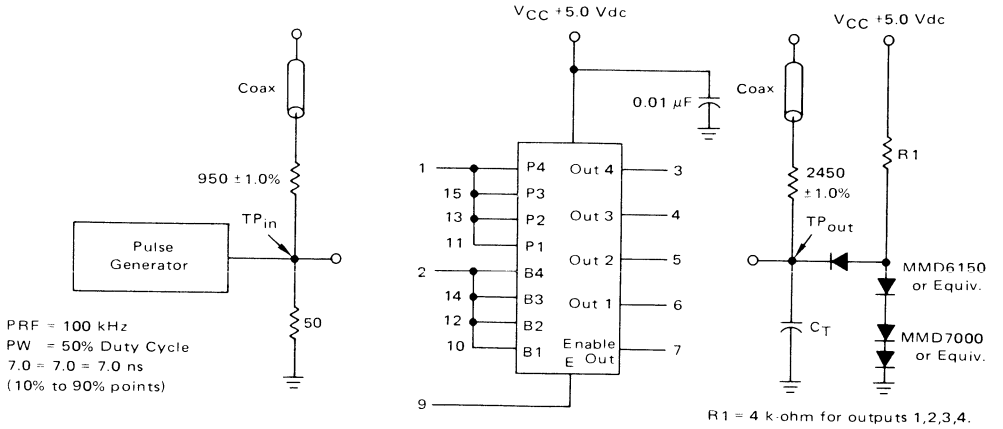
PROPAGATION DELAY TIMES



AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc, waveform letters refer to the waveforms)

Characteristic	Symbol	Pin Under Test In	Pin Under Test Out	Test Limits (ns) MC12020/520 -55°C to +25°C Typ	Test Limits (ns) MC12020/520 +85°C to +125°C Max	Pulse Gen. Wave form	Pulse Gen. Pin	Pulse Out Wave form	Pulse Out Pin	Voltage Applied to Pins Listed Below 2.4 V	Voltage Applied to Pins Listed Below 0.5 V
Propagation Delay	t_{10+3-}	10	3	95	87	U	10	V	3	1	
	t_{10+3-}	10	3	56	48	U	10	V	3	1	
	t_{10+5+}	10	5	47	48	U	10	W	5	1	
	t_{10+5-}	10	5	99	87	U	10	W	5	1	
	t_{10+5+}	10	5	47	48	U	10	Y	5		1
	t_{10-5-}	10	5	29	36	U	10	Y	5		1
	t_{13+11-}	13	11	56	33	U	13	X	11		
	t_{13-11+}	13	11	18	50	U	13	X	11		
Risetime	t_{3-}	10	3	111	18	U	10	Z	3	1	
	t_{5+}	10	5	8.7	17	U	10	Z	5	1	
	t_{11+}	13	11	18	35	U	13	Z	11		
Falltime	t_3	10	3	3.5	3.5	U	10	Z	3	1	
	t_5	10	5	4.0	4.6	U	10	Z	5	1	
	t_{11}	13	11	3.4	3.3	U	13	Z	11		

SWITCHING TIME TEST CIRCUIT AND WAVEFORMS FOR MC12021, MC12521

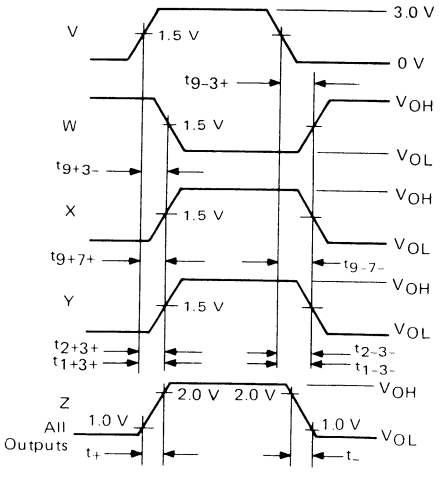


R1 = 4 k-ohm for outputs 1,2,3,4.
R1 = 500-ohm for Enable Out.

C_T = 15 pF = total parasitic capacitance, which includes probe, wiring, and load capacitances.

The coax delays from input to scope and output to scope must be matched.
The scope must be terminated in 50-ohm impedance. The 2450-ohm resistor and the scope termination impedance constitute a 50:1 attenuator probe. The 950 Ω resistor and the scope impedance constitute a 20:1 attenuator probe. Coax shall be CT-070-50 or equivalent.

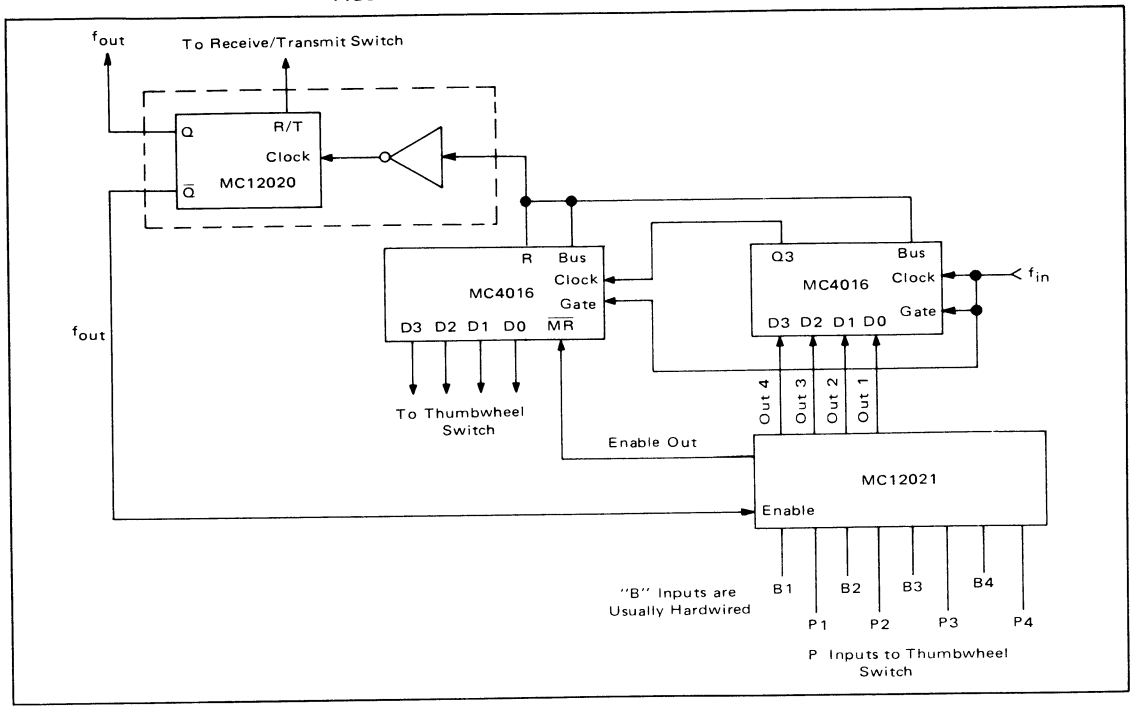
PROPAGATION DELAY TIMES



AC ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 Vdc ± 5%, unless otherwise noted; see waveforms.)

Characteristic	Symbol	Pin Under Test		Test Limits (ns) MC12021/521		Pulse Gen.		Pulse Out		Voltage Applied to Pins Listed Below	
				55°C to +25°C	+85°C to +125°C	Wave form	Pin	Wave form	Pin	2.4 V	0.5 V
		In	Out	Typ	Max						
Propagation Delay	t_{g-3+}	9	3	234	237	V	9	W	3	2	1
	t_{g-3-}	9	3	108	112	V	9	W	3	2	1
	t_{2-3}	2	3	164	171	V	2	Y	3	1	9
	t_{2+3-}	2	3	129	119	V	2	Y	3	1	9
	t_{1-3}	1	3	163	170	V	1	Y	3	9	2
	t_{1-3-}	1	3	128	117	V	1	Y	3	9	2
	t_{g-7}	9	7	80	84	V	9	X	7	2	1
	t_{g-7-}	9	7	128	147	V	9	X	7	2	1
Risetime	t_{3-}	9	3	23	32	V	9	Z	3	2	1
	t_{7-}	9	7	96	12	V	9	Z	7	2	1
Falltime	t_3	9	3	18	21	V	9	Z	3	2	1
	t_7	9	7	20	23	V	9	Z	7	2	1

FIGURE 1 – BASIC DUAL PRESETTING TECHNIQUE



APPLICATION INFORMATION

The frequency generating section of a multichannel transceiver must be capable of two major functions: 1) generate the exact transmit frequency for any one of many channels selectable by a front panel control, and 2) offset, within milliseconds, the transmit frequency by plus (or minus) the intermediate frequency (IF) when the receive mode is selected. The digitally programmed frequency synthesizer (PLL) is well suited to the solution of multichannel frequency generation, and its use as the local oscillator in channelized transceivers is widely accepted. With the parts and literature available, the implementation of a synthesizer to generate a band of channelized frequencies is straightforward with only the V_{CO} and loop filter left as design variables. A synthesizer allows channel selection by the use of front panel thumbwheel switches which display the transmit frequency selected.

Several methods exist for obtaining the frequency offset required during receive. Unfortunately, none of the present techniques offer a universal solution for all transceivers. Three methods for frequency offsetting presently available to the transceiver designer are mixing, direct logic implementation, and adders. The mixing method is widely used because of price and simplicity. The mixing technique has the disadvantage of: 1) requiring an additional oscillator at the IF frequency; 2) except for applications requiring a narrow tuning range, the tank circuit for the mixer must be designed to track the synthesizer oscillator; and 3) spurious frequencies are generated which can severely degrade system performance.

For certain applications where tuning range is wide and the IF frequency is simple (10 MHz, 20 MHz, etc.) the addition of logic circuitry to the programming inputs to add, on command, the IF frequency to the transmit frequency is simple and inexpensive. This technique is used in several aircraft radios built today. The technique becomes prohibitive because of logic complexity, number of packages, and power for standard IF frequencies, such as 10.7 MHz, 21.4 MHz, etc., and for frequency bands where the IF offset cannot be accomplished by adding (or subtracting) a number to the most significant divider in the divider chain.

Adders offer a universal solution for frequency offsetting for any IF frequency but are used in very few applications because of: 1) the large number of packages required; 2) power dissipation; 3) the price; and 4) the difficulty of obtaining NBCD adders.

The MC12020/520 (offset control) and the MC12021/521 (offset programmer) combination offers a new method for frequency offsetting. The new method is referred to as "dual presetting" and allows the implementation of any IF frequency in a very straightforward manner. The complexity of the system depends on the IF frequency required, but is always less complex than the adder method and is

competitive with the direct implementation method for specific applications.

The dual presetting method is applied in the low frequency section of a synthesizer and does not require high performance, high powered units to accomplish its function. The method does not require an additional oscillator and tank circuits as does the mixing method.

The dual presetting (MC12020 and MC12021) system produces the required shift in frequency by adding the IF frequency to the transmit frequency. The system accom plishes this addition by alternately programming the divide counters to the transmit frequency and the IF frequency.

The MC12020/520 is a modified D-type flip-flop that is capable of two modes of operation. The mode is controlled by the R/T (Receive/Transmit) input. With the R/T input at a logical one level, the part divides by two at both the Q and $\overline{Q}$ outputs. With the R/T input at a logical zero level, the Q output becomes a buffer gate that follows the clock input, and the $\overline{Q}$ output produces a logical one level. An inverter gate is provided which can be used to invert the clock polarity of the MC12020. This option is to ensure the MC12020 can always be clocked on the same edge that clears the counter presets.

The MC12021/521 is an eight-input, four-output data selector constructed from low level TTL gates. It is the logic implementation of a four-pole, two-position switch with the switch position controlled by the enable input. A buffer output that follows the enable input is provided and can be used to program divide counters to zero when necessary.

The operation of the dual presetting method can best be described for one MC12020, one MC12021 and two MC4016 counters (see Figure 1). The transmit code (N1) is seventeen (0001, 0111) and the IF code (N2) is eight (0000, 1000). The buffer out of the MC12021 is connected to the master reset ($\overline{MR}$) of the most significant counter (MS). The outputs of the MC12021 are connected to the programming inputs of the least significant (LS) counter. The number one is programmed into the MS counter programming inputs, and the numbers seven and eight are programmed into the P and B inputs, respectively, of the MC12021. The inverter gate in the MC12020 is used to invert the bus out from the counters allowing the MC12021

FIGURE 2 – TIMING DIAGRAM FOR SYSTEM OF FIGURE 1 (R/T Input High)

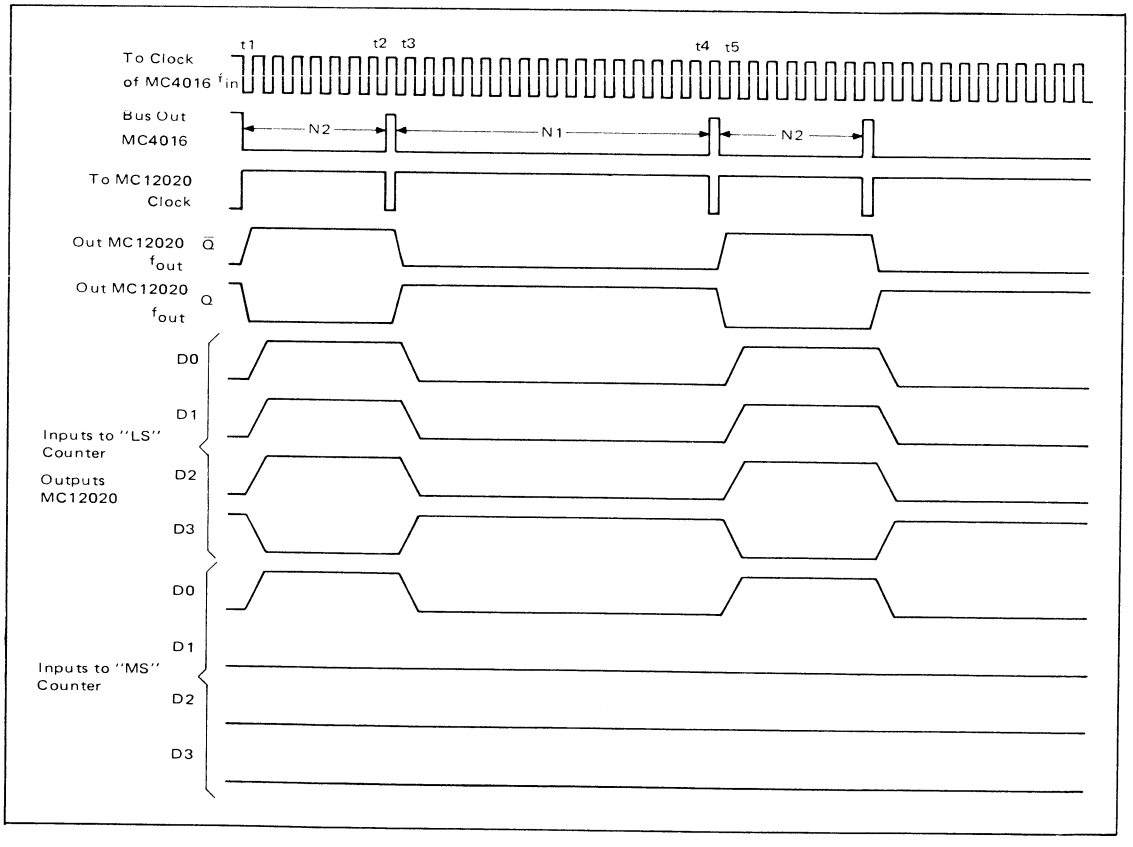
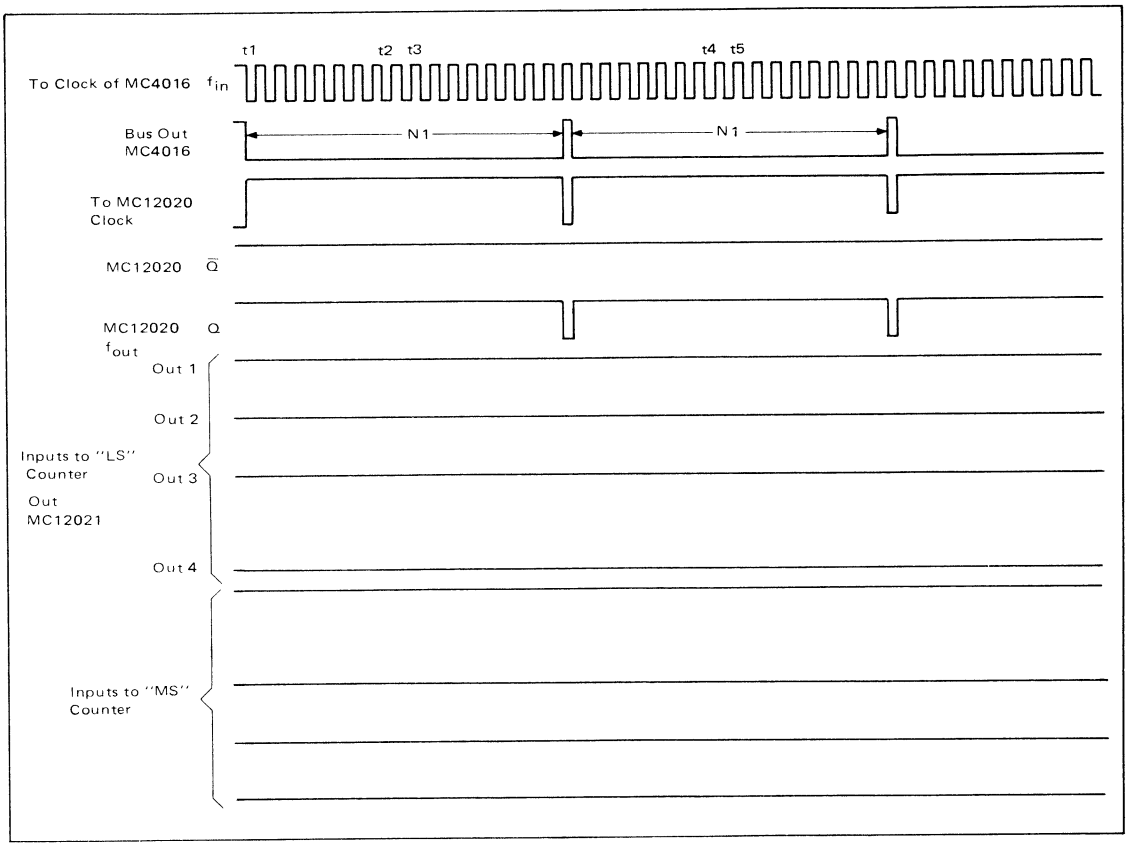


FIGURE 3 – TIMING DIAGRAM FOR SYSTEM OF FIGURE 1 (R/T Input Low)



the maximum time to change the counters' programming.

To illustrate the operation of the system, assume the R/T input at a logical one level, the Q out is a logical one, the counters have been decremented to zero, and the bus output has just gone to a logical one level (see Figure 2). The $\overline{Q}$ output is a logical zero level, the number eight is on the programming inputs of the LS counter, the number zero is on the $\overline{MR}$ of the MS counter, and the preset logic of the counters is enabled.

The negative transition of the clock at t1 presets the number eight in the LS counter and zero in the MS counter. The change in programming forces the bus output to a logical zero level, inhibiting the counter preset logic, changing the state of the MC12020, and enabling the counters. The state change of the MC12020 puts the $\overline{Q}$ output at a logical one level which forces the MC12021 to route the number seven to the LS counter and clears the zero from the $\overline{MR}$ of the MS counter allowing the number one to be programmed. Since the counters preset new information only when the bus output is high, the changing numbers have no effect until the next positive transition of the bus output. The positive transition at t2 decrements the counters to zero causing the bus output to go high enabling the counter presets. The negative transition of the clock at t3 presets the number one and seven into the MS and LS counters, respectively. The bus output goes low, clears the preset, enables the count down, and clocks the MC12020. The $\overline{Q}$ output goes low routing zero and eight counters. Seventeen clock pulses later the transition at t4 and t5 brings the system back to the initial conditions completing one cycle. The system will continue in a like manner until the R/T input is taken low. The frequency out will be the frequency in divided by N1 plus N2 ($f_{in} \div [8+17]$). The MC12020 and MC12021 combination has added the IF code to the transmit code by alternately programming the divide counters to N1 and N2.

The R/T input is taken low to place the MC12020 in the transmit mode. The logical zero on the R/T input forces the $\overline{Q}$ output to a logical one level selecting, through the MC12021, code N1. The $\overline{Q}$ output will remain a logical

one and the Q output will follow the input to the MC12020 until the R/T input is taken high.

For purposes of description, assume that some time prior to the transition at t1 (see Figure 3) the R/T input was taken low. The transitions at t1 and t2 program the counters to N1 and seventeen clock pulses later the transitions at t3 and t4 repeat the process. As long as the R/T input remains low the code on the counter inputs will remain unchanged and the output frequency will be the input frequency divided by N1 ($f_{in} \div 17$).

The operation for this simplified system is valid for any number of MC12021's and counters. The number of MC12021's required by any system is a function of the required IF frequency. The number needed to implement a given IF frequency is equal to the number of non-zero integers in the IF frequency. The buffer output of the MC12021 and the master reset on the MC4016's allow zeros to be programmed without the addition of a package. For example, the IF of 67.02 MHz requires three MC12021's while the IF of 100.02 MHz requires only two.

The synthesizer shown in Figure 4 is designed to operate over the aircraft frequencies from 118 to 136 MHz in 25 kHz steps while in the transmit mode and will add 10.7 MHz to any transmit frequency in the receive mode. The synthesizer is a typical phase-lock loop (PLL) system that uses one MC12020 and two MC12021's. The system's mode of operation is controlled by the R/T input of the MC12020; a logical one for receive mode and a logical zero for transmit mode.

The MC12020/520 and MC12021/521 are implemented

FIGURE 4 – TYPICAL PLL SYNTHESIZER SYSTEM USING MC12020/520, MC12021/521 CIRCUITS TO ACCOMPLISH IF OFFSET

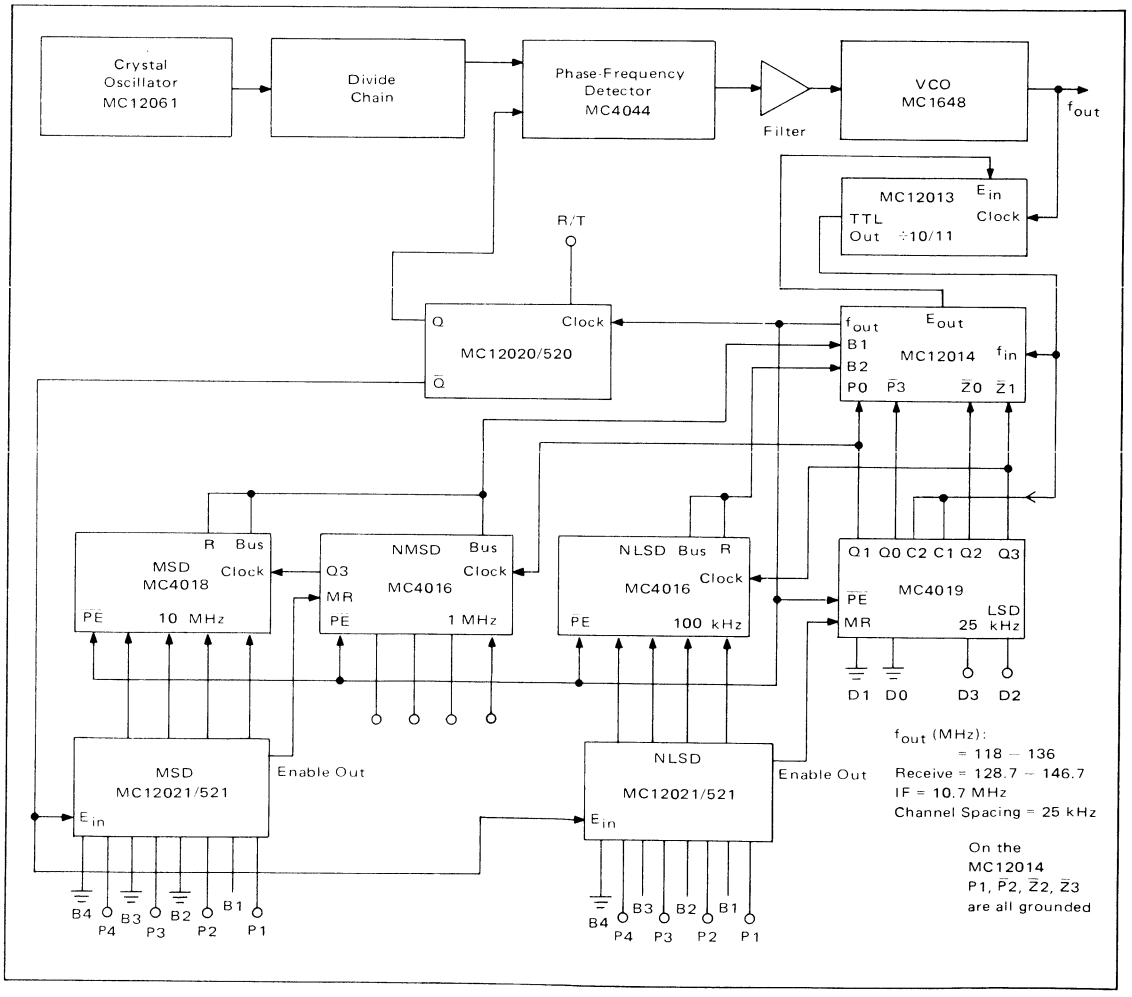


FIGURE 5 – PROGRAMMING EXAMPLES FOR SYNTHESIZER SYSTEM OF FIGURE 4

	← ÷N_p Counter →			← ÷A Counter →	
Sample Transmit/Receive Frequency (MHz)	MSD MC4018	NMSD MC4016	÷4 P/O MC4019	NLSD MC4016	LSD P/O MC4019
118.000	11	8	4	0	0
.025	11			0	1
.050	11			0	2
.075	11			0	3
.100	11			1	0
.125	11			1	1
.150	11			1	2
.175	11			1	3
.200	11			2	0
↓	↓	↓		↓	↓
119.000	11	9		0	0
↓	↓	↓		↓	↓
120.175	12	0		1	3
↓	↓	↓		↓	↓
128.000	12	8		0	0
↓	↓	↓		↓	↓
136.000	13	6		10	10

NOTE: Columns below counters indicate the number to be programmed into that respective counter. For direct frequency, read out the four programming switches as viewed from the front panel, display the same column numbers, except for the LSD switch. The LSD switch displays 00, 25, 50, and 75 when programmed for 0, 1, 2, and 3 respectively.

to add the IF offset for the receive mode as described previously. Programming details for the balance of the counting system are as follows:

The MC4019 contains two modulo four counters. One of these forms the LSD section of the ÷A counter and is programmed by D2 and D3 to divide by 0, 1, 2, or 3. The second modulo four counter acts as a fixed divide by four and forms the LSD counter for the ÷Np counter (see MC12012 data sheet for a discussion of ÷A and ÷Np counters in conjunction with two modulus prescaling). The NLSD counter makes up the rest of the ÷A counter and provides for 100 kHz frequency increments. The rest of the ÷Np counter is formed by the NMSD and MSD counters which provide for 1 MHz and 10 MHz steps respectively.

Direct frequency readout is easily achieved as shown by the example frequencies in Figure 5. Note that a four section selector can be used to generate the necessary programming.

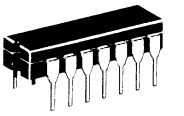
The dual presetting method offers an efficient and economical solution to the problem of IF offsetting, and the MC12020 and MC12021 make implementation straightforward.

PHASE-FREQUENCY DETECTOR

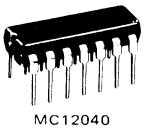
MC12040
MC12540

The MC12040/MC12540 is a phase-frequency detector intended for use in systems requiring zero phase and frequency difference at lock. In combination with a voltage controlled oscillator (such as the MC1648), it is useful in a broad range of phase-locked loop applications. Operation of this device is very similar to that of Phase Detector #1 of the MC4044. A discussion of the theory of operation and applications information is given on the MC4344/4044 data sheet.

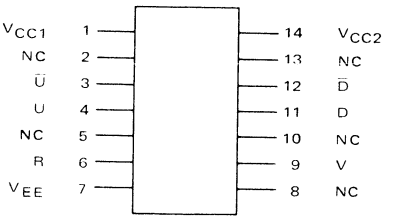
- Operating Frequency = 70 MHz Min. -55° to +125°C



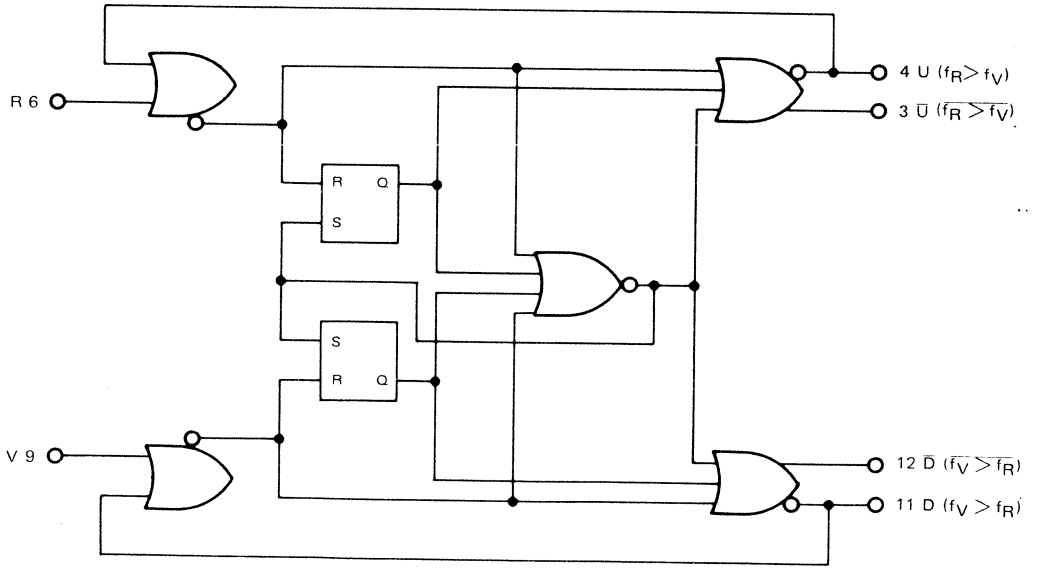
MC12040 – MC12540
CERAMIC PACKAGE
CASE 632-02



MC12040
P SUFFIX
PLASTIC PACKAGE
CASE 648



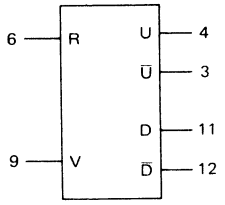
NC – No Connection



V_{CC1} = Pin 1
V_{CC2} = Pin 14
V_{CC3} = Pin 7

ELECTRICAL CHARACTERISTICS – MC12040

The MC12040 has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 50 ohm resistor to +3.0 V for +5.0 V tests and through a 50 ohm resistor to -2.0 V for -5.2 V tests.



INPUT		OUTPUT			
R	V	U	D	Ū	D̄
0	0	X	X	X	X
0	1	X	X	X	X
1	1	X	X	X	X
0	1	X	X	X	X
1	1	1	0	0	1
0	1	1	0	0	1
1	1	1	0	0	1
1	0	1	0	0	1
1	1	0	0	1	1
1	0	0	0	1	1
1	1	0	1	1	0
1	0	0	1	1	0
1	1	0	1	1	0
0	1	0	1	1	0
1	1	0	0	1	1

X = Don't Care

TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not cover all possibile modes of operation. However it gives a sufficient number of tests to ensure that the device will function properly in all modes of operation.

@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}
0°C	-0.840	-1.870	-1.145	-1.490	-5.2
25°C	-0.810	-1.850	-1.105	-1.475	-5.2
75°C	-0.720	-1.830	-1.045	-1.450	-5.2

Supply Voltage = -5.2V

Characteristic	Symbol	Pin Under Test	MC12040 0°C Min	0°C Max	25°C Min	25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	7			-120	-60			mAdc						1,14
Input Current	I_{INH}	6 9				350 350			µAdc µAdc	6 9				7 7	1,14 1,14
Logic "1" Output Voltage	V_{OH} (1)	3 4 11 12	-1.000	-0.840	-0.960	-0.810	-0.900	-0.720	Vdc					7	1,14
Logic "0" Output Voltage	V_{OL} (1)	3 4 11 12	-1.870	-1.635	-1.850	-1.620	-1.830	-1.595	Vdc					7	1,14
Logic "1" Threshold Voltage	V_{OHA} (2)	3 4 11 12	-1.020		-0.980		-0.920		Vdc			6,9		7	1,14
Logic "0" Threshold Voltage	V_{OLA} (2)	3 4 11 12		-1.615		-1.600		-1.575	Vdc			9 6 9 6	6 9 6 9	7	1,14

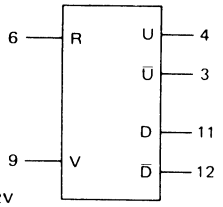
@ Test Temperature	TEST VOLTAGE VALUES (Volts) $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{CC}
0°C	+4.160	+3.130	+3.855	+3.510	+5.0
25°C	+4.190	+3.150	+3.895	+3.525	+5.0
75°C	+4.280	+3.170	+3.955	+3.550	+5.0

Supply Voltage = +5.0V

Characteristic	Symbol	Pin Under Test	MC12040 0°C Min	0°C Max	25°C Min	25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW $V_{IH\ max}$	$V_{IL\ min}$	$V_{IHA\ min}$	$V_{ILA\ max}$	V_{CC}	(V_{EE}) Gnd
Power Supply Drain Current	I_E	7			-115	-60			mAdc					1,14	7
Input Current	I_{INH}	6 9				350 350			µAdc µAdc	6 9				1,14 1,14	7 7
	I_{INL}	6 9			0.5 0.5				µAdc µAdc		6 9			1,14 1,14	7 7
Logic "1" Output Voltage	V_{OH} (1)	3 4 11 12	4.000	4.160	4.040	4.190	4.100	4.280	Vdc					1,14	7
Logic "0" Output Voltage	V_{OL} (1)	3 4 11 12	3.190	3.430	3.210	3.440	3.230	3.470	Vdc					1,14	7
Logic "1" Threshold Voltage	V_{OHA} (2)	3 4 11 12	3.980		4.020		4.080		Vdc			6,9		1,14	7
Logic "0" Threshold Voltage	V_{OLA} (2)	3 4 11 12		3.450		3.460		3.490	Vdc			9 6 9 6	6 9 6 9	1,14	7

ELECTRICAL CHARACTERISTICS – MC12540

The MC12540 has been designed to meet the dc specifications shown in the test table after thermal equilibrium has been established. Outputs are terminated through a 100 ohm resistor to +3.0 V for +5.0 V tests and through a 100 ohm resistor to -2.0 V for -5.2 V tests. The package should be housed in a heat sink, capable of maintaining junction temperatures ≤ 165°C.



INPUT		OUTPUT			
R	V	U	D	Ū	D̄
0	0	X	X	X	X
0	1	X	X	X	X
1	1	X	X	X	X
0	1	X	X	X	X
1	1	1	0	0	1
0	1	1	0	0	1
1	1	1	0	0	1
1	0	1	0	0	1
1	1	0	0	1	1
1	0	0	0	1	1
1	1	0	1	1	0
1	0	0	1	1	0
1	1	0	1	1	0
0	1	0	1	1	0
1	1	0	0	1	1

X = Don't Care

TRUTH TABLE

This is not strictly a functional truth table; i.e., it does not cover all possibile modes of operation. However it gives a sufficient number of tests to ensure that the device will function properly in all modes of operation.

Supply Voltage = -5.2V

@ Test Temperature	TEST VOLTAGE VALUES (Volts)				
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}
-55°C	-0.880	-1.920	-1.255	-1.510	-5.2
25°C	-0.780	-1.850	-1.105	-1.475	-5.2
+125°C	-0.630	-1.820	-1.000	-1.400	-5.2

Characteristic	Symbol	Pin Under Test	MC12540 -55°C Min	-55°C Max	25°C Min	25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{EE}	(V_{CC}) Gnd
Power Supply Drain Current	I_E	7			-120	-60			mAdc					7	1,14
Input Current	I_{INH}	6 9				350 350			µAdc µAdc	6 9				7 7	1,14 1,14
Logic "1" Output Voltage	V_{OH} (1)	3 4 11 12	-1.080	-0.880	-0.930	-0.780	-0.825	-0.630	Vdc					7	1,14
Logic "0" Output Voltage	V_{OL} (1)	3 4 11 12	-1.920	-1.655	-1.850	-1.620	-1.820	-1.545	Vdc					7	1,14
Logic "1" Threshold Voltage	V_{OHA} (2)	3 4 11 12	-1.000		-0.950		-0.845		Vdc			6,9		7	1,14
Logic "0" Threshold Voltage	V_{OLA} (2)	3 4 11 12		-1.635		-1.600		-1.525	Vdc			9 6 9 6	6 9 6 9	7	1,14

Supply Voltage = +5.0V

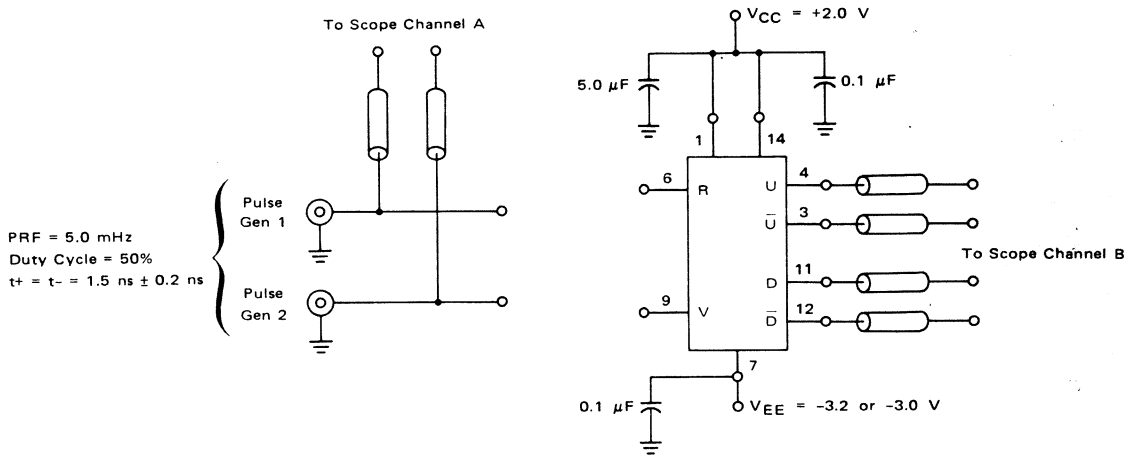
@ Test Temperature	TEST VOLTAGE VALUES (Volts)				
	V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{CC}
-55°C	+4.120	+3.080	+3.745	+3.490	+5.0
25°C	+4.220	+3.150	+3.895	+3.525	+5.0
+125°C	+4.370	+3.180	+4.000	+3.600	+5.0

Characteristic	Symbol	Pin Under Test	MC12540 -55°C Min	-55°C Max	25°C Min	25°C Max	+125°C Min	+125°C Max	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW: V_{IH} max	V_{IL} min	V_{IHA} min	V_{ILA} max	V_{CC}	(V_{EE}) Gnd
Power Supply Drain Current	I_E	7	-		-115	-60	-		mAdc	-	-	-	-	1,14	7
Input Current	I_{INH}	6 9			-	350 350	-	-	µAdc µAdc	6 9	-	-	-	1,14 1,14	7 7
	I_{INL}	6 9			0.5 0.5				µAdc µAdc	-	6 9	-	-	1,14 1,14	7 7
Logic "1" Output Voltage	V_{OH} (1)	3 4 11 12	3.920	+4.120	4.070	+4.220	4.175	+4.370	Vdc					1,14	7
Logic "0" Output Voltage	V_{OL} (1)	3 4 11 12	3.140	3.405	3.210	3.440	3.240	3.515	Vdc					1,14	7
Logic "1" Threshold Voltage	V_{OHA} (2)	3 4 11 12	3.900		4.050		4.155		Vdc			6,9		1,14	7
Logic "0" Threshold Voltage	V_{OLA} (2)	3 4 11 12		3.425		3.460		3.535	Vdc			9 6 9 6	6 9 6 9	1,14	7

(1) Outputs of the device must be tested by sequencing through the truth table. All input, power supply and ground voltages must be maintained between tests.

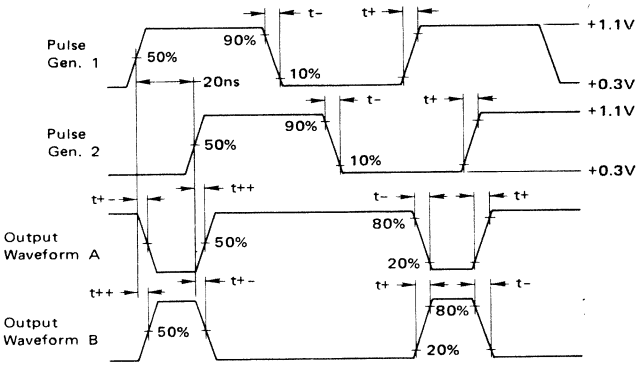
(2) The device must also function according to the truth table during these tests.

AC TESTS



NOTES:

1. All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.
2. Unused input and outputs are connected to a 50 Ω (MC12040) and 100 Ω (MC12540) resistor to ground.
3. The device under test must be preconditioned before performing the ac tests. Preconditioning may be accomplished by applying pulse generator 1 for a minimum of two pulses prior to pulse generator 2. The device must be preconditioned again when inputs to pins 6 and 9 are interchanged. The same technique applies.



Characteristic	Symbol	Pin Under Test	Output Waveform	MC12040 0°C Max	MC12040 +25°C Max	MC12040 +75°C Max	MC12540 -55°C Max	MC12540 +25°C Max	MC12540 +125°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse Gen. 1	Pulse Gen. 2	VEE -3.0 or -3.2 V	VCC +2.0 V
Propagation Delay	t_{6+4+}	6,4	B	4.6	4.6	5.6	4.6	4.6	5.0	ns	6	9	7	1,14
	t_{6+12+}	6,12	A	6.0	6.0	7.2	6.0	6.0	6.6		9	6		
	t_{6+3-}	6,3	A	4.5	4.5	5.5	4.5	4.5	4.9		6	9		
	t_{6+11-}	6,11	B	6.4	6.4	7.7	6.4	6.4	7.0		9	6		
	t_{9+11+}	9,11	B	4.6	4.6	5.6	4.6	4.6	5.0		9	6		
	t_{9+3+}	9,3	A	6.0	6.0	7.2	6.0	6.0	6.6		6	9		
	t_{9+12-}	9,12	A	4.5	4.5	5.5	4.5	4.5	4.9		9	6		
	t_{9+4-}	9,4	B	6.4	6.4	7.7	6.4	6.4	7.0		6	9		
Output Rise Time	t_{3+}	3	A	3.4	3.4	3.8	3.4	3.4	3.8	ns	6	9	7	1,14
	t_{4+}	4	B								6	9		
	t_{11+}	11	B								9	6		
	t_{12+}	12	A								9	6		
Output Fall Time	t_{3-}	3	A	3.4	3.4	3.8	3.4	3.4	3.8	ns	6	9	7	1,14
	t_{4-}	4	B								6	9		
	t_{11-}	11	B								9	6		
	t_{12-}	12	A								9	6		

APPLICATIONS INFORMATION

The MC12040/MC12540 is a logic network designed for use as a phase comparator for MECL-compatible input signals. It determines the "lead" or "lag" phase relationship and the time difference between the leading edges of the waveforms. Since these edges occur only once per cycle, the detector has a range of $\pm 2\pi$ radians.

Operation of the device may be illustrated by assuming two waveforms, R and V (Figure 1), of the same frequency but differing in phase. If the logic had established by past history that R was leading V, the U output of the detector (pin 4) would produce a positive pulse width equal to the phase difference and the D output (pin 11) would simply remain low.

On the other hand, it is also possible that V was leading R (Figure 1), giving rise to a positive pulse on the D output and a constant low level on the U output pin. Both outputs for the sample condition are valid since the determination of lead or lag is dependent on past edge crossing and initial conditions at start-up. A stable phase-locked loop will result from either condition.

Phase error information is contained in the output duty cycle – that is, the ratio of the output pulse width to total period. By integrating or low-pass filtering the outputs of the detector and shifting the level to accommodate ECL swings, usable analog information for the voltage-controlled oscillator can be developed. A circuit useful for this function is shown in Figure 2.

Proper level shifting is acomplished by differentially driving the operational amplifier from the normally high outputs of the phase detector ($\overline{U}$ and $\overline{D}$). Using this technique the quiescent differential voltage to the operational amplifier is zero (assuming matched "1" levels from the phase detector). The $\overline{U}$ and $\overline{D}$ outputs are then used to pass along phase information to the operational amplifier. Phase error summing is accomplished through resistors R1 connected to the inputs of the operational amplifier. Some R-C filtering imbedded within the input network (Figure 2) may be very beneficial since the very narrow correctional pulses of the MC12040/MC12540 would not normally be integrated by the amplifier. General design guides for calculating R1, R2, and C are included in the MC4344/MC4044 data sheet. Phase detector gain for this configuration is approximately 0.16 volts/radian.

System phase error stems from input offset voltage in the operational amplitier, mismatching of nominally equal resistors, and mismatching of phase detector "high" states between the outputs used for threshold setting and phase measuring. All these effects are reflected in the gain constant. For example, a 16 mV offset voltage in the amplifier would cause an error of 0.016/0.16 = 0.1 radian or 5.7 degrees of error. Phase error can be trimmed to zero initially by trimming either input offset or one of the threshold resistors (R1 in Figure 2). Phase error over temperature depends on how much the offending parameters drift.

FIGURE 1 – TIMING DIAGRAM

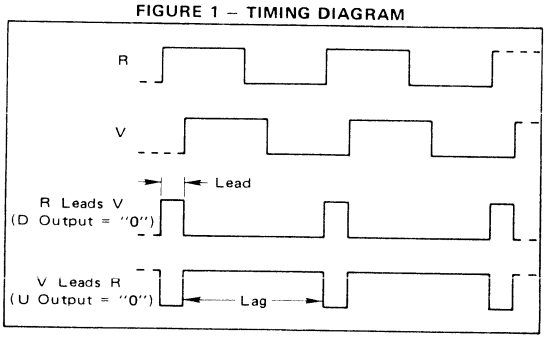
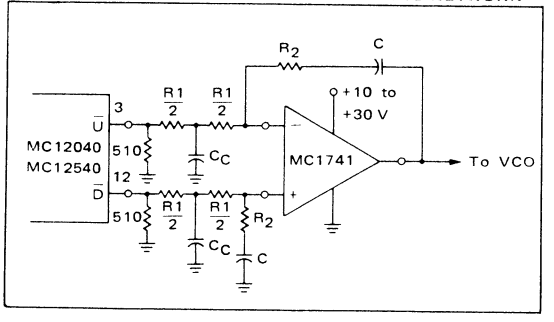
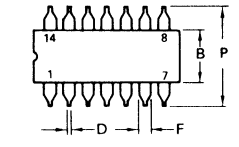
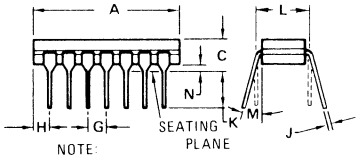


FIGURE 2 – TYPICAL FILTER AND SUMMING NETWORK





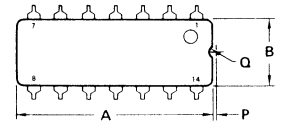


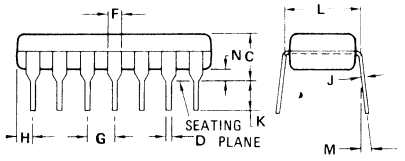
NOTE:
DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	16.8	19.9	0.660	0.785
B	5.59	7.11	0.220	0.280
C	–	5.08	–	0.200
D	0.381	0.584	0.015	0.023
F	0.77	1.77	0.030	0.070
G	2.54 BSC		0.100 BSC	
J	0.203	0.381	0.008	0.015
K	2.54	–	0.100	–
L	7.62 BSC		0.300 BSC	
M	–	15°	–	15°
N	0.51	0.76	0.020	0.030
P	–	8.25	–	0.325

All JEDEC dimensions and notes apply.

CASE 632
TO-116





DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	18.16	18.80	0.715	0.740
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

CASE 646

PLASTIC PACKAGE

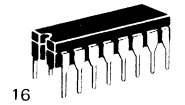
CRYSTAL OSCILLATOR

ISSUE A

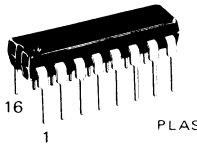
MC12060 • MC12560
MC12061 • MC12561

The MC12060/12560 and MC12061/12561 are designed for use with an external crystal to form a crystal controlled oscillator. In addition to the fundamental series mode crystal, two bypass capacitors are required (plus usual power supply pin bypass capacitors). Translators are provided internally for MECL and MTTL outputs.

- Frequency Range = 100 kHz to 2.0 MHz for MC12060/12560
  = 2.0 MHz to 20 MHz for MC12061/12561
- Temperature Range = -55°C to +125°C for MC12560, 61
  = 0°C to +70°C for MC12060, 61
- Single Supply Operation: +5.0 Vdc or -5.2 Vdc
- Three Outputs Available:
  1. Complementary Sine Wave (600 mVp-p typ)
  2. Complementary MECL
  3. Single Ended MTTL



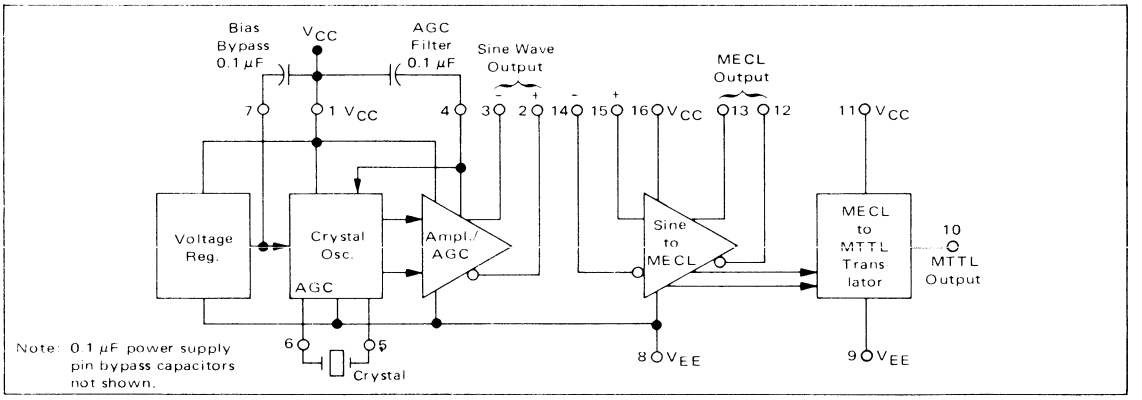
L SUFFIX
CERAMIC PACKAGE
CASE 620



P SUFFIX
PLASTIC PACKAGE
CASE 648

MC12060/MC12061 only.

FIGURE 1 – BLOCK DIAGRAM



TYPICAL CIRCUIT CONFIGURATIONS Note: 0.1 μF power supply pin bypass capacitors not shown.

FIGURE 2 – SINE WAVE OUTPUT

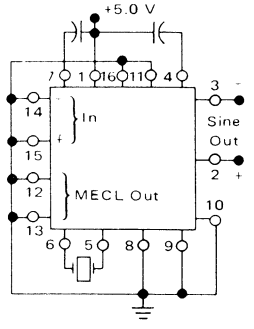


FIGURE 3 – MTTL OUTPUT

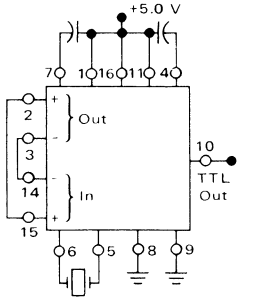


FIGURE 4 – MECL OUTPUT (+5.0 V Supply)

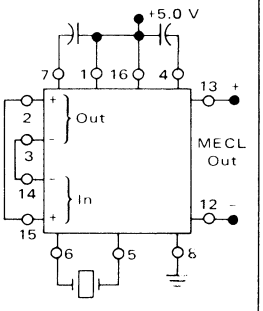
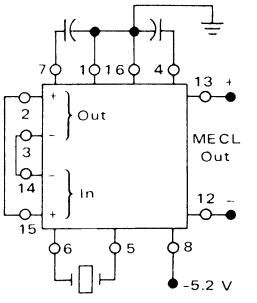


FIGURE 5 – MECL OUTPUT (-5.2 V Supply)

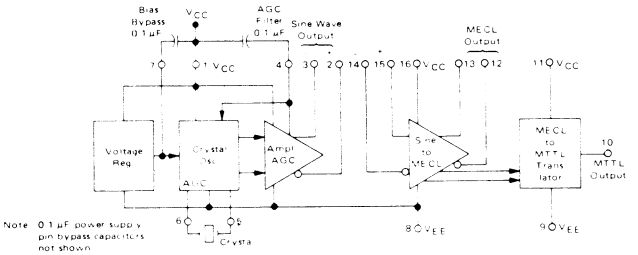


CRYSTAL REQUIREMENTS

Note: Start-up stabilization time is a function of crystal series resistance. The lower the resistance, the faster the circuit stabilizes.

Characteristic	MC12060/12560	MC12061/12561
Mode of Operation	Fundamental Series Resonance	
Frequency Range	100 kHz – 2.0 MHz	2.0 MHz – 20 MHz
Series Resistance, R1	Minimum at Fundamental	
Maximum Effective Resistance, R_E	4 k ohms	155 ohms

ELECTRICAL CHARACTERISTICS

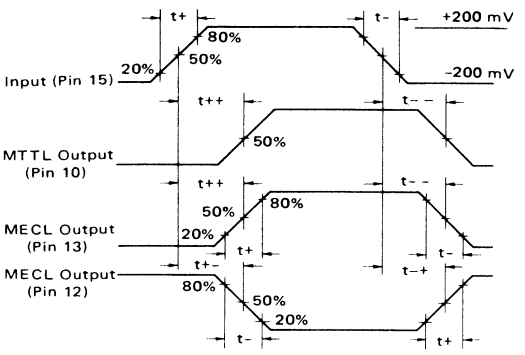


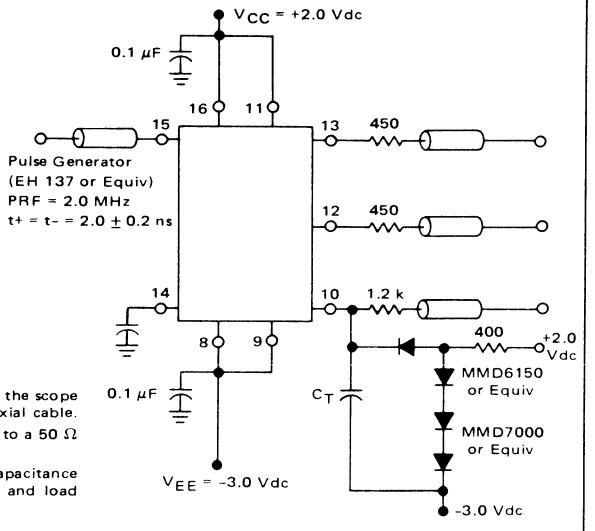
@ Test Temperature		TEST VOLTAGE/CURRENT VALUES											
		Volts								mA			
		V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHT}	V_{CCL}	V_{CC}	V_{CCH}	I_{OL}	I_{OH}	I_L	
MC12560, MC12561	-55°C	4.07	3.18	3.72	3.49	4.0	4.5	5.0	5.5	16	-0.4	-2.5	
	+25°C	4.19	3.21	3.90	3.54	4.0	4.5	5.0	5.5	16	-0.4	-2.5	
	+125°C	4.37	3.25	4.03	3.60	4.0	4.5	5.0	5.5	16	-0.4	-2.5	
MC12060, MC12061	0°C	4.16	3.19	3.86	3.51	4.0	4.75	5.0	5.25	16	-0.4	-2.5	
	+25°C	4.19	3.21	3.90	3.52	4.0	4.75	5.0	5.25	16	-0.4	-2.5	
	+75°C	4.28	3.23	3.96	3.55	4.0	4.75	5.0	5.25	16	-0.4	-2.5	

Characteristic	Symbol	Pin Under Test	MC12560, MC12561 -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	-125°C Min	-125°C Max	MC12060, MC12061 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW V_{IHmax}	V_{ILmin}	V_{IHAmin}	V_{ILAmax}	V_{IHT}	V_{CCL}	V_{CC}	V_{CCH}	I_{OL}	I_{OH}	I_L	Gnd
Power Supply Drain Current – MC12060, 12560 MC12061, 12561	I_{CC}	1	–	–	13	16	19	–	–		–	13	16	19		–	mAdc												
		1	–	–	18	23	28	–	–		–	18	23	28		–												
		11	–	–	–	3.0	4.0	–	–		–		3.0	4.0		–		14	15				–	–	11,16	–	–	–	8,9
		16	–	–	13	16	19	–	–		–	13	16	19		–							–	–	16	–	–	–	8
Input Current	I_{INH}	14	–	–	–	–	250	–	–		–	–	–	250	–	–	µAdc	14	15					–	16	–	–	–	8
		15	–	–	–	–	250	–	–		–	–	–	250	–	–	µAdc	15	14					–	16	–	–	–	8
	I_{INL}	14	–	–	–	–	1.0	–	–		–	–	–	1.0	–	–	µAdc	15						–	16	–	–	–	8,14
		15	–	–	–	–	1.0	–	–		–	–	–	1.0	–	–	µAdc	14						–	16	–	–	–	8,15
Differential Offset Voltage MC12060, 12560 MC12061, 12561	ΔV	4 to 7	–	–	40	–	325	–	–		–	40	–	325	–	–	mVdc	–	–	–	–	5,6	–	1	–	–	–	–	8
		2 to 3	–	–	-220	0	+220	–	–		–	-300	0	+300	–	–		–	–	–	–	4	–	–	–	–	–	–	
		2 to 3	–	–	-100	0	+100	–	–		–	-200	0	+200	–	–		–	–	–	–	4	–	–	–	–	–	–	
Output Voltage Level	V_{out}	2	–	–	–	3.5	–	–	–		–	–	3.5	–	–	–	Vdc	–				4	–	1	–		–		8
		3	–	–	–	3.5	–	–	–		–	–	3.5	–	–	–	Vdc					4	–	1	–		–		8
Logic "1" Output Voltage	V_{OH1}*	12	3.92	4.07	4.04		4.19	4.17	4.37	4.00	4.16	4.04	–	4.19	4.10	4.28	Vdc	14	15			–	–	–	16	–	–	12	8
		13	3.92	4.07	4.04		4.19	4.17	4.37	4.00	4.16	4.04		4.19	4.10	4.28	Vdc	15	14			–	–	–	16	–	–	13	8
	V_{OH2}	10	2.4	–	2.4			2.4	–	2.4	–	2.4			2.4	–	Vdc	15	14	–	–	–	11,16	–	–	–	10	–	8,9
Logic "0" Output Voltage	V_{OL1}*	12	3.18	3.39	3.21		3.44	3.25	3.50	3.19	3.43	3.21	–	3.44	3.23	3.47	Vdc	15	14			–	–	–	16	–	–	12	8
		13	3.18	3.39	3.21	–	3.44	3.25	3.50	3.19	3.43	3.21		3.44	3.23	3.47	Vdc	14	15			–	–	–	16	–	–	13	8
	V_{OL2}	10	–	0.5	–		0.5	–	0.5		0.5			0.5	–	0.5	Vdc	14	15	–	–	–	11,16	–	–	10	–	–	8,9
		10	–	0.5	–		0.5	–	0.5		0.5			0.5	–	0.5	Vdc	14	15			–		–	11,16	10	–	–	8,9
Logic "1" Threshold Voltage	V_{OHA}	12	3.90	–	4.02	–	–	4.15	–	3.98	–	4.02	–	–	4.08	–	Vdc	–		14	15	–	–	16	–	–	–	12	8
		13	3.90	–	4.02	–	–	4.15	–	3.98	–	4.02	–	–	4.08	–	Vdc			15	14	–	–	16	–	–	–	13	8
Logic "0" Threshold Voltage	V_{OLA}	12	–	3.41	–	–	3.46	–	3.52	–	3.45	–	–	3.46	–	3.49	Vdc		–	15	14	–	–	16	–	–	–	12	8
		13	–	3.41	–	–	3.46	–	3.52	–	3.45	–	–	3.46	–	3.49	Vdc	–	–	14	15	–	–	16	–	–	–	13	8
Output Short-Circuit Current	I_{OS}	10	20	60	20	–	60	20	60	20	60	20	–	60	20	60	mAdc	15	14	–	–	–	11,16	–	–	–	–	–	8,9,10

*Devices will meet standard MECL logic levels using V_{EE} = -5.2 Vdc and V_{CC} = 0

FIGURE 6 – AC CHARACTERISTICS – MECL AND MTTL OUTPUTS





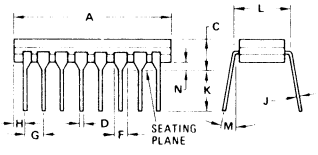
All input and output cables to the scope are equal lengths of 50 Ω coaxial cable.

Unused outputs are connected to a 50 Ω ±1% resistor to ground.

C_T = 15 pF = total parasitic capacitance which includes probe, wiring, and load capacitance.

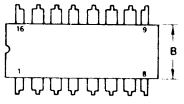
Characteristic	Symbol	Pin Under Test	MC12560, MC12561 -55°C Min	-55°C Max	+25°C Min	+25°C Typ	+25°C Max	+125°C Min	+125°C Max	MC12060, MC12061 0°C Min	0°C Max	+25°C Min	+25°C Typ	+25°C Max	+75°C Min	+75°C Max	Unit	TEST VOLTAGES/WAVEFORMS APPLIED TO PINS LISTED BELOW: Pulse In	Pulse Out	+2.0 Vdc	-3.0 Vdc	Gnd
Propagation Delay	t_{15+10+}	10	–	30	–	17	25	–	30	–	22	–	17	25	–	27	ns	15	10	11,16	8,9	14
	t_{15-10-}	10	–	22	–	12	18	–	22	–	19	–	12	18	–	18			10			
	t_{15+12-}	12	–	5.0	–	4.3	5.5	–	6.0	–	5.2	–	4.3	5.5	–	5.8			12			
	t_{15-12+}	12	–	4.8	–	3.7	5.2	–	5.5	–	5.0	–	3.7	5.2	–	5.2			12			
	t_{15+13+}	13	–	4.6	–	4.0	5.0	–	5.4	–	4.8	–	4.0	5.0	–	5.2			13			
	t_{15-13-}	13	–	5.0	–	4.0	5.0	–	5.2	–	5.0	–	4.0	5.0	–	5.1			13			
Rise Time	t_{12+}	12	–	3.8	–	3.0	4.0	–	5.0	–	4.0	–	3.0	4.0	–	4.4	ns	15	12	11,16	8,9	14
	t_{13+}	13	–	3.8	–	3.0	4.0	–	5.0	–	4.0	–	3.0	4.0	–	4.4	ns	15	13	11,16	8,9	14
Fall Time	t_{12-}	12	–	3.8	–	3.0	4.0	–	4.5	–	4.0	–	3.0	4.0	–	4.0	ns	15	12	11,16	8,9	14
	t_{13-}	13	–	3.8	–	3.0	4.0	–	4.5	–	4.0	–	3.0	4.0	–	4.0	ns	15	13	11,16	8,9	14

OUTLINE DIMENSIONS

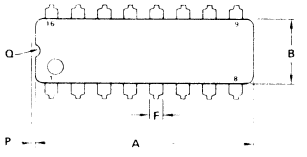


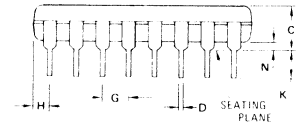
L SUFFIX
CERAMIC PACKAGE
CASE 620

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	19.05	19.81	0.750	0.780
B	6.22	6.98	0.245	0.275
C	4.06	5.08	0.160	0.200
D	0.38	0.51	0.015	0.020
F	1.40	1.65	0.055	0.065
G	2.54 BSC		0.100 BSC	
H	0.51	1.14	0.020	0.045
J	0.20	0.30	0.008	0.012
K	3.17	4.06	0.125	0.160
L	7.37	7.87	0.290	0.310
M	–	15°	–	15°
N	0.51	1.02	0.020	0.040



NOTES
1 LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION
2 PKG. INDEX: NOTCH IN LEAD
NOTCH IN CERAMIC OR INK DOT
3 DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL





P SUFFIX
PLASTIC PACKAGE
CASE 648

DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	20.70	21.34	0.815	0.840
B	6.10	6.60	0.240	0.260
C	4.06	4.57	0.160	0.180
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.32	1.83	0.052	0.072
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.37	7.87	0.290	0.310
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

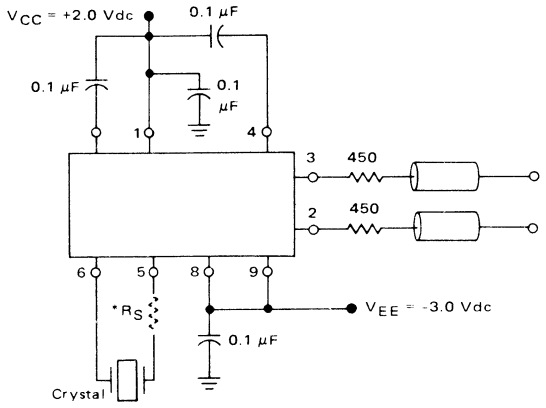
NOTES
1 DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL

FIGURE 7 – AC TEST CIRCUIT – SINE WAVE OUTPUT

Crystal – Reeves Hoffman Series Mode, Series Resistance Minimum at Fundamental
MC12060/12560:
f = 500 kHz
R_E = 1 k Ω
MC12061/12561:
f = 10 MHz
R_E = 5 Ω

*R_S – MC12060/12560 = 3 kΩ
MC12061/12561 = 150 Ω
R_S is inserted only for test purposes. When used with the above specified crystal, it guarantees oscillation with any crystal which has an equivalent series resistance ≤4 kΩ for MC12060/12560 and 155 Ω for MC12061/12561.

All output cables to the scope are equal lengths of 50 Ω coaxial cable. All unused cables must be terminated with a 50 Ω ±1% resistor to ground.
450 Ω resistor and the scope termination impedance constitute a 10:1 attenuator probe.



Characteristic	Pin Under Test	MC12560 MC12561 +25°C Min	MC12560 MC12561 +25°C Typ	MC12060 MC12061 +25°C Min	MC12060 MC12061 +25°C Typ	Unit	TEST VOLTAGE APPLIED TO PINS LISTED BELOW +2.0 Vdc	TEST VOLTAGE APPLIED TO PINS LISTED BELOW -3.0 Vdc
Sine Wave Amplitude								
MC12060/12560	2	600	675	500	650	mVp-p	1	8,9
	3	600	675	500	650			
MC12061/12561	2	700	750	650	750			
	3	700	750	650	750			

OPERATING CHARACTERISTICS

The MC12060/12560 and MC12061/12561 consist of three basic sections: an oscillator with AGC and two translators (Figure 1). Buffered complementary sine wave outputs are available from the oscillator section. The translators convert these sine wave outputs to levels compatible with MECL and/or MTTL.

Series mode crystals should be used with the oscillator. If it is necessary or desirable to adjust the crystal frequency, a reactive element can be inserted in series with the crystal – an inductor to lower the frequency or a capacitor to raise it. When such an adjustment is necessary, it is recommended that the crystal be specified slightly lower in frequency and a series trimmer capacitor be added to bring the oscillator back on frequency. As the oscillator frequency is changed from the natural resonance of the crystal, more and more dependence is placed on the external reactance, and temperature drift of the trimming components then affects overall oscillator performance.

The MC12060/12560 and MC12061/12561 are designed to operate from a single supply – either +5.0 Vdc or -5.2 Vdc. Although each translator has separate V_{CC} and V_{EE} supply pins, the circuit is NOT designed to operate from both voltage levels at the same time. The separate V_{EE} pin from the MTTL translator helps minimize transient disturbance. If neither translator is being used, all unused pins (9 thru 16) should be connected to V_{EE} (pin 8). With the translators not powered, supply current drain is typically reduced from 35 mA to 16 mA for the MC12060/12560, and from 42 mA to 23 mA for the MC12061/12561.

Frequency Stability

Output frequency of different oscillator circuits (of a given device type number) will vary somewhat when used with a given test setup, however the variation should be within approximately ±0.001% from unit to unit.

Frequency variations with temperature (independent of the crystal, which is held at 25°C) are small – about -0.08 ppm/°C for MC12061/12561 operating at 8.0 MHz, and about -0.16 ppm/°C for MC12060/12560 operating at 1.0 MHz (see Figure 8).

Signal Characteristics

The sine wave outputs at either pin 2 or pin 3 will typically range from 800 mVp-p (no load) to 500 mVp-p (120 ohm ac load). Approximately 500 mVp-p can be provided across 50 ohms by slightly increasing the dc current in the output buffer by the addition of an external resistor (680 ohms) from pin 2 or 3 to ground, as shown in Figure 9. Frequency drift is typically less than 0.0003% when going from a high-impedance load (1 megohm, 15 pF) to the 50-ohm load of Figure 9. The dc voltage level at pin 2 or 3 is nominally 3.5 Vdc with V_{CC} = +5.0 Vdc.

Harmonic distortion content in the sine wave outputs is crystal as well as circuit dependent. The largest harmonic (third) will usually be at least 15 dB down from the fundamental. The harmonic content is approximately load independent except that the higher harmonic levels (greater than the fifth) are increased when the MECL translator is being driven.

Typically, the MECL outputs (pins 12 and 13) will drive up to five gates, as defined in Figure 10, and the MTTL output (pin 10) will drive up to ten gates, as defined in Figure 11.

Noise Characteristics

Noise level evaluation of the sine wave outputs using the circuit of Figure 12, with operation at 1.0 MHz for MC12060/12560 or 9.0 MHz for MC12061/12561, indicates the following characteristics:

1. Noise floor (200 kHz from oscillator center frequency) is approximately -122 dB when referenced to a 1.0 Hz bandwidth. Noise floor is not sensitive to load conditions and/or translator operation.
2. Close-in noise (100 kHz from oscillator center frequency) is approximately -88 dB when referenced to a 1.0 Hz bandwidth.

FIGURE 8 – FREQUENCY SHIFT versus TEMPERATURE

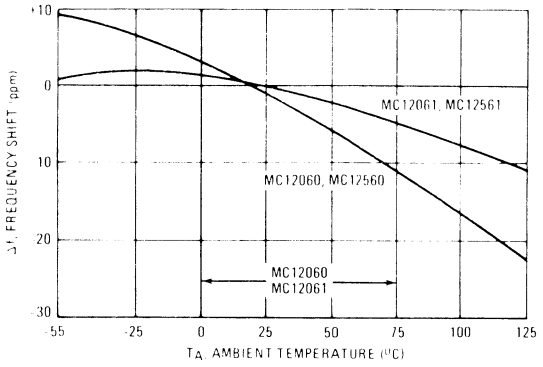
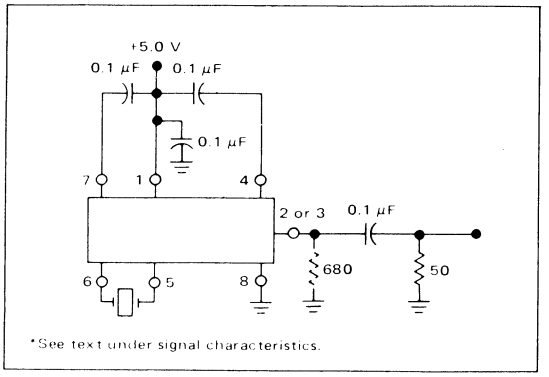


FIGURE 9 – DRIVING LOW-IMPEDANCE LOADS



*See text under signal characteristics.

FIGURE 10 – MECL TRANSLATOR LOAD CAPABILITY

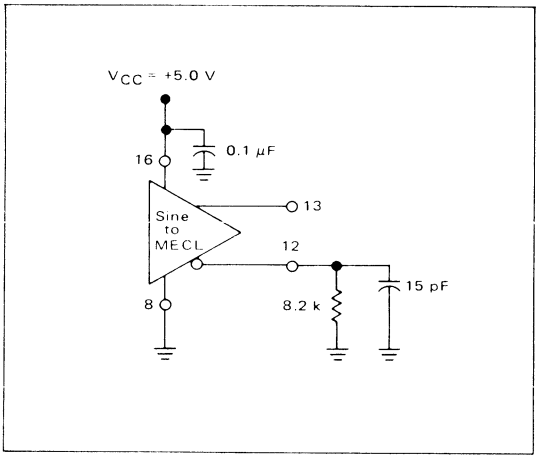


FIGURE 11 – MTTL TRANSLATOR LOAD CAPABILITY

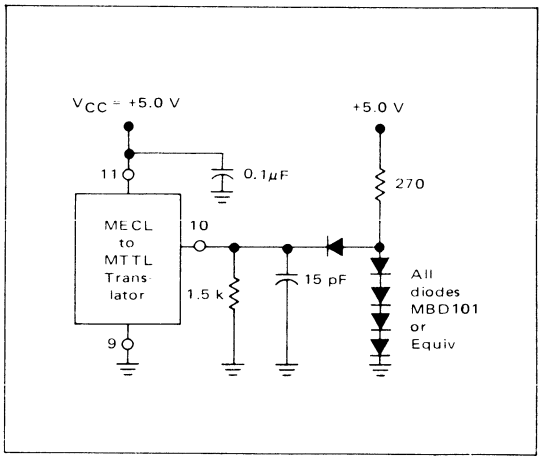
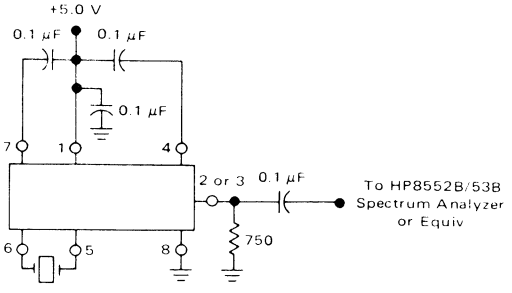


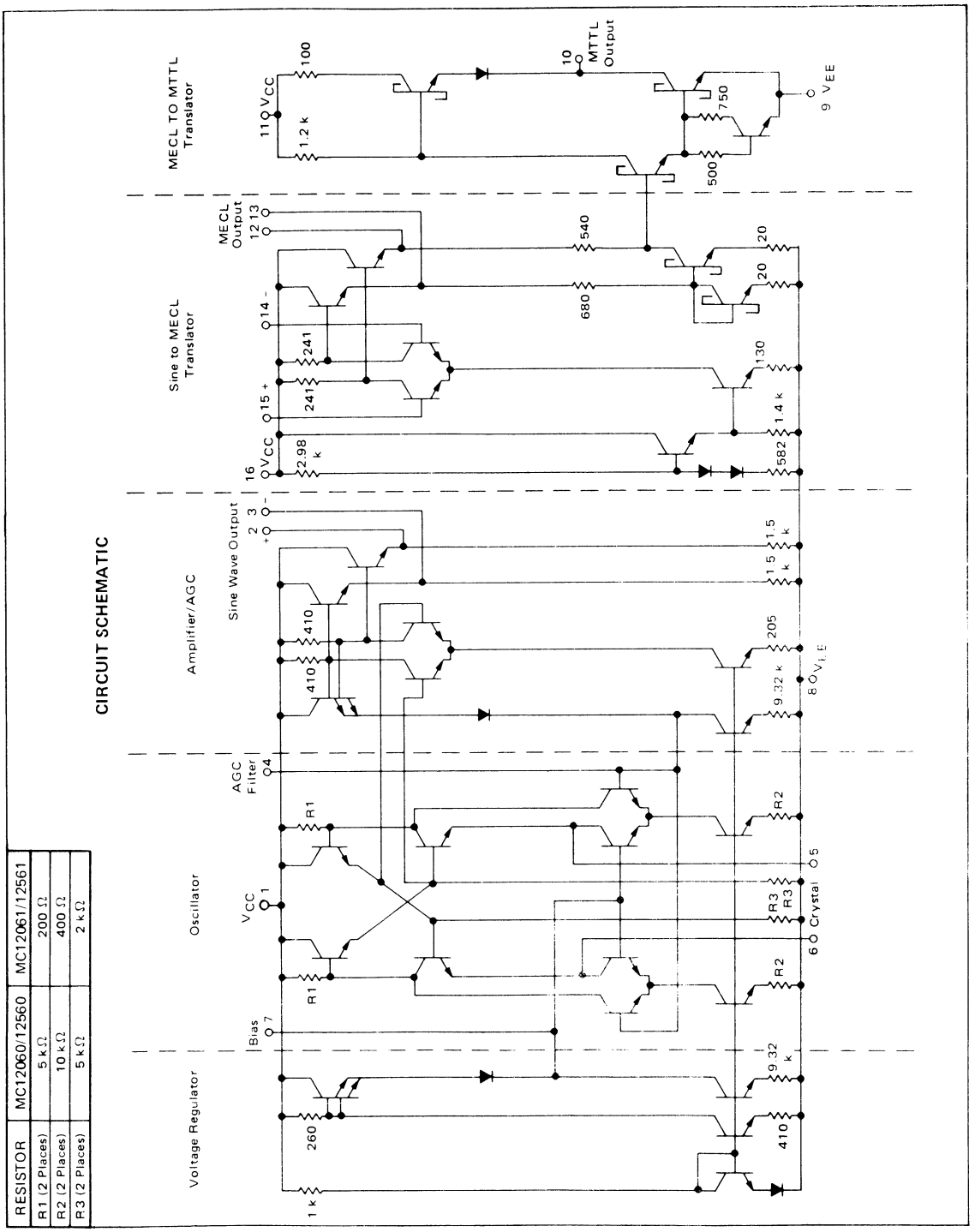
FIGURE 12 – NOISE MEASUREMENT TEST CIRCUIT



ANALYZER SETTING

Measurement	Sweep	Bandwidth	Video Filter
Noise Floor	50 kHz/div	10 kHz	10 Hz
Close In Noise	20 kHz/div	10 Hz	10 Hz

CIRCUIT SCHEMATIC



RESISTOR	MC12060/12560	MC12061/12561
R1 (2 Places)	5 kΩ	200 Ω
R2 (2 Places)	10 kΩ	400 Ω
R3 (2 Places)	5 kΩ	2 kΩ

EUROPEAN MOTOROLA SEMICONDUCTOR SALES OFFICES

DENMARK
Motorola A/S
Bredebovej 23
DK-2800 Lyngby
Tel. (02) 88 44 55

FRANCE
Motorola Semiconducteurs S.A.
Headquarter
15-17, avenue de Ségur
75007 Paris
Tel. 551 50 61
Sales Office
42, avenue de La Plaine-Fleurie
38240 Meylan (Grenoble)
Tel. (76) 90 22 81

WEST GERMANY
Motorola GmbH, Geschäftsbereich Halbleiter
Headquarter
Munchner Strasse 18
8043 Unterföhring
Tel. (089) 92 481
Sales Offices
Hans-Böckler-Strasse 30
3012 Langenhagen – Hannover
Tel. (0511) 77 20 37
Virnsbergerstrasse 43
8500 Nürnberg
Tel. (0911) 6 57 61
Stralsunder Strasse 1
7032 Sindelfingen
Tel. (07031) 8 30 74/8 30 75
Abraham-Lincoln-Strasse 28
6200 Wiesbaden
Tel. (06121) 76 19 21

HOLLAND
Motorola B.V.
Emmalaan 41
Utrecht
Tel. (030) 51 02 07

ITALY
Motorola S.p.A.
Headquarter
Via Ciro Menotti 11
20129 Milano
Tel. 738 6
Sales Office
Via Portanova 10
40123 Bologna – Tel. 26 69 05
Sales Office
Via Costantino Maes 68
00162 Roma – Tel. 831 47 46

NORWAY
Motorola A/B.
Brugt. 1
Oslo 1 – Tel. (02) 41 91 40

SOUTH AFRICA
Motorola South Africa (Pty) Ltd.
P.O. Box 39586
Bramley 2018
Tel. 786 11 84

SWEDEN
Motorola AB.
Virebergsvagen 19
17140 Solna – Tel. (08) 82 02 95

SWITZERLAND
Motorola Semiconductor Products S.A.
Alte Landstrasse 101
8700 Zollikon – Tel. (01) 65 56 56

UNITED KINGDOM
Motorola Ltd.
Headquarter
York House, Empire Way
Wembley Middlesex
Tel. (01) 902 88 36
Sales Office
10-12, Mount Street, Television House
Manchester M2 5WS, Lancs
Tel. (61) 833 07 31/833 07 34
Sales Office
Colvilles Road, Kelvin Estate
East Kilbride, Scotland
Tel. (3552) 3 91 01

HEADQUARTERS EUROPEAN OPERATIONS

SWITZERLAND
Motorola Inc.
Semiconductor Products Group
16, chemin de la Voie-Creuse, P.O. Box 8
1211 Genève 20
Tel. (022) 33 56 07

FRANCHISED I

ITORS

AUSTRIA
Elbatex GmbH
Endresstrasse 54 – 1238 Wien
Tel. (222) 88 55 11

BELGIUM
Diode Belgium
Rue Picard 202-204 – 1020 Bruxelles
Tel. (02) 428 51 05

DENMARK
GDS-Henckel ApS
Fyrrevangen 4 – 4622 Havdrup
Tel. (03) 38 57 16

FINLAND
Field Oy
Veneentekijantie 18 – 00210 Helsinki 21
Tel. (80) 692 25 77

FRANCE
Bellion Electronique
Zone Industrielle de Kerscao/Brest
29219 Le Relecq-Kerhuon – B.P. 16
Tel. (98) 28 03 03
Celdis S.A.
53, rue Charles-Frérot – 94250 Gentilly
Tel. (01) 581 00 20
Ets. F. Feutrier S.A. (Main Office)
Rue des Trois-Glorieuses
42270 St-Priest-en-Jarez (St-Etienne)
Tel. (77) 74 67 33
Ets. F. Feutrier S.A.
Avenue Laplace – Zone industrielle
13470 Carnoux
Tel. (42) 82 16 41
Feutrier Ile de France
29, rue Ledru-Rollin – 92150 Suresnes
Tel. (01) 772 46 46
Ets. Gros S.A. (Main Office)
13, rue Victor-Hugo – 59350 St-André-lez-Lille
Tel. (20) 51 21 33
Ets. Gros S.A.
14, avenue du Général-Leclerc – 54000 Nancy
Tel. (28) 35 17 35
Ets. Gros S.A.
5, rue Pascal – 94800 Villejuif
Tel. (01) 678 27 27
S.C.A.I.B. S.A.
80, rue d'Arcueil – Zone Silic
94150 Rungis
Tel. (01) 687 23 13
Sté. Commerciale Toutélectric (Main Office)
15-17, boulevard Bonrepos
31008 Toulouse
Tel. (61) 62 11 33
Sté. Commerciale Toutélectric
80-83, quai des Queyries – 33100 Bordeaux
Tel. (56) 86 50 31

GERMANY
Alfred Neye Enstechnik GmbH (Ab 1.1.1979)
Schillerstrasse 14 – D-2085 Quickborn/Hamburg
Tel. (04) 106 61 21
Distron GmbH & Co.
Behaimstrasse 3 – P.O. Box 100 208
1000 Berlin 10
Tel. (030) 342 10 41/45
EBV Elektronik Vertriebs-GmbH (Main Office)
Gabriel-Max-Strasse 72
8000 Munchen 90
Tel. (089) 64 40 55
EBV Elektronik Vertriebs GmbH
In der Meineworth 9
3006 Burgwebel 1 / Hannover
Tel. (0511) 39 45 70
EBV Elektronik Vertriebs-GmbH
Osstrasse 129
4000 Dusseldorf
Tel. (0211) 8 48 46
EBV Elek
Myliusstra
6000 Fran
Tel. (0611)
EBV Elektronik Vertriebs-GmbH
Alexanderstrasse 63
7000 Stuttgart 1
Tel. (0711) 24 74 81
Jermyn GmbH
Postfach 1180
6277 Camberg
Tel. (06434) 60 05
Mütron Müller & Co. KG
Bornstrasse 22
2800 Bremen
Tel. (0421) 31 04 85
RTG, E. Springorum KG (Main Office)
Postfach 426
46 Dortmund 1
Tel. (0231) 5 49 51
RTG, E. Springorum KG
Friedrich-Ebert-Damm 112
2000 Hamburg 70
Tel. (040) 693 70 61/62
RTG, E. Springorum KG
Ungererstrasse 43
8000 Munchen 40
Tel. (089) 36 65 00
RTG, E. Springorum KG
Reutlingerstrasse 87
7000 Stuttgart-Degerloch
Tel. (0711) 76 64 28
RTG, E. Springorum KG
Mendelssohn-Bartholdy-Strasse 16
6200 Wiesbaden
Tel. (06121) 52 73 09
SASCO Vertrieb von elektronischen Bauelementen GmbH (Main Office)
Hermann-Oberth-Strasse 16
8001 Putzbrunn b. Munchen
Tel. (089) 46 40 61/69
SASCO Vertrieb von elektronischen Bauelementen GmbH
Postfach 3066
4005 Dusseldorf/Meerbusch 3
Tel. (02150) 14 33
SASCO Vertrieb von elektronischen Bauelementen GmbH
Postfach 890214
3000 Hannover
Tel. (0511) 86 25 86
SASCO Vertrieb von elektronischen Bauelementen GmbH
Lorenzer Strasse 15
8500 Nürnberg
Tel. (0911) 20 41 52
SASCO Vertrieb von elektronischen Bauelementen GmbH
Staffienbergstrasse 24 – 7000 Stuttgart 1
Tel. (0711) 24 45 21
SPOERLE Electronic (Ab 1.1.1979)
Otto-Hahn-Strasse 13 – 6072 Dreieich b. Frankfurt
Tel. (06103) * 3 04-1
Technoprojekt (Main Office)
Heinrich-Ebner-Strasse 13
7000 Stuttgart – Bad Cannstatt
Tel. (0711) 56 17 12
Technoprojekt
Ostring 150 – 6231 Schwalbach/Ts
Tel. (06196) 8 21 00

GREECE
Macedonian Electronics Ltd.
Charilaou – P.O. Box 240 – Thessaloniki
Tel. 30 68 00
Macedonian Electronics Ltd.
Lloyd George 10 – Athens
Tel. (21) 360 95 71

Manudax Naderland B.V.
Meerstraat 7
5473 ZG Heeswijk (N.B.) – P.O. Box 25
Tel. (41) 39 12 52

HUNGARY
Interag Co., Ltd.
XIII Rajk Laszlo u. 11 – P.O. Box 184
1330 Budapest
Tel. (1) 32 93 40

IRAN
Milcom LTD, Motorola Building
Niloo Street, Vanak Square – Teheran
Tel. 66 12 14/15

ITALY
Celdis Italiana S.p.A. (Main Office)
Via F.lli Gracchi 36 – 20092 Cinisello Balsamo (MI)
Tel. (02) 612 00 41-2-3-4-5
Celdis Italiana S.p.A.
Via Lorenzo il Magnifico 109 – 00162 Roma
Tel. (06) 42 38 55
Celdis Italiana S.p.A.
Via Turati, 33 – 40055 Castenaso (Bologna)
Tel. (051) 78 80 78
Celdis Italiana S.p.A.
Via Mombarcaro 96 – 10136 Torino
Tel. (11) 35 93 12
Celdis Italiana S.p.A.
Via Ognissanti, 83 – 35100 Padova
Tel. (049) 2 68 02
Cramer Italia S.p.A. (Main Office)
Via Cristoforo Colombo 134 – 00147 Roma
Tel. (06) 51 79 81-2-3-4-5-6-7
Cramer Italia S.p.A.
Via S. Simpliciano 2 – 20121 Milano
Tel. (02) 80 93 26
Cramer Italia S.p.A.
Via Umberto 1 59 – 35100 Padova
Tel. (049) 2 53 74
Cramer Italia S.p.A.
Via Malta 5 – 40135 Bologna
Tel. (051) 42 28 90
Cramer Italia S.p.A.
Corso Traiano 28/15 – 10135 Torino
Tel. (011) 619 20 62
Silverstar Ltd. S.p.A.
Via dei Gracchi 20 – 20146 Milano
Tel. (02) 49 96
Silverstar Ltd. S.p.A.
Via Paisiello 30 – 00198 Roma
Tel. (06) 844 88 41
Silverstar Ltd. S.p.A.
Piazza Adriano 9 – 10139 Torino
Tel. (011) 44 32 75/6 – 44 23 21

NIGERIA
Beckron International
14, Alhaji Bashorun Street
SW Ikoyi – P.O. Box 1896 – Lagos
Tel. 5 66 29

NORWAY
Ola Tandberg Elektro A/S
Skedsmogatan 25 – Oslo 6
Tel. (02) 19 70 30

POLAND
PHZ Transpol S.A. (Intraco Building)
Ul. Stawki 2 – 00-950 Warsaw 1
Tel. (004822) 39 50 79

PORTUGAL
Equipamentos de Laboratorio LDA
Rua Pedro Nunes 47 – Lisbon 1
Tel. 97 02 51

SOUTH AFRICA
L'Electron
704 Main Pretoria Road, Wynberg Tvl.
P.O. Box 10544, Johannesburg 2000
Tel. 40 62 96

SPAIN
Hispano Electronica S.A. (Main Office)
Polígono Industrial "Urtinsa"
Apartado de Correos 48 – Alcorcón (Madrid)
Tel. (01) 619 41 08
Hispano Electronica S.A.
Figols, 27-29
Barcelona 14 – Tel. 259 05 22/23

SWEDEN
Interelko AB.
Sandsborgsvagen 50
12233 Enskede – Tel. (08) 49 25 05
AB Gösta Bäckström
Alströmergatan 22 – Box 12009
10221 Stockholm
Tel. (08) 54 10 80

SWITZERLAND
Elbatex AG
Alb. Zwyssig-Strasse 28 – 5430 Wettingen
Tel. (056) 26 56 41
Omni Ray AG
Dufourstrasse 56 – 8008 Zurich
Tel. (01) 34 07 66

TURKEY
ERA Elektronik Sanyi Ve Ticaret A.S.
Ankara Irtibat Bürosu
Gazi Mustapha Kemal Bul. 12
KAT4D79 Yenisehir/Ankara – Tel. 25 49 33

UNITED KINGDOM
A.M. Lock & Co. Ltd
Neville Street, Middleton Road
Oldham, Lancs OL96LF
Tel. (061) 652 04 31
Celdis Ltd.
37-39 Loverock Road
Reading, Berks, RG3, 1ED
Tel. (0734) 585 171
Cramer Components Ltd
Hawke House Green Street
Sunbury on Thames, Middlesex, England
Tel. (9327) 8 55 77
Crellon Electronics Ltd.
380, Bath Road
Slough, Berks SL1 6JE
Tel. (06286) 6 36 11
ITT Electronic Services
Edinburgh Way
Harlow, Essex CM20 (2DF)
Tel. Harlow (0279) 26 777
Jermyn Industries
Vestry Estate – Sevenoaks, Kent
Tel. (732) 5 11 74
Macro-Marketing Ltd.
396, Bath Road
Slough, Berks SL1 6JD
Tel. (06286) 630 11

YUGOSLAVIA
Elektrotehna Ljubljana
Export-Import
Titova 51 – P.O. Box 34 1
61000 Ljubljana
Tel. (61) 32 02 41
Elektrotehna Ljubljana
Filiala Beograd
Marsala Tita 61
11000 Beograd
Tel. (011) 69 69 24

EUROPEAN SEMICONDUCTOR FACTORIES

FRANCE
Motorola Semiconducteurs S.A.
Canto Laouzetto – Le Mirail
31023 Toulouse CEDEX
Tel. (61) 40 11 88

GERMANY
Motorola GmbH
Munchner Strasse 18
8043 Unterföhring
Tel. (089) 92 481

UNITED KINGDOM
Motorola Semiconductors Ltd.
Colvilles Road, Kelvin Estate
East Kilbride/Glasgow (Scotland)
Tel. (3552) 39 101